A HIGH PERFORMANCE CLASS-D AMPLIFIER WITH
CASCADED SIGMA-DELTA MODULATORS

by

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ABSTRACT

The focus of this thesis is on analysis, simulation and board level implementation of the proposed Class-D power amplifier architecture. The structural design consists of two Sigma-Delta Modulator (SDM) stages in cascade with an intermediate decimation-filter between them. Noise and high tone introduced at the first- stage is filter out through the decimation filter. The signal is converted to a 1-bit Pulse Duration Modulation (PDM) signal by the second stage SDM. The H-Bridge is made part of the SD loop, which enables not only the noise shaping of the quantization noise but also stabilizes the output power switching stage. Output of the H-Bridge is converted to a digital signal using a comparator and latch circuitry and is fed back. To further increase the linearity and performance, high frequency ripples introduced at the H-Bridge is quantized by using a 4-bit SD Analog-to-Digital Converter (ADC) in the feedback loop. Due to the intermediate digital stage and the feedback control at the output stage, the proposed structure has high efficiency and linearity and still is very compact making it possible for wide range of applications.

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CHAPTER I

INTRODUCTION

1.1 Motivation

Amplifiers boost the weak signal and generate a powerful signal which drives the speaker. In general power amplifiers (PA) are classified in two broad categories – linear and non-linear. A detailed explanation of different classes of PA can be found in [3]. A few of the basic and important classes are briefed here. In PA terminology, a linear PA is the one which has a linear relationship between its input and output.

Class-A amplifier, the most basic one, use one or more transistors that conduct during both the positive and negative half cycles of the signal i.e. the conduction angle is 360° and operates over a linear portion of its characteristics. It has very low distortion but it is very inefficient and generates a lot of heat. It requires that the amplifier should generate full power regardless of the output. In this case, relative to the desired output power, there is a great deal of power consumed, over and beyond what is being used to drive the load. Ideally, the power consumed in the device should be zero, allowing all the power coming from the supply to be directed to the output. As a result, Class-A is used only in those situations where either the linearity requirements are so stringent as to necessitate an entirely linear output stage. Fig. 1.1 shows the basic structure of a Class-A amplifier.

Fig. 1.1: Class-A Amplifier

In order to increase efficiency, Class-B amplifiers use two transistors to conduct during both positive and negative cycle of the input waveform as shown in Fig. 1.2. The main disadvantage of the Class-B amplifier is the crossover distortion. The crossover distortion occurs when one transistor is turned off and the other is turned on and there is a portion of time when neither is conducting which reduces the linearity of the amplifier. Moreover, if different transistors – NMOS and PMOS are used as push and pull devices, it will further degrade the linearity, since NMOS and PMOS have different characteristics.

Fig. 1.2: Class-B Amplifier

Class-AB is most widely used for audio applications. The linearity achieved with this structure is still good in addition to elimination of the cross-over distortion that can cause problems in Class-B. In these amplifiers both transistors conduct for sometime and there is an overlap of current through the transistors. This produces distortion called gumming where the signal would get a little fatter when the two transistors are simultaneously conducting.

A Class-C amplifier is the one in which the operating point is chosen such that the output current (or voltage) is zero for more than one half of an input signal. This cannot be used for an audio signal.

Class-D amplifier, as shown in Fig. 1.3 has emerged as the high efficiency solution for audio applications. In this amplifier a pulse code modulation (PCM) data stream is converted to a two level signal (pulse width modulation – PWM), which drives the power MOSFET switches (H-Bridge). Output waveform is converted into an analog signal by a lowpass filter. The switching elements allow high efficiency and this leads to smaller heat sink and size. While the Class-D amplification is very efficient, analog PWM is highly non-linear and noisy. Amplifiers based on this conversion technique are not very competitive and could never replace the well-established Class-AB amplifiers.

Fig. 1.3: Class-D Amplifier

To perform high quality power conversion following criteria must be satisfied:

- Linearity of the output signal in the audio band to avoid harmonic distortion.
- High timing accuracy for the switching-points of the pulses to give a precise representation of the input level in the mean value of the pulses.
- Stable power supply for the switching levels. Variations in the switching levels lead to distortions and further modulation products.
- Sharp edges to create a nearly ideal rectangular form of the pulses.

- Feedback from the output to cancel errors produced by the power circuitry.
- Reduction of Electromagnetic Interference (EMI).

Recently, using digital signal processing, digital PWM and Sigma-Delta Modulation (SDM), has attracted interest as an alternative to traditional conversion technique. As compared to SDM, PWM offers the lower switching frequency, but without proper linearization it introduces distortion in the audio band. The linearization methods based on interpolation and non-linear modeling require high computational power. The SDM is a more linear method, if the presence of idle tones is reduced by dithering [1]. However, SDM produces bit-stream which is uniformly distributed over the oversampling period. This causes high switching frequencies in the output power stage.

The introduction of feedback from the filtered or unfiltered output provides a possibility to control the distortions caused by output stage. The use of feedback implies a conversion from the analogue to the digital domain using high resolution Analog-to-Digital Converter (ADC). This causes increase in chip area and delay in the feedback path which makes the system unstable. Another methodology is to implement the power stage in analog domain and provide the feedback path. This however imposes practical problems associated with analog circuitry.

The proposed structure of Class-D amplifier employs cascaded SDM in digital domain with an intermediate digital filter to get around some of the shortcomings of previous designs. The switching frequency of H-Bridge is reduced by Pulse Group Modulation (PGM) technique. The feedback is implemented using 4-bit SD-ADC which takes care of nonlinearities at the output. The architecture is simulated in SIMULINK and

design is verified by board level implementation using Motorola - 68HC12 and TI-TMS6211 fixed point processor.

1.2 Organization of the Thesis

The remainder of the thesis is organized as follows. Chapter II and Chapter III depicts basic building blocks of the Class-D amplifier. Chapter II consists of sigma-delta modulation techniques and states how Pulse Duration Modulation (PDM) can be used to drive the H-Bridge. PWM generation techniques and H-Bridge circuits are covered in Chapter III. Chapter IV covers various non-idealities introduced due to pre-processing and power output stage of Class-D amplifier. In Chapter V, various preliminary architectures are simulated and their problems from implementation and efficiency stand point are discussed. Chapter VI consists of proposed structures with simulation results including various circuit non-idealities. In Chapter VII, implementation details of the output power stage using Motorola 68HC12 EVM and pre-processing stage using DSP – fixed point processor TMS320C6211 are discussed. Finally, Chapter VIII includes conclusions of design along with future work which can be done to improve the amplifier's performance.

CHAPTER II

BASIC BUILDING BLOCKS – I

2.1 Sigma-Delta Modulation (SDM)

As the name implies in a sigma-delta modulation (SDM) the input is integrated (sigma) prior to delta modulation coding. The signal amplitude remains constant with the increasing frequency, hence SDM is also known as pulse density modulation (PDM). In SDM signal is been quantized directly and not its derivative as in Delta Modulation (DM). Hence maximum quantizer range is determined by the maximum signal amplitude and is not dependent on the signal spectrum. The SDM is achieved by over-sampling the input data and shaping the quantization noise. Descriptions of SDM from theory, design, and simulation point of view are detailed in [1, 2].

2.1.1 Over-Sampling

Extra dynamic range can be achieved by spreading the quantization noise power over a larger frequency range. The increase in the dynamic range is only 3dB for every doubling of the sampling frequency.

2.1.2 White Noise Assumption

If $x(n)$ is very active, $e(n)$ can be approximated as an independent random number uniformly distributed between $-\Delta/2$ and $\Delta/2$, where $x(n)$ is the input sample, $e(n)$ is the quantization error for that sample and Δ is equal to the difference between two adjacent quantization levels. The quantization noise power is $\Delta^2/12$ and is independent of the

sampling frequency f_s . Also the spectral density of $e(n)$, $S_e(f)$ is white and all its power lies within $-f_s/2$ and $+f_s/2$ [3].

Fig. 2.1: Noise Power Spectrum Density

As shown in the Fig. 2.1, if quantization noise is assumed to be constant for the entire frequency range, the total noise in the band of interest can be reduced.

2.1.3 Over-sampling with Noise Shaping

Noise shaping implies that the noise in the band of interest is reduced and is increased out of the band. But the overall noise remains the same for the entire band. The system architecture of the SD over-sampling converters and its equivalent linear model are shown in Fig. 2.2 and Fig. 2.4

2.2 SDM in Digital and Analog Domain

Normally SDM is used in analog-to-digital converters (ADC) and digital-to-analog converters (DAC). The SDM noise or error introduced in the quantizer is shaped

Fig. 2.2: Sigma-Delta Modulator

by oversampling the output signal and feeding it back to correct the input signal as shown in Fig. 2.2. The quantized oversampled output is passed through a cascade of digital lowpass filter and downsampler, which converts the signal into Nyquist rate [1, 2]. The SDM can also be used in an all-digital domain, as shown in Fig. 2.3, where an input PCM signal with N bits are reduced to N' bits ($N' < N$). Here the quantization noise introduced due to truncation of bits is shaped. Integrator is replaced by digital counter and in the feedback N' bits are converted to N bits simply by appending $(N - N')$ zeros to the output.

Fig. 2.3: SDM in Digital Domain

2.2.1 SDM Analysis

Behavioral modeling of SDM is done in the analog domain. Analog input signal is passed through a 1-bit quantizer, and this quantized analog signal is fed back to the input

Fig. 2.4: General SDM (interpolator structure)

as shown in Fig. 2.4.

Fig. 2.5: Linear Model of the Modulator showing the Quantization Noise

Treating the linear model as shown in Fig. 2.5, as having two independent inputs, signal transfer functions are given by

$$S_{TF}(z) = \frac{Y(z)}{U(z)} = \frac{H(z)}{(1 + H(z))} \quad (2.1)$$

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = \frac{1}{1 + H(z)} \quad (2.2)$$

Hence, zeros of noise transfer function, $N_{TF}(z)$ will be equal to poles of $H(z)$. We want our system such that $N_{TF}(z)$ should have a zero at d.c. To realize this, $H(z)$ is chosen such that it has a pole at $z = 1$, i.e.,

$$H(z) = \frac{1}{(z - 1)} \Rightarrow \frac{z^{-1}}{(1 - z^{-1})} \quad (2.3)$$

The corresponding transfer function in the frequency domain is given by,

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z). \quad (2.4)$$

Hence first-order noise shaping can be achieved by letting $H(z)$ be a discrete time integrator. Output of the system though quantized has high frequency components and is passed through a decimation filter, which is a combination of a digital lowpass filter and a down-sampler. It can be shown that peak Signal to Noise Ratio (SNR) for first-order noise shaper is given by

$$SNR = 6.02n + 1.76 - 5.17 + 30 \log(OSR). \quad (2.5)$$

SIMULINK model for the first-order 1-bit Sigma-Delta with simulation results is shown in Fig. 2.6. The sinusoidal input is given to the system and the digital output from the quantizer is fed to lowpass filter which acts as a reconstruction filter. Finally, output from this lowpass filter is compared with the original signal both in the time and frequency domain.

Fig. 2.6: Sigma Delta Modulator – SIMULINK MODEL

Fig. 2.7 shows the implementation of an integrator as a subsystem.

Fig. 2.7: Ideal Integrator

Practically integrator saturates at a particular value and also has a leakage.

Transfer function of the integrator with saturation and leakage is given by

$$\Rightarrow \frac{az^{-1}}{(1-bz^{-1})}$$

where a and b are leakage and saturation constant, respectively.

Fig. 2.8 shows model of an integrator with non-idealities.

Fig. 2.8: Non-Ideal Integrator

2.2.2 The second-order converter

The modulator shown in Fig. 2.9 also known as Candy Structure [3], realizes a second-order A/D Converter where the noise transfer function is given by

$$N_{TF}(z) = (1 - z^{-1})^2. \quad (2.6)$$

Maximum SNR assuming maximum signal power obtained is

$$SNR_{\max} = 6.02n + 1.76 - 12.9 + 50 \log(0.5R). \quad (2.7)$$

Hence, a second-order modulator gives improvement of 12-15dB over first-order structure.

Fi

Fig. 2.9: Second-Order Modulator

2.3 Higher-Order Structures

Generally an Mth-order noise shaper structure improves SNR by $6M + 3$ dB/octave. Higher order modulators can be realized by cascading first- order modulators, but such realization is difficult because for large signal, modulator may go unstable and never return to stability.

2.3.1 Multi-Stage Noise Shaping (MASH) Architecture

Alternative approach for realizing higher order modulators is to use cascade structure in the feedforward manner, where higher order modulator is constructed using lower order modulators. Since lower order structures are more stable, the overall structure remains stable [3].

2.3.2 Second-Order MASH

The arrangement for realizing a second-order modulator using two first-order modulators is shown in Fig. 2.10. The idea is to pass the error from the first stage to the second stage of the modulator and combine the output of the two stages in such a manner that error introduced due to the first stage can be completely removed. Transfer function for output of each stage $Y_1(z)$ and $Y_2(z)$ are obtained as,

$$Y_1(z) = z^{-1}X(z) + (1 - z^{-1})E_1(z) \quad (2.8)$$

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z) \quad (2.9)$$

If equation (2.8) is multiplied by z^{-1} and equation (2.9) by $1 - z^{-1}$ and then subtracting the resulting equations, we get

$$Y(z) = z^{-2} X(z) - (1 - z^{-1})^2 E_2(z). \quad (2.10)$$

The digital cancellation block is shown in Fig. 2.11. It is seen that $E_1(z)$ has been completely eliminated while the quantization noise $E_2(z)$ is now second-order shaped. Hence as compared to Candy structure this structure has less quantization error and accordingly has higher SNR.

Fig. 2.10: Second-order MASH structure

2.3.3 Digital Cancellation Logic Block for 1-1 MASH

Fig. 2.11: Digital Cancellation Structure

2.3.4 Third-order MASH

A third-order MASH can be realized by two methods. One way is termed as 2-1 in which there are two stages. First stage has a second-order modulator and second stage has a first-order modulator. Other method is 1-1-1, which consists of 3 stages each with a first-order modulator. Consider a 1-1-1 third-order MASH as shown in Fig. 2.12. Output of each stage is given as,

$$Y_1(z) = z^{-1}X(z) + (1 - z^{-1})E_1(z) \quad (2.11)$$

$$Y_2(z) = z^{-1}E_1(z) + (1 - z^{-1})E_2(z) \quad (2.12)$$

$$Y_3(z) = z^{-1}E_2(z) + (1 - z^{-1})E_3(z). \quad (2.13)$$

Now these outputs are combined together such that $E_1(z)$ and $E_2(z)$ are canceled out.

Hence output of the overall modulator is,

$$Y(z) = z^{-3}X(z) + (1 - z^{-1})^3 E_3(z). \quad (2.14)$$

Fig. 2.12: Third-order (1-1-1) MASH structure

2.3.5 Digital Cancellation Logic Block for 1-1-1 MASH

Outputs from each stage are combined in the manner shown in Fig. 2.13 such that the output is given as,

$$Y(z) = z^{-2}Y_1(z) - (1 - z^{-1}) \cdot z^{-1}Y_2(z) + (1 - z^{-1})^2 Y_3(z) \quad (2.15)$$

Fig. 2.13: Digital Cancellation Logic for third-order SDM

2.4 Results for Different SDM Structures

Table 2.1 Simulation parameters for SDM

Bandwidth	16 kHz
Input frequency	2 kHz
FFT points	2^{15}
Cut-off frequency of butter-worth filter f_c	16 kHz
Total Leakage factor	0.999
Saturation	± 1.5
OSR	16

Fig. 2.14: Simulation Results for first-order SDM

Fig. 2.14 shows 200 samples of input, quantization output and reconstructed output obtained by a lowpass filter, for first-order 1-bit SDM in time domain. Higher the order of the reconstruction filter, lesser would be the ripple at the output. Hence to obtain perfected signal we need higher order lowpass filter at the output. Generally for the L th-order SDM, $(L+1)$ th-order lowpass filter is required.

Fig. 2.15: Comparison of SNR for different SDM Structures

Fig. 2.15 compares SNR for different SDM structures in frequency domain. Higher-order structures have better SNR [3] but as mentioned earlier they are more

unstable and poles tend to go out of the unit circle. MASH structures, however, are stable and give high SNR.

2.5 Continuous Time Sigma-Delta Modulation

The use of continuous time (CT) Sigma Delta Modulators provide many advantages over the Discrete Time (DT) modulators. It is due to the fact that only the quantizer enforces constraint on the maximum sampling frequency. Hence integrators with lower Gain Bandwidth Product (GBP) can be used. This is useful for low power design since overall power consumption is smaller. However, CT SDM is difficult to design. Another disadvantage is that impact of non-idealities like clock jitter and loop delay is more [10].

To analyze the performance of CT modulator, its equivalence with DT modulator is drawn as shown in Fig. 2.16. Since quantizer operates at a particular clock frequency, the overall loop is discrete and hence it will produce same output bits as the DT modulator at same time instances, i.e., $z(nT) = z[n]$.

Figure 2.16: DT Equivalent of CT structure

Fig. 2.17 and Fig. 2.18 show the SIMULINK model and the frequency response of the CT SDM structure. From simulation results, it follows that the frequency response of CT SDM is same as that of DT SDM.

Fig. 2.17: CT SDM structure

Fig. 2.18: CT SDM Simulation Results

CHAPTER III

BASIC BUILDING BLOCKS – II

3.1 Pulse Width Modulation

Pulse width modulation (PWM) is a technique that provides a logic '0' and logic '1' for the controlled period of time. Essentially, pulse width modulation refers to a method of carrying information on a train of pulses with the information being encoded in the width of the pulses. PWM is employed in a wide variety of applications, ranging from measurement and communications to power control and conversion.

A PWM signal is not constant. Rather, the signal is on for part of its period, and off for the rest. The duty cycle (DC) refers to the percentage of the period for which the signal is on. The duty cycle can be anywhere from 0, where the signal is always off, to 1, where the signal is constantly on. A 50% D.C. results in a perfect square wave. Fig. 3.1 shows the on time variation [5, 8] for the output square wave.

Fig. 3.1: Variable duty cycle for PWM

3.2 Analog signal-to-PWM Generation

Analog input signal having f_s as the sampling rate is compared to a high frequency saw-tooth comparison waveform with period T_c . As shown in Fig. 3.2, the input signal is applied to the non-inverting terminal of the comparator. The output of the comparator changes state such that a PWM waveform with 'pulse repetition frequency, $f_c = 1/T_c$, is produced. This is known as 'Natural Sampling PWM' (NPWM) as opposed to 'Uniform Sampling PWM' (UPWM) which is produced when input analog signal is sampled with zero-order hold.

Fig. 3.2: PWM waveform generation

PWM generation by this method is known as 'single-sided' modulation scheme. If triangular waveform is used for comparison, both edges of PWM are modulated and scheme is known as 'double-sided' modulation scheme [13].

3.2.1 Pulse-Code-Modulation (PCM) to PWM Conversion

PCM to PWM conversion consists of N bit input digital sampled to 1-bit output. This is carried out using digital algorithm based on binary conversion routine, e.g., for a 4-bit unsigned sample 0 1 1 0, DC is computed as,

$$\frac{0*2^0 + 1*2^1 + 1*2^2 + 0*2^3}{1*2^0 + 1*2^1 + 1*2^2 + 1*2^3} = \frac{6}{15}. \quad (3.1)$$

Maximum value a signal can have is 1. Hence to represent a 4-bit PCM input signal by a PWM signal, the input signal is oversampled by 16. Usually, input signal is over-sampled by 2^N , where N is the number of input PCM bits.

3.3 Distortion in PWM

Fundamentally, PWM is a non-linear process. The spectrum of the output pulse-series contains the pulse repetition frequency and its harmonics plus the spectral components caused by the modulation. In a digital modulator the PWM pulse does not represent the mean-value of the continuous input signal, but one sample value. This causes further distortions. Fig. 3.3 shows the spectrum of the audio base-band from PWM simulation. The leftmost line represents the original input tone, all other lines result from the non-linear process. UPWM adds more distortion in the output signal as compared to NPWM as evident in Fig. 3.4.

Fig. 3.3: PWM waveform frequency spectrum

3.3.1 Interpolation of Input Signal

To reduce the distortion introduced due to UPWM, interpolation techniques are used. Different samples are interpolated and the resultant signal is compared to the saw-tooth/triangle waveform to generate PWM. As shown in Fig. 3.4, the resultant value is closer to NPWM. Generally higher the order of the interpolation, lesser distortion would result. But higher-order interpolation adds delay in the system which leads to instability of the loop. PWM interpolation techniques can be applied to both analog with zero-order hold and PCM to PWM generation [13, 14].

Fig. 3.4: Uniform, Natural and Interpolated sampling PWM Generation

Fig. 3.5 shows the simulation results of Analog PWM and Digital PWM generation.

Fig. 3.5: Analog and Digital PWM Conversion

The SNR for Analog PWM is 59dB and for Digital PWM is 52dB.

From simulation results shown in Fig. 3.5, it follows that PWM signal has harmonic distortion at $nf_o, n > 1$ and f_o is the fundamental frequency. Digital PWM is more distorted than analog PWM and hence has lower SNR.

Fig. 3.6 shows the comparison between the zero order and the first-order interpolation techniques. As mentioned earlier there is a significant improvement due to interpolation.

Fig. 3.6: Comparison of first and zero-order sampling hold

The SNR with first-order interpolation of input signal is found to be 64dB.

3.4 Pulse Group Modulation

In Pulse Group Modulation (PGM), to reduce the PRF of the SDM bit stream and in order to force it to be a constant, samples with the same sign are grouped together [17]. This results in reduction of transitions after the sample and hold. The output is divided into frames of length N and the samples in each frame are relocated so that all the 1's occur in a single group. The group size is given by:

$$S(pN) = \sum_{n=0}^{N-1} v(pN - n). \quad (3.2)$$

where $v(n)$ is the output samples of the SDM and p is the group number.

If there is a sequence $v(n)$ of 1-bit data from the SDM output, consisting of zeros and ones. The sum of the present sample and previous $N-1$ samples at any instant is represented by,

$$y(n) = \sum_{k=0}^{N-1} v(n - k). \quad (3.3)$$

In z -domain,

$$Y(z) = M(z)V(z) = \sum_{k=0}^{N-1} V(z)z^{-k} = V(z) \left(\frac{1 - z^{-N}}{1 - z^{-1}} \right) \quad (3.3)$$

where,

$$M(z) = \frac{1 - z^{-N}}{1 - z^{-1}}. \quad (3.4)$$

So the summation is equal to the moving average filter of length N . Every N th sample of the summation corresponds to the sum of the samples constituting the group. The operation of taking every N th sample and discarding the remaining samples is termed as

decimation. The formation of the pulse group from the uniformly sampled PWM waveform, involves an increase in the sampling rate by a factor of N. The decimation produces aliasing and the PWM introduces harmonic distortion, carrier and sideband tones and inter-modulation distortion noise.

3.4.1 PCM Grouping versus PWM Grouping

For conversion from PCM to PWM, PCM input is grouped together but it distorts/modulates the input PCM signal and the original signal cannot be reconstructed. The scheme implemented here, groups PWM output instead of PCM and thus the signal is not modulated. Let 3 samples of input PCM signal be 0001, 0010, 0011. These binary numbers corresponds to decimal numbers 0.0625, 0.1250 and 0.1875 respectively. Taking these three samples together and arranging 0's and 1's we have – Number of zeros = 8, Number of ones = 4. Hence PGM of PCM gives – 0000 0000 1111. These correspond to 0, 0, and 0.9375 respectively in decimal notation. Hence the original signal is distorted. PWM of this PGM will give erroneous results. However if the PCM signal is first converted to PWM, the result is given as,

$$0001 \Rightarrow 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad -1 \quad -1 \quad -1 \quad -1 \quad -1 \quad -1 \Rightarrow 10/16$$

$$0010 \Rightarrow 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad -1 \quad -1 \quad -1 \quad -1 \quad -1 \Rightarrow 11/16$$

$$0011 \Rightarrow 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad 1 \quad -1 \quad -1 \quad -1 \quad -1 \Rightarrow 12/16$$

Now grouping these PWM signals and arranging 1's and -1's we have,

$$(10 + 11 + 12)/16 \times 3 \text{ as output or } 33/48 = 11/16, \quad (3.5)$$

so effectively we are taking mean value of three samples and hence the original signal is not distorted and at the same time the sampling frequency of the input signal is reduced considerably.

The simulation results of PGM with samples 0001, 0010 and 0011 are shown in Fig. 3.7.

Fig. 3.7: PGM of PWM signal

3.4.2 Pulse Density Modulation and Pulse Width Modulation

In PDM, samples are represented with a frequency modulated square wave, with pulses of equal duration, whilst in PWM the duration of the pulses is modulated rather

than the frequency of the pulses. Hence, PDM is a frequency domain approach, while PWM is a time domain approach.

Consider a dc level signal that is 0.50 times of its maximum value V_m . Fourier representation of PWM signal is given by

$$y(t) = \frac{8}{16}V_m + V_m \sum_{n \neq 0} \frac{1}{n\pi} \sin\left(\frac{8}{16}n\pi\right) \exp\left(jn \frac{2\pi f_s}{16} t\right) \quad (3.6)$$

Its harmonic energy is contained at a frequency $\frac{f_s}{16}$. The Fourier series representation of the same dc level signal with PDM is

$$y(t) = \frac{1}{2}V_m + V_m \sum_{n \neq 0} \frac{1}{n\pi} \sin\left(\frac{1}{2}n\pi\right) \exp\left(jn \frac{2\pi f_s}{2} t\right) \quad (3.7)$$

It is evident from the equation (3.7) that dominant frequency harmonic is at $\frac{f_s}{2}$ which is much higher. An output reconstruction filter of higher order is required in the case of PWM signal as compared to PDM signal.

3.5 DC-to-DC Conversion

DC-to-dc conversion is a technique by which input dc voltage is converted to output dc voltage typically of different level. They are used for switched power regulation, noise level removal and motor drive applications. The basic operation of a dc-to-dc converter can be understood by using a step-down (buck) converter. Theoretically, this is for a resistive load. The average output voltage can be calculated in terms of the switch duty ratio [8] given as

$$V_o = \frac{1}{T_s} \int_0^{T_s} v_o(t) dt = \frac{1}{T_s} \left(\int_0^{t_{ON}} V_s dt + \int_{t_{ON}}^{t_s} 0 dt \right) = \frac{t_{ON}}{T_s} V_s = D V_s. \quad (3.8)$$

Fig. 3.8 shows the buck regulator with an ideal switch and Fig. 3.9 shows its output simulation results.

Fig. 3.8: Buck Regulator Operation

Fig. 3.9: Buck Regulator output for different duty cycles

3.5.1 Continuous and Discontinuous Conduction Mode

Continuous conduction mode [8] is the one in which inductor current flows continuously. When the switch is turned on as shown in Fig. 3.10, inductor voltage $v_L = V_s - V_o$ causes linear increase in the inductor current. When the switch is turned off, inductor voltage is $v_L = -V_o$, current across inductor keeps on flowing due to its stored energy.

Fig. 3.10: Continuous Conduction Mode Operation

Neglecting power losses and equating the input power P_s and the output power P_o , yields

$$V_s I_s = V_o I_o \text{ or } \frac{I_o}{I_d} = \frac{V_s}{V_o} = \frac{1}{D}. \quad (3.9)$$

Hence, in the continuous-conduction mode, the buck converter works as a transformer with varying turn ratio between 0-1. In the discontinuous-conduction mode on the other

hand, as shown in Fig. 3.11 the input voltage V_s may fluctuate but V_o is kept equal to the input voltage by adjusting the duty ratio.

Fig. 3.11: Discontinuous Conduction Mode Operation

During the interval $\delta_2 T_s$, where the inductor current is zero, the power to the load is entirely supplied by the filter capacitor. Inductor voltage during that time is zero. The output voltage is given by

$$\frac{V_o}{V_s} = \frac{D}{D + \delta_1}. \quad (3.10)$$

Hence, the output voltage which is relatively small depends upon both the on-time and the dead-time. The output voltage ripple can be obtained as

$$\frac{\Delta V_o}{V_o} = \frac{\pi^2}{2} (1-D) \left(\frac{f_c}{f_s} \right)^2 \quad (3.11)$$

where, f_c is the filter cut-off frequency and f_s is the switching frequency. Hence higher ratio of $\frac{f_c}{f_s}$ would result in lower ripple voltage for both continuous and discontinuous mode of operation.

3.6 H-Bridge

H-Bridge or full-bridge converter [8] is biased by fixed magnitude input voltage V_i . The output of the converter for a Class-D amplifier is an amplified dc voltage, whose polarity and magnitude depends upon the duty ratio. Magnitude and direction of the output current depends on the load. An H-bridge converter consists of two legs as shown in Fig. 3.12. Each leg consists of two switches and they switch in such a way that when one pair is in the on state the other pair remains off. Hence they are never off or on at the same time. In practice, there is always a dead time or blanking time, when both legs are off for certain time period and the operation is discontinuous. In this mode both switches are off and there is only one dominant pole in the frequency response. Another advantage of the blanking time is it avoids short circuiting of the input bias voltage. Switches, which are essentially MOSFET transistors, are controlled by PWM or PDM signal. In general,

$$V_{1N} = V_s (\text{Duty Cycle of 1st arm})$$

Similarly,
$$V_{2N} = V_s (\text{Duty Cycle of 2nd arm})$$

Advantage of a H-Bridge is that it doesn't become discontinuous at the low values of I_o , unlike single-stage converters such as buck converter and half-bridge.

3.6.1 Output Filter Design

The high frequency high-low output signal from the H-Bridge is converted into amplified audio signal by passing it through an analog lowpass filter [8], [18]. Output Filters not only suppress high frequency components and increase efficiency but also reduce Electromagnetic Interference (EMI) produced by the fast operating output transistors. Usually, a balanced 2-pole filter is used to effectively reduce the EM radiations.

Transfer function of a Butterworth filter is given by

$$H(s) = \frac{\left(\frac{1}{LC}\right)}{s^2 + s\left(\frac{1}{RC}\right) + \left(\frac{1}{LC}\right)}. \quad (3.12)$$

If L and R are known, C can be computed as,

$$C = \frac{L}{4R^2\xi^2} \text{ where } \xi = 0.707 \text{ for Butterworth filter.}$$

Substituting, $L = 5\mu H$ and $R = 4\Omega$, we obtain $C = 0.110\mu F$

Fig.. 3.12 shows the H-Bridge implementation using ideal switches in PSPICE, and Fig. 3.13 shows the corresponding amplified output.

Fig. 3.12: H-Bridge with Feedback

Fig.. 3.13 shows the simulation results of H-Bridge

Fig. 3.13: Input and H-Bridge Output

CHAPTER IV

NON-IDEALITIES IN A CLASS-D AMPLIFIER

4.1 Clock Jitter

Jitter is a random variation of sampling instants. Clock generator phase noise and sampling circuit is the cause of jitter. The effect of jitter is independent of the order and the structure of SDM. Noise introduced by jitter can be assumed to be white, i.e., it is uniformly distributed between frequencies 0 to $f_s/2$. Jitter error can be reduced by over-sampling the input signal. The clock jitter value of a sampled signal is represented by

$$x_i'[t] = x_i[t] + \tau \{x_i[t+1] - x_i[t]\} f_s \quad (4.1)$$

where $x_i'[t]$ is the error due to jitter deviation of τ in sample value $x_i[t]$ with a true sampling frequency of f_s . Using Taylor's series expansion we have,

$$\tau \{x_i[t+1] - x_i[t]\} f_s \approx \tau \frac{d}{dt} x_i(t). \quad (4.2)$$

To model jitter, τ is generated using a random noise generator [19]. Fig. 4.1 shows the SIMULINK model of the clock jitter noise.

Fig. 4.1: Clock Jitter Model

4.2 Integrator's Noise

4.2.1 Thermal Noise

In switched capacitor (SC) implementation of an integrator shown in Fig. 4.2 [3], there is always some finite resistance associated with a switch and this generates thermal noise. This resistance is the source of the thermal energy which leads to random fluctuation of carriers. Input signal, when superimposed to the switch's thermal energy $n_T(t)$, is given by

$$x'[t] = \{ x[t] + n_T[t] \} b = \{ x[t] + \sqrt{\frac{kT}{bC_f}} n(t) \} b \quad (4.3)$$

where b is the integrator's gain, C_f is the integrator's feedback capacitor and $n(t)$ is uniformly generated random number signifying the random motion of carriers in semiconductor.

Fig. 4.2: Switched Capacitor implementation of Integrator

4.2.2 Op-Amp Noise

Flicker Noise, wide-band thermal noise and dc offset contribute to op-amp noise. Flicker noise in the drain current is produced when charge carriers move at the interface between gate oxide and the silicon substrate in a MOSFET; some are randomly trapped and are released by high-energy states (generated due to dangling bonds at the end of interface) latter on. Fig. 4.3 shows the model used to simulate the effect of the flicker noise [19].

Fig. 4.3: Op-amp Noise SIMULINK Model

4.2.3 Integrator's Leakage

Ideally, the dc gain of the integrator is infinite. In practice, however, previous integrator's output does not completely add to the current input sample due to circuit constraints. Transfer function of the integrator with leakage is represented as

$$H(z) = \frac{1}{z - \alpha} = \frac{z^{-1}}{1 - \alpha z^{-1}}, \quad (4.4)$$

where α is the leakage factor. Hence, dc gain of the integrator is given by

$$H(0) = \frac{1}{1 - \alpha}. \quad (4.5)$$

4.2.4 Integrator's Saturation

The voltage swing of an op-amp is taken into account for modeling of an ideal integrator. Fig. 4.4 shows SIMULINK model [19] of an integrator with the op-amp noise, leakage, and saturation

Fig. 4.4: Practical Integrator Model

4.3 Third-order (1-1-1) MASH SDM with Non-Idealities

Fig. 4.5 shows the simulation results of the third order MASH shown in Fig. 2.12 with non-idealities such as jitter, op-amp noise, integrator's leakage and saturation and its comparison with an ideal SDM structure. The output signal is passed through the lowpass filter described in Chapter 2.

Fig. 4.5: Ideal and Non-ideal PSD of SDM in analog system

4.3.1 Digital Domain SDM

In digital domain, digital counter acts as an integrator, and hence it suffers from digital clock jitter and saturation. Comparison of results of the second-order ideal and non-ideal SDM simulation in digital system is shown in Fig. 4.6. The noise floor is higher in non-ideal case in comparison to the ideal one.

Fig. 4.6: Ideal and Non-ideal SDM in Digital Domain

4.4 H-Bridge Non-Idealities

The major problem with the H-Bridge is the power supply ripple. Percentage of ripple in supply depends upon its source. In addition to ripple there's delay in the signal due to power MOSFETS. Although the SDM/PCM-to-PWM conversion stage has more transistors in comparison to the H-Bridge implementation, SDM operates at much higher frequency as compared to the power output stage. Hence structures involving feedback at

the output stage have much greater impact on the output signal. Discontinuous mode of operation also introduces non-linearity as discussed in Chapter 3.

In general there are three main sources of noise associated with output stage [24]:

- Jitter noise is produced due to imprecision in commutation instant time by clock.
- The asymmetry between the edges of a pulse produces noise. Further more distortion due to the fact that the PDM is pseudo-correlated to the input signal is generated.

Both of these problems are associated with the frequency and noise introduced is proportional to the switching frequency of the H-bridge. This distortion reduces the dynamic range of the signal.

- The noise is generated due to ripple in the supply voltage. Characteristic of this noise depends upon the power supply generator.

Fig. 4.7 shows the model of these noises at the output stage.

Fig. 4.7: Non-ideal H-Bridge Model in SIMULINK

CHAPTER V

CLASS-D AMPLIFIER STRUCTURE

5.1 Basic Architecture

A Class-D amplifier essentially consists of two parts: signal pre-processing stage and power driving stage. In the pre-processing stage 16-bit digital input signal is converted into over-sampled PWM or PDM signal using digital processing techniques. Power Stage consists of H-Bridge and its duty cycle is controlled by the PWM or PDM signal generated in the processing stage. The amplified analog audio signal is obtained after passing the output of the H-bridge through an analog lowpass filter.

5.2 Class-D Amplifier without Feedback

Fig. 5.1: Class-D Amplifier with H-Bridge driven by PWM signal

PWM conversion is done in the pre-processing stage. It requires a sampling frequency of $44.1KHz * 2^{16} = 2.89GHz$ to convert a PCM into 1-bit PWM signal without losing information [14]. This high switching frequency would incur very high power loss which leads to reduction in the efficiency of the amplifier. Simulation has been done with switching frequency of $8.192MHz$. This is still very high with only 8 bits of PCM been taken. If $X(z)$ is the input signal, $E_{pwm}(z)$ the error or noise introduced by PWM conversion, $E_{h-bridge}(z)$ the noise introduced at full-bridge stage, then output $Y(z)$ is given by

$$Y(z) = X(z) + E_{pwm}(z) + E_{h-bridge}(z). \quad (5.1)$$

However, there would be some delay in the output due to both pre-processing and power output stages. Fig. 5.1 shows the Class-D amplifier with H-bridge driven by PWM waveform.

Table 5.1 shows the simulation parameters for Class-D Amplifier simulation.

Table 5.1 Class-D amplifier simulation parameters

Bandwidth	16 kHz
Input frequency	1 kHz
FFT points	2^{18}
Cut-off frequency of butter-worth filter f_c	16 kHz
Total Leakage factor	0.999
Saturation	± 1.5
Jitter	1ns
H-bridge ripple noise	5-10%
Op-amp and Thermal Noise	1%

Power Spectrum Density (PSD) of the output signal for PWM signal is shown in Fig. 5.2.

Fig. 5.2: PSD of Class-D with H-Bridge driven by PWM input

To reduce the switching frequency, a 1-bit SDM is used and output PDM signal is generated based upon the input audio signal. The H-Bridge is driven by PDM output signal [14, 15]. Switching frequency is considerably reduced in this method at the expense of linearity of the signal as evident from Fig. 5.3. Output in this case is given by

$$Y(z) = X(z) + (1 - z^{-1})^2 E_{sdm}(z) + E_{h-bridge}(z). \quad (5.2)$$

Fig. 5.3: PSD of the output with H-Bridge driven by SDM

There is an additional second-order noise shaping of the quantization error and hence the over-sampling ratio can be reduced considerably.

In the hybrid structure [17], SDM is used to reduce the number of bits from 16-bits to 5-bits and eventually the 5-bit signal is converted to a PWM waveform. Hence this structure gives a better SNR as compared to the pure 1-bit SDM signal. Fig. 5.4 shows the SIMULINK model, and Fig. 5.5 shows the simulation results of the hybrid structure Class-D amplifier without feedback. Transfer function for hybrid architecture is given as,

$$Y(z) = X(z) + (1 - z^{-1})^2 E_{sdm}(z) + E_{pwm}(z) + E_{h-bridge}(z). \quad (5.3)$$

Fig. 5.4: SIMULINK Model for the Hybrid Structure

As compared to the Class-D structure using SDM with the second-order noise shaping, the magnitude of the quantization and PWM distortion of the hybrid structure is less.

Fig. 5.5: PSD of the output for Hybrid Structure

Table 5.2 summarizes the results of the different schemes of Class-D Amplifiers without feedback.

Table 5.2 Comparison of class-D architectures without feedback

	Pulse Width Modulation	1-bit SDM	Hybrid – SDM and PWM Conversion
FFT points N_p	2^{18}	2^{18}	2^{18}
Fundamental Frequency f_{in}	1000	1000	1000
Bandwidth BW	16000	16000	16000
Over-sampling Ratio OSR	256	64	128
Signal-to-Noise Ratio $SNR(dB)$	30.74	39.22	38.45
Dynamic Range $DR(dB)$	53.55	46.02	53.33
Efficiency η	Low	Moderate	Moderate

5.3 Class-D Amplifier with Feedback

To increase linearity and Power Supply Rejection Ratio (PSRR) audio output is fed back to the input [15]. This requires very high resolution ADC in the feedback loop. Usually a SD-ADC is used owing to its high resolution and SNR. If the second-order SD-

ADC is used in the feedback and $E_{sdmfb}(z)$ is the quantization noise of the feedback path, output is given by

$$Y(z) \approx X(z) + E_{sdm}(z) + (1 - z^{-1})^2 E_{pwm}(z) + (1 - z^{-1})^2 E_{h-bridge}(z) + (1 - z^{-1})^2 E_{sdmfb}(z). \quad (5.4)$$

It is clear from the above expression that quantization noise in the forward path of the SDM is canceled out. Fig. 5.6 shows the SIMULINK model, and the output PSD is shown in Fig. 5.7.

Fig. 5.6: SIMULINK Model for the Class-D Amplifier with feedback using ADC

Fig. 5.7: PSD of the output with feedback using ADC

5.3.1 Analog Feedback Architecture

As mentioned in the previous section, feedback structures require high resolution ADC in the feedback path which increases the size of the chip. To circumvent this problem, pre-processing and power conversion is done in both – digital and analog domains. As shown in Fig. 5.8, SDM and PWM conversion are done in digital domain. A 1-bit PWM signal is converted in analog signal using 1-bit DAC which is essentially a switch, and fed to the closed loop H-bridge in the analog domain. Different types of analog feedback control schemes can be employed [16, 25].

Fig. 5.8: Class-D Amplifier with analog domain feedback scheme

It is evident from the results that this type of topology produces high SNR and efficiency. Comparator and loop filter is clock free at the output analog stage, which makes the output power stage free from the jitter noise. However, if the amplitude of the noise in the feedback is too high, it will generate a steep slope at the integrator's output leading to instability of the H-Bridge. To circumvent this problem the slope of integrator is limited and hence for large errors it saturates, which leads to non-linearity and distortion of the signal. Fig. 5.9 shows the SIMULINK model of the output power stage with the second- order CT SDM and the PSD of output is shown in Fig. 5.10

Fig. 5.9: SIMULINK Model for Class-D Amplifier with feedback in analog domain

Fig. 5.10: PSD of the output with feedback in the analog domain

Table 5.3 summarizes the result for feedback structures both for hybrid scheme and loop filter scheme. Although the switching frequency is smaller for the analog structure its SNR is lower owing to the analog circuitry.

Table 5.3 Comparison of class-D amplifiers with feedback

	PWM and SDM with Feedback	SDM with Analog Filter
FFT points N_p	2^{18}	2^{18}
Fundamental Frequency f_{in}	1000	1000
Bandwidth BW	16000	16000
Over-sampling Ratio OSR	128	32
Signal-to-Noise Ratio $SNR(dB)$	47.66	43.5
Dynamic Range $DR(dB)$	56.4	51.2
Efficiency η	Moderate	High

CHAPTER VI

PROPOSED ARCHITECTURE

Different architectures are proposed for improving the efficiency of Class-D amplifiers achieved by reducing the switching frequency at the output stage. The behavioral simulation results in MATLAB/ SIMULINK are also provided.

6.1 Modified SDM with Feedback

Improvement on the structure mentioned in Chapter 5, Fig. 5.11 can be done by including the H-Bridge as a part of the forward path of the SDM loop as shown in Fig. 6.1. This architecture provides a second-order shaping of the noise generated of the SDM in the forward path, the PWM conversion, the H-bridge (including power supply ripple) and the SD-ADC in the feedback path.

Fig. 6.8: SIMULINK model for modified Hybrid Structure with SD-ADC in the feedback

The output can be obtained as

$$Y(z) \approx X(z) + (1 - z^{-1})^2 E_{sdm}(z) + (1 - z^{-1})^2 E_{pwm}(z) + (1 - z^{-1})^2 E_{h-bridge}(z) + (1 - z^{-1})^2 E_{sdmfb}(z) \quad (6.1)$$

where $Y(z)$ is the output signal, $E_{sdm}(z)$ represents the noise introduced by the second-order modulator, $E_{pwm}(z)$ is the noise introduced by pulse width modulation, $E_{h-bridge}(z)$ denotes the ripple noise introduced at H-Bridge and $E_{sdmfb}(z)$ is the quantization noise introduced due to high resolution SD-ADC in the feedback.

Fig. 6.2 shows the PSD of the output of the modified hybrid structure with sigma-delta ADC in the feedback.

Fig. 6.2: PSD of the output for modified hybrid structure

6.2 Class-D Amplifier with Cascaded SDM

The proposed structure consists of a cascade of sigma-delta modulators in the digital domain with an intermediate decimation-filter which filters out the quantization noise generated by the first stage. The first modulator truncates a 16 bit input to a 5 bit signal with an OSR of 32 and a sampling frequency of $44.1 * 32$ KHz. This signal is fed to the decimation-filter which down-samples the signal by the factor of 16. The decimation-filter described in [9] is used here. It consists of three FIR filters and two down-samplers as shown in Fig. 6.4

Fig. 6.3: Proposed architecture using cascaded SDM

A 12-bit output from the decimation-filter is passed to the second stage SDM which quantizes it to a 1-bit signal. The H-Bridge is made part of the SDM loop which shapes the distortion at the output power stage as shown in Fig. 6.3

Fig. 6.4: A decimation filter

Since the ideal output signal of the H-bridge is of 1-bit, it can be fed back directly to the input without requiring a high resolution ADC. The 12-bit output of the first-stage SDM with a frequency of $32f_s$ is given as

$$Y_1(z) = z^{-3}X(z) + (1 - z^{-1})^3 N_{3q}(z) + N_{df}(z) \quad (6.2)$$

where $Y_1(z)$ is the output of the first stage, $N_{3q}(z)$ represents the noise introduced by the third stage of the 1-1-1 MASH and $N_{df}(z)$ is the noise introduced by the decimation filter.

The analog output is given by

$$Y(z) = z^{-1}Y_1(z) + (1 - z^{-1})^2 N_{2q}(z) + E_r(z) \quad (6.3)$$

where $Y(z)$ is the analog output, $N_{2q}(z)$ represents the quantization and jitter noise introduced by the second-order modulator and $E_r(z)$ denotes the high frequency ripple noise.

Table 6.1 shows the simulation parameters for the proposed structure of Class-D amplifier

Table 6.1 Simulation parameters for proposed structures

Bandwidth	16 kHz
Input frequency	1 kHz
FFT points	2^{18}
Cut-off frequency of butter-worth filter f_c	16 kHz
Total Leakage factor	0.999
Saturation	± 1.5
Jitter	1ns
H-bridge ripple noise	5-10%
Op-amp and Thermal Noise	1%

Fig. 6.5 shows that there is not much degradation in the quality of the input signal by using a third-order noise shaper at sampling frequency of 1.411MHz and reducing the original signal to a 5-bit signal.

Fig. 6.59: PSD of the output of the first stage SDM

However, as mentioned earlier due to the non-idealities at output stage, noise/errors are introduced in the system.

- **Timing Delay Noise:** Noise introduced due to delay is fed back to the SDM input and can be shaped. This timing delay noise has a frequency between 0 to $f_s/2$. Higher frequency delay errors are taken care of by the second-order analog lowpass filter and speaker.
- **Power Supply Noise:** As shown in Fig. 6.5, a 1-bit ADC cannot detect power supply ripple till the absolute value of the error reaches $V_{\max}/2$.

The output of the H-Bridge with 1-bit ADC is shown in Fig. 6.6

Fig. 6.6: PSD of the output with 1-bit A/D Feedback

Although the design is relatively simple, compact and easy to implement, it can only correct the quantization and jitter-delay noise (in the range of 0 to $f_s/2$). This produces distortion at the output which leads to the increase in the Total Harmonic Distortion (THD) of the signal.

Fig. 6.7: H-Bridge Output signal waveform

6.3 Class-D Amplifier with Cascaded SDM and SD-ADC Feedback

Linearity of the signal can be improved, by increasing the sampling frequency of the second-stage modulator to $256f_s$ and by inserting the second-order SD-ADC in the feedback path as shown in Fig. 6.8. The output PDM signal of the SDM is grouped using the Pulse Group Modulation (PGM) technique [13], in which 0's and 1's are clubbed together resulting in the reduction of the switching frequency at the output power stage (H-Bridge) to 705.6 KHz. A 4-bit SD-ADC is connected in the feedback loop, to quantize the high-frequency ripple and noise generated at the output stage. When the current is delivered to the load, power supply voltage drops and this decreases the signal amplitude at the output. Output signal is just an amplified form of input PDM signal. Negative feedback signal increases the amplitude of input PDM and corrects errors. SD-ADC also reduces the overall

time delay of the system and improves ripple rejection. If the second stage is operating at V_{ref} process, the SD-ADC operates at: $V_{ref}/8$, and it will take care of minimum ripple noise of 1.5% and maximum of 11%.

Fig. 6.8: Proposed Class-D Architecture using Cascaded SDM and feedback loop

Of 10 feedback bits, the first four bits are 0xF or 0x0, the last three bits are 0x7 or 0x0, and the central three bits are the output of SD-ADC as shown in Fig. 6.9. These bits subsequently correct the input depending upon the quantization, ripple and delay noise.

Fig. 6.9: 10-bit Feedback Arrangement

Transfer function of the second-stage with the H-Bridge switching at $256f_s$ is given as

$$Y(z) = (z^{-M})Y_1(z) + (1 - z^{-1})^2 N_{2q}(z) + N_{pgm}(z) + (1 - z^{-1})^2 E_r(z) + (1 - z^{-1})^2 E_f(z) \quad (6.3)$$

where $Y_1(z)$ is the output signal, $N_{2q}(z)$ denotes the quantization noise introduced by the second-order modulator, $N_{pgm}(z)$ represents the noise introduced by pulse group modulation, $E_r(z)$ is the ripple noise introduced at H-Bridge, $E_f(z)$ denotes the quantization noise introduced due to SD-ADC in the feedback and M is the number of groups (for $OSR = 256f_s$, $M = 32$).

To ascertain stability of the system, delay of M samples is introduced at the quantizer output stage to compensate for the forward path delay due to PGM processing. Fig. 6.10 shows the output with 4-bit SD-ADC in the feedback. High frequency tones are attributed due to the over-sampling of signal at the second stage of the amplifier, which brings high switching frequency tones of 1.411 MHz at 60~70 kHz.

Fig. 6.10: PSD of the H-Bridge output with SD-ADC feedback

Table 6.2 summarizes the results obtained from all the proposed structures

Table 6.2 Comparison of proposed structures of class-D amplifier

	Modified Hybrid Feedback	Cascaded SDM with 1-bit ADC Feedback	Cascaded SDM with SD ADC Feedback
FFT points N_p	2^{18}	2^{18}	2^{18}
Fundamental Frequency f_{in}	1000	2000	2000
Bandwidth BW	16000	16000	16000
Over-sampling Ratio OSR	32	16	16
Switching Frequency (kHz)	1411.2	705.6	705.6
Signal-to-Noise Ratio $SNR(dB)$	58.2	51.24	71.1
Total Harmonic Distortion $THD(dB)$	-67.5	-61	-80.8
Efficiency η	Moderate	High	High

CHAPTER VII

HARDWARE REALIZATION

Primary objective of the board level implementation is to verify the functionality of the proposed structure of the Class-D amplifier. For simplicity the implementation is divided in two parts – the preprocessing stage and the output power stage. The processing stage is done by using TI DSP- TMS320C6211, a floating point processor and the output power stage is realized by using a digital audio board, which consists of an H-Bridge driven by Motorola microcontroller - 68HC12.

7.1 Preprocessing Implementation

Fig. 7.1 shows the block diagram of the pre-processing stage implemented in DSP.

Fig. 7.1: Preprocessing Implementation on TMS320C6211

The third-order SDM, the decimation filter and the second order SDM are implemented using Q15 format in C/C++. A 1-bit output of the second stage is decimated and converted into a digital output by passing it through the FIR filter. This FIR filter is

not part of the design but is included here only for converting the 1-bit output in a multi-bit signal. The sample program incorporating DSP/BIOS application from [27] is been used and the Class-D amplifier routine is invoked through the sample application. The application is a non-BIOS program that uses the Codec, Multi-Channel Buffered Serial Port (McBSP) and Direct Memory Access (DMA) to continuously process digitized audio data. The overall signal flow diagram is shown in Fig. 7.2.

Fig. 7.2: Signal flow diagram in DSP module

The pre-processing routine including the FIR filter is executed after data is received from the ping-pong receive buffers and the FIR filter output is transmitted to the ping-pong transmit buffer. The reference program consists of codec, McBSP, DMA ping-pong buffers and FIR filter routines. Fixed point routines for addition, subtraction, multiplication and division are written to prevent registers from overflowing. Fig. 7.3 shows the PSD of the digital output with a sinusoidal input of a frequency of 2 kHz. Filter

coefficients used are the same as that for simulation in Chapter 6 and are designed using SIMULINK. Since there is no H-Bridge at the output stage, the SNR of the output signal is around 12-15dB higher than the real value.

Fig. 7.3: PSD of the output

7.2 Power Stage Implementation

The power stage implementation is done to analyze the performance of the amplifier with PDM as the driving signal. Fig. 7.4 shows the output stage realization with a first-order, 1-bit SDM. Motorola 68HC12 processor is used for the PDM generation. The processor runs at a speed of 24MHz. The SDM is implemented in Motorola assembly language. The switching frequency of the H-Bridge is 40 kHz.

Fig. 7.4: Output stage implementation on 68HC12

The schematics of the audio daughter board are shown in Fig. 7.5 and Fig. 7.6. As shown in the schematic diagram, the DIR pin of the LMD18200 is connected to the PDM signal and the PWM pin is connected to logic High [28]. PDM output signal is generated in the processor by the SDM routine.

Fig. 7.5: Digital Audio Schemtaic – Regulator and HC12

Fig. 7.6: Digital Audio Schematic – Level Shifter and LMD18200

Fig. 7.7 shows the digital audio board and Fig. 7.8 shows the waveforms of the measurement. Input signal has amplitude of 2V p-p and a frequency of 1 kHz. The top waveform shows the output current through a 10 Ω resistor, giving an output voltage of 3V p-p. The PDM output signal is also shown. There is a delay in the output current, which is attributed to the inductive filter.

Fig. 7.7: Audio Daughter Board

Fig. 7.8: Output waveform

CHAPTER VIII

CONCLUSIONS AND FUTURE WORK

In Class-D amplifiers, high quality digital-to-analog conversion can be achieved by applying digital signal processing (DSP) techniques to generate PWM and PDM signal. DSP is capable of noise shaping and distortion elimination such that quality is governed only by circuit design and construction techniques. The distortion produced by the power supply ripple can be reduced by using negative feedback. Edge timing and clock jitters are concerned for very high fidelity applications. The edge timing jitter is significantly reduced by feedback and output analog filter. The clock jitter however is so small, that it is very difficult to eliminate. To reduce the size of the jitter, re-synchronization or clock recovery circuitry running at a very high clock frequency is required [24].

A high quality Class-D amplifier using cascaded SDM and feedback loop has been proposed, in which all the signals are processed in the digital domain. The pulse group modulation technique reduces the output switching frequency to 705 kHz. The high frequency noise using due to switching and power supply is properly shaped by using 4-bit SD-ADC in the feedback which produce high quality digital signal with reduced Electromagnetic Interference (EMI) without requiring very high precision dc power source, very high speed clock and fast switched MOSFETs. Simulation conducted in SIMULINK verifies the result of the proposed structure.

At the output stage PGM introduces non-linearity in the output signal. If PGM can be included as a part of the output feedback loop, this non-linearity can be reduced. Further improvement in the performance can be achieved by doing feedback, both in the analog and digital domains.

Multi-level converter structure can be implemented in which the output load can be shared among two H-Bridges of smaller size. The current ripple in the output signal can be reduced by realizing the unipolar switching technique [8].

A clock recovery circuit can be used as a part of the main circuitry or as a separate circuit to correct jitter error.

Finally, complete board level implementation of the design can only be done by using TMS320C6211 DSP which runs at 150-200MHz as opposed to 68HC12 which runs only at 24MHz. This speed will enable implementation of complex digital filters and higher order SDM in the software.

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