DESIGN OF A 30 kV POWER SUPPLY
FOR RAPID CAPACITOR CHARGING

by

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ABSTRACT

This thesis describes the design and construction of a compact power supply designed to charge a $6.6\ \mu\text{F}$ capacitor to 30 kV in 40 ms from a thermal battery. The thermal battery has an output of 500 Vdc which is stepped up to 30 kV DC through the use of a micro-controlled H-Bridge and a custom built step-up transformer. The H-Bridge is used to convert the DC into AC which the transformer steps up to 30 kV. A rectifier is then used to convert the AC output of the transformer into DC used to charge the $6.6\ \mu\text{F}$ load capacitor. The load capacitor will eventually drive a pulsed microwave emitter.

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NOMENCLATURE

A = Amps (Current)

Bank = Grouping of components

Blanking Time = The time that opposing legs are off to avoid shorting of the bus

°C = Celsius (Temperature)

C_1 = Input capacitors

C_2 = Load capacitors

cm = Centimeter ($\times 10^{-2}$ m)

cm^3 = Cubic centimeters

CPU = Central processing unit

C_{SB} = Capacitance of snubbers

Ctl- = Gate control on IGBT's 1 & 4

Ctl+ = Gate control on IGBT's 2 & 3

C_{XrX} = Capacitor in diode string from output rectifier

D = Duty cycle

D_{1i} = IGBT freewheeling diode

D_{1r} = Diode module in output rectifier

D_{1v} = Diode in input rectifier

D_{2i} = IGBT freewheeling diode

D_{2r} = Diode module in output rectifier

D_{2v} = Diode in input rectifier

D_{3i} = IGBT freewheeling diode

D_{3r} = Diode module in output rectifier

D_{3v} = Diode in input rectifier

D_{4i} = IGBT freewheeling diode

D_{4r} = Diode module in output rectifier

D_{4v} = Diode in input rectifier

D_{5v} = Diode in input rectifier

D_{6v} = Diode in input rectifier

D_i = Initial duty cycle

DS = Decimal

Dump = Discharge

D_{XrX} = Diode in diode string from output rectifier

EEPROM = Electrical Erasable Programmable Read Only Memory

F = Farad (Capacitance)

Free wheeling diode = A diode that provides a continuous current path for inductors when an adjacent switch is turned off to reduce transient voltage spikes

f_{smax} = Maximum switching frequency

G = Giga ($\times 10^9$)

H = Henry (Inductance)

Half Bridge = One leg of an H-Bridge

HC12 = Motorola micro-controller

Hex = Hexadecimal

Hz = Hertz

H-Bridge = 4 switches arranged in an H configuration

I = Current (Amps)

IGBT = Isolated Gate Bipolar Transistor

I_C = Continuous collector current

I_{FAV} = Mean forward current

I_{FSM} = Surge forward current

I_{FRMS} = RMS forward current

I_I = Input current
 I_O = Load current
 I_{RMS} = Alternating output current
 J = Joule (VA)
 J/cm^3 = Energy density
 k = Kilo ($\times 10^3$)
 L_1 = Primary inductance
 L_2 = Secondary inductance
LED = Light Emitting Diode
 L_S = Stray inductance
 M = Mega ($\times 10^6$)
 m = Milli ($\times 10^{-3}$)
 mm = Millimeter ($\times 10^{-3}$ m)
MOV = Metal Oxide Varistor
 ms = milliseconds ($\times 10^{-3}$ s)
 n = Nano ($\times 10^{-9}$)
PWM = Pulse Width Modulation
P-P = Point to Point
 R = Resistance (Ohms)
RAM = Random Access Memory
 R_B = Battery resistance
 R_{d1} = Load capacitor dump resistor
 R_{d2} = Input capacitor dump resistor
 R_{d3} = Charging resistor
RLC = Resistor, inductor, capacitor circuit
RMS = Root mean squared

R_{Prim} = Resistance on primary of transformer

R_{Sa} = Input capacitor center post resistor a

R_{Sb} = Input capacitor center post resistor b

R_{Sc} = Input capacitor center post resistor c

R_{Sd} = Input capacitor center post resistor d

R_{Sec} = Resistance on secondary of transformer

R_{thjc} = Thermal resistance junction to case

R_{va} = Input capacitor midpoint resistor a

R_{vb} = Input capacitor midpoint resistor b

R_{XrX} = Resistor in diode string from output rectifier

s = second

sec = seconds

S_1 = Dump switch for load capacitors

S_2 = Dump switch for input capacitors

S_3 = Dump switch for charge resistor

Sa = Samples (data points)

SKiiPPACK® = SK (Semikron) Integrated Intelligent Power Pack

Snubber = A device used to reduce oscillations.

Stray Inductance = Undesirable inductance between circuit components

t = time (seconds)

T_{case} = Case temperature

t_{on} = Time signal is on (seconds)

T_{S} = Total time allotted for signal (seconds)

T_{vj} = Case temperature virtual junction temperature

Throttle = Initial duty cycle

τ = Time constant

V = Voltage (Volts)

V_{ac} = AC voltage

Varistor = Variable resistor

V_B = Battery voltage

V_{BB} = Bus bar voltage

V_{Cap} = Voltage of the input capacitors

V_{CC} = Collector-emitter supply voltage

V_{CES} = Collector-emitter (direct) voltage with base (gate) emitter short-circuited

V_B = Battery voltage

V_{BB} = Bus bar voltage

V_{Cap} = Voltage of the input capacitors

V_{dc} = DC voltage

V_{dc} = Voltage on the DC bus

V_I = Input voltage

V_{isol} = Isolation voltage

V_{Logic} = Voltage recommended to drive logic

V_{LL} = Line to Line voltage (3-Phase)

V_O = Output voltage

V_{RRM} = Repetitive peak reverse voltage

V_S = Source voltage

V_T = Transient voltage (Parasitic voltage)

Waistline = Waveform envelope

Y/X = Dip switch setting

@ = at

μ = Micro ($\times 10^{-6}$)

Ω = Ohms (Resistance)

π = pi (3.14...)

CHAPTER 1

INTRODUCTION

The purpose of this experiment is to design a power supply that is able to take the 500 volts output of a thermal battery and charge a 6.66 μF capacitor bank to 30 kV (3 kJ) in 40 ms. The capacitor bank will eventually be used to drive a pulsed microwave source. The power supply has to be able to charge the capacitor bank several times in the span of a few minutes. The 500 Vdc input needs to be stepped up to 30 kV DC output to charge the load capacitor bank. The problem is that DC is not as easy to step up as AC. In fact DC to DC boost converters are usually limited to a step-up ratio smaller than ten. The voltage level of AC can be changed with a transformer through the fact that the primary and secondary windings are coupled through the changing magnetic field. The solution to the problem is to turn the DC into AC, step it up with a transformer and then turn it back into DC. The DC is converted into AC through the use of an H-Bridge switching at 10 kHz. The output of the H-Bridge is AC which can be stepped up in the transformer. After the transformer steps up the voltage, a single phase rectifier turns the AC into DC that is used to charge the load capacitor. For testing purposes the thermal battery is replaced with a 480 V, 3-phase, 70 amp Variac stack (Y-Y auto transformer). The output of the Variac stack is converted to DC through the use of a full wave 3-phase rectifier. The capacitance of the load capacitor bank was 7.4 μF , which was slightly higher than the 6.6 μF load the project required.

CHAPTER 2

IGBT

The heart of the charging system is 4 Semikron 1242 GB120-407CTV SKiiPPACK® Dual-IGBT modules shown in Table 2.1 and Figure 2.1. The Semikron IGBT's are very robust in that each can carry 1200A @ 1200 V. The IGBT's are arranged in a standard H-bridge configuration. An H-Bridge consists of two half bridges, A and B, Each half bridge consists of two switches (IGBT's) and their anti parallel diodes. The two switches (IGBT's) in each half bridge are switched in such a way that when one of the switches is in its off state, the other switch is on. Therefore, both switches (IGBT's) in the same half bridge are never on simultaneously as this would lead to a short [Mohan 1995]. In practice both switches (IGBT's) are off for short intervals known as the blanking time. Blanking time is required so that both switches in the same half bridge can not accidentally be on at the same time which would short the DC inputs. The IGBT's are switched in opposing legs allowing the DC voltage at the input to be converted to AC at the output of the H-Bridge, as shown in Figure 2.2. Each SKiiPPACK® is half of an H-Bridge with IGBT 's 1 & 2 being controlled by one SKiiPPACK® and IGBT's 3 & 4 being controlled by the other SKiiPPACK®, as shown in Figures 2.2 and 2.3. To increase the current carrying ability of the H-Bridge, a second H-Bridge was added to form parallel H-Bridges. "The H-Bridges can be driven in parallel since the IGBT's exhibit a positive temperature coefficient of the forward voltage drop, which assists in current sharing between two parallel modules"[Giesselmann p.2]. The SKiiPPACK® modules all came with matched "(forward) voltage group" ratings, which indicates that the

half bridge modules will equally share current when they are connected in parallel.

Table 2.1 IGBT Parameters

Semikron SKiiPPACK (IGBT Module)	
Type	SKiiPPACK
Model	1242 GB120-407CTV
Topology	halfbridge
V_{CES}	1200 V
V_{CC}	900 V
I_C	1200 A
I_{RMS}	580 A
V_{Logic}	18 V
f_{smax}	14 kHz
V_{isol} (1min)	3000 V
Operating Temperature	-25...+85 °C

Figure 2.1 Semikron 1242 GB120-407CTV SKiiPPACK® IGBT's

Figure 2.2 Circuit Diagram Highlighting the Location of the H-Bridge

Figure 2.3 Circuit Showing Half Bridges A and B

The Semikron IGBT's came with large heat sink fins designed to keep them cool during continuous use. In an attempt to reduce the stray inductance (L_S) of the bus work and to improve the compactness of the design the heat sinks were removed. The heat sinks were not needed since the IGBT's are on for only 40 ms and the thermal characteristics of the aluminum would not allow heat to reach the cooling fins. With the removal of the heat sinks the overall size of the H-Bridge could be reduced by 60.5 cm from a height of 153 cm to 92.50 cm, as shown in Figure 2.4.

Figure 2.4 Removal of Aluminum Heat Sink

The next consideration that was taken in the design was the bus work connecting the terminals of the IGBT's. To keep the stray inductance (L_S) of the bus work down, the IGBT's were mounted back to back so that a simple U-channel bus with extended terminals could be used, as shown in Figures 2.5, 2.6, 2.7, 2.8 and 2.9. The positive and negative bus U-channels are located very close to each other (2.47 mm) to reduce the stray inductance (L_S) between the two channels. The channels were designed to fit inside of each other with a simple rubber insulator inserted between the conductors. Angular cuts were made in the custom aluminum bus bars in an attempt to keep the path between terminals as short as possible, as shown in Figure 2.5. Each bus bar has extended terminals to connect the respective terminals on the half bridge modules as seen in Figure 2.5, 2.6 and 2.7. Parallel half bridges are assembled back to back, as shown in Figure 2.5.

Figure 2.5 End View of Parallel Half Bridges with Bus Work

Figure 2.6 Side Picture of Parallel Half Bridges with Bus Work

Figure 2.7 Parallel Half Bridge Modules with Bus Work

Figure 2.8 Side Picture of Half Bridge Modules

Figure 2.9 Enlarged View of Bus Terminals

Snubbers ($0.47 \mu\text{F}$ capacitors) were used to reduce voltage transients during fast switching across the terminals of the IGBT's, as shown in Figure 2.10 and 2.11. When an IGBT is abruptly turned off, the energy trapped in the circuits' stray inductance (L_S) can cause damage to the IGBT if a snubber is not used to reduce the transient voltage (V_T) surges. The transient voltage (V_T) is determined by the stray inductance (L_S) and the rate at which the current is interrupted (di/dt) in addition to the voltage (V_{dc}) on the DC bus as in Eq. (2.1).

$$V_T = V_{dc} + L_S \left(\frac{di}{dt} \right) \quad (2.1)$$

The use of a snubber will change the transient voltage (V_T) to become

$$V_T = V_{dc} + I_0 \left(\frac{L_S}{C_{SB}} \right) \quad (2.2)$$

where I_0 is the load current before the IGBT is turned off and C_{SB} is the capacitance of the snubber [Sensitron]. The fact that the IGBT's are operating at 10 kHz and the large input current gives rise to some very

large transient voltages (V_T) even with small stray inductances (L_S). The use of snubber circuits offers some protection from these transient voltages (V_T). Measurements and analytical calculations determined that the value of the stray inductance (L_S) is on the order of 10 nH.

Figure 2.10 IGBT's with Snubbers Across the Terminals

Figure 2.11 IGBT with Snubbers Attached

Once the IGBT has been shut off, the input bus voltage oscillates as the free wheeling diodes conduct. The snubber is designed to reduce the effect of the voltage spike on the input bus. The effect of the snubbers on the bus work can be seen in Figures 2.12, 2.13 and 2.14. Figure 2.12

shows the bus voltage measured on the terminals of the snubbers connected to the IGBT's. The voltage oscillation across the snubbers shows the largest variation since they are designed to oscillate faster than the input capacitors. Figure 2.13 shows the bus voltage measured at the connection of the input capacitors to the bus work. Figure 2.14 shows the bus voltage measured from inside of the input capacitors. The input capacitors are too slow to oscillate at the frequency of the snubbers. All of the measurements are made on the same bus work at varying locations, which shows that location of measurements is important.

Figure 2.12 Bus Voltage Measured at Snubbers

Figure 2.13 Bus Voltage Measured at Terminals

Figure 2.14 Bus Voltage Measured at Input Capacitors

The operation of the H-Bridge can be described in 3 phases that are repeated for both opposing legs. In the first phase IGBT 2 and IGBT 3 are conducting. During this period current flows from the positive bus to the negative bus through the primary of the transformer, as shown in Figure 2.15. The second phase occurs when the IGBT's are shut off. The primary of the transformer continues to force the current to flow in the same direction. The diodes (free wheeling diodes) on IGBT's 1 and 4 conduct the current through the transformer primary from the negative bus to the positive bus which is shown by the voltage level reversing from phase 1, as shown in Figure 2.16. These diodes provide a continuous path for the load current when the opposing IGBT's are switched off. The ringing that is present on the voltage waveform is from the DC bus and the stray inductance (L_S). The third phase occurs when the IGBT's and the diodes are all shut off, as shown in Figure 2.17. The primary of the transformer starts to ring with the junction capacitance of the IGBT's in a RLC resonance. The process is repeated for the other opposing legs of the H-Bridge.

Figure 2.15 Phase 1 Current Path

Figure 2.16 Phase 2 Current Path

Figure 2.17 Phase 3 Current Path

CHAPTER 3

INPUT CAPACITORS

Most power supplies require some form of charge buffers. On the input side of the H-Bridge is a capacitor bank designed to provide reactive power and assist in the power surge when the IGBT's are turned on. The capacitor bank is connected across the DC inputs of the H-Bridge, as shown in Figure 3.1.

Figure 3.1 Circuit of input capacitors

The capacitor bank is separated into 6 removable modules. Each module has 8 ea, 1500 μ F @ 450 V electrolytic capacitors, as shown in Figures 3.2 and 3.3. The capacitors are connected so that there are 4 parallel pairs of series capacitors. The connection of the capacitors in series changes the value of a pair of capacitors to 750 μ F @ 900 V. Once these pairs of capacitors are connected parallel to each other, the value of a module becomes 3000 μ F @ 900V. The total value of all six modules becomes 18000 μ F @ 900V. The circuit layout of the capacitors can be seen in Figure 3.3. The actual value of the 6 input capacitor modules is 22000 μ F @ 900V. This value was calculated by measuring the RC time constant as the input bank is discharged through a 2.5 k Ω resistor, as

shown in Figure 3.4. The input capacitors do not discharge at a steady rate. The rate of discharge is rapid at first, but slows considerably as the charge approaches zero. During each time constant, the input capacitors discharge 63.2% of the remaining charge. The input capacitors are considered discharged at the end of 5 time constants, as shown in Figure 3.4.

Figure 3.2 Capacitor Banks

Figure 3.3 Layout of Capacitor Modules

Figure 3.4 Capacitor RC discharge

The internal connections of the input capacitor modules have been designed to reduce the stray inductance (L_S) as much as possible. The capacitors had to be connected to each other using center posts and connector plates. The center posts connected the the series capacitors to each other so that the other terminals could be connected to the connector plates for the positive and negative terminals of the module, as shown in Figures 3.5, 3.6 and 3.7. The connection of the center posts and connector plates can be further seen in the cross-section in Figure 3.8. Insulation of the post and plates is provided by 4 insulating sheets. The insulators used were rubber sheets which allowed the sheets to conform to the contours between the conducting parts. The sheets were also designed to cover up resistors and MOV's to reduce any possibility of a component failure affecting other components.

Figure 3.5 Front View of Capacitor Bank Connections

Figure 3.6 Side Picture of Capacitor Bank Connections

Figure 3.7 Side View of Capacitor Bank Connections

Figure 3.8 Cross Section of Capacitor Bank Connections

A problem arises from the layout of the the capacitors. In a perfect situation when 600 Vdc is applied across the capacitors, both capacitors should act as a voltage divider and each should have 300 Vdc across the terminals. Since the capacitors are not exactly the same due to imperfections in manufacturing and the age of the capacitors, extra circuitry must be added to correct the imbalance in the voltages. Initially resistors (680 k Ω) and MOV's were added across the terminals of each capacitor, as shown in Figures 3.9, 3.10 and 3.11. The MOV's purpose is to start to turn on at 450 V and to turn on hard at 500 V. Initially this worked for low input voltages (below 450 Vdc). Once the input voltage rose above 550 Vdc, one of the MOV's failed and discharged the entire bank and caused a short across the charging transformer. The discharge threw the breakers and shorted the input rectifier. The MOV (MOV 2_a) failed because the capacitor (C_{1a}) that was in series with the MOV's capacitor failed and had a large leakage current, as shown in Figures 3.12 and 3.13. The MOV turned on hard as it tried to balance the voltage

between the capacitors and eventually failed as the MOV heated up until it broke its casing and caused a short that resulted in the full discharge of the input capacitor bank (2.7 kJ) and the power supply. After the failure of the MOV in the capacitor bank all of the banks were tested to determine the problem areas. The banks, were individually charged up to 620 V to measure imbalances in the voltage sharing as seen in Table 3.1. Measurements were taken on the terminal that is shared by the series capacitors with respect to both ground and the high voltage terminal. Initial tests showed that the midpoint voltages varied on an average 19.29% with a maximum variation of 54.5% as seen in Table 3.1. From this information it was determined which capacitors created potential problems and they were replaced.

Figure 3.9 Implementation of Protective Circuits

Figure 3.10 MOV's and Resistors in Place

Figure 3.11 Top View of MOV's and Resistors

Figure 3.12 Failure of Capacitor and MOV

Figure 3.13 Picture of Failed MOV

Table 3.1 Initial Voltage Levels of Capacitor Banks

Initial Test of Capacitor Banks	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6
Initial Charging Voltage	620.0 V	574.0 V	619.0 V	600.0 V	620.0 V	619.0 V
1/2 of charging Voltage	310.0 V	287.0 V	309.5 V	300.0 V	310.0 V	309.5 V
Center Post A						
Respect to ground	348.0 V	129.7 V	216.1 V	414.0 V	192.6 V	257.2 V
Respect to High	271.0 V	440.0 V	402.0 V	187.9 V	422.0 V	361.0 V
Ground + High	619.0 V	569.7 V	618.1 V	601.9 V	614.6 V	618.2 V
Voltage Sharing High Cap	43.8%	77.2%	65.0%	31.2%	68.7%	58.4%
Voltage Sharing Ground Cap	56.2%	22.8%	35.0%	68.8%	31.3%	41.6%
Difference in Voltage Sharing	12.4%	54.5%	30.1%	37.6%	37.3%	16.8%
Center Post B						
Respect to ground	344.0 V	266.4 V	218.0 V	172.8 V	294.5 V	277.4 V
Respect to High	276.0 V	310.6 V	400.0 V	427.0 V	322.7 V	339.4 V
Ground + High	620.0 V	577.0 V	618.0 V	599.8 V	617.2 V	616.8 V
Voltage Sharing High Cap	44.5%	53.8%	64.7%	71.2%	52.3%	55.0%
Voltage Sharing Ground Cap	55.5%	46.2%	35.3%	28.8%	47.7%	45.0%
Difference in Voltage Sharing	11.0%	7.7%	29.4%	42.4%	4.6%	10.1%
Center Post C						
Respect to ground	294.6 V	285.5 V	406.0 V	312.4 V	330.0 V	281.4 V
Respect to High	328.0 V	295.2 V	216.0 V	285.8 V	289.7 V	331.0 V
Ground + High	622.6 V	580.7 V	622.0 V	598.2 V	619.7 V	612.4 V
Voltage Sharing High Cap	52.7%	50.8%	34.7%	45.7%	46.7%	54.0%
Voltage Sharing Ground Cap	47.3%	49.2%	65.3%	54.7%	53.3%	46.0%
Difference in Voltage Sharing	5.4%	1.7%	30.5%	8.9%	6.5%	8.1%
Center Post D						
Respect to ground	271.3 V	221.9 V	333.0 V	202.0 V	390.0 V	324.2 V
Respect to High	353.3 V	356.0 V	284.5 V	399.0 V	228.6 V	292.3 V
Ground + High	624.6 V	577.9 V	617.5 V	601.0 V	618.6 V	616.5 V
Voltage Sharing High Cap	56.6%	61.6%	46.1%	66.4%	37.0%	47.4%
Voltage Sharing Ground Cap	43.4%	38.4%	53.9%	33.6%	63.0%	52.6%
Difference in Voltage Sharing	13.1%	23.2%	7.9%	32.8%	26.1%	5.2%

The second level of protection was applied to the capacitors. A resistive network was used to force the center posts of the series capacitors to evenly share voltage as in Figures 3.14 and 3.16.

Balancing resistors are required if two electrolytics are connected in series. Without them, leakage current through both capacitors is the same. Because leakage current for two electrolytics can be quite different when the same voltage is applied, forcing the same current through both capacitors causes an uneven voltage division between them....and one [capacitor] may be subjected to voltage exceeding its rated voltage. [Steeg p.53]

All of the center post in each module are connected together through the

center point, as shown in Figure 3.14. A 1 k Ω resistor (R_3 resistors shown in Figures 3.15 and 3.16) is placed between each center post and the center point to allow for some voltage variation between the center posts. The center point was positioned between the upper and lower connecting plates with insulation on both sides to isolate the conductors. Additional tests were taken for the capacitor banks both before and after the introduction of the resistive network as seen in Tables 3.3 and 3.4. In both tests the banks were individually charged up to 620 V to measure imbalances in the voltage sharing. Measurements were taken on the terminal that is shared by the series capacitors with respect to both ground and the high voltage terminal. Testing of the capacitor banks before the resistive network was in place showed that the midpoint voltage varied on an average 14.7% with a maximum variation of 37.3%, as shown in Table 3.3. Testing of the capacitor banks after the resistive network was in place showed that the midpoint voltage varied on an average of 6.2% with a maximum variation of 14.8%, as shown in Table 3.4. To further balance the voltage sharing, each of the center posts were connected to a voltage divider that was designed to dynamically provide 1/2 of the voltage being applied to the inputs of the H-Bridge through the midpoint from a pair of 69.8 k Ω resistors (R_{sa} shown in Figure 3.16). Voltage levels showed that center points for each capacitor bank was within ± 3.9 Volts of 146.5 Volts when the bank was charged to 295 Volts, as shown in Table 3.3.

Figure 3.14 Top View Showing Resistive Network

Figure 3.15 Picture of Resistive Network

Figure 3.16 Resistive network

Table 3.2 Input Capacitor Center Point Voltage Measurements

	Voltage Midpoint	Voltage CenterPoint	Voltage Difference	Difference (ABS)
Input Capacitor Bank 1	146.4 V	143.5 V	2.9 V	2.9 V
Input Capacitor Bank 2	146.4 V	148.3 V	-1.9 V	1.9 V
Input Capacitor Bank 3	146.4 V	147.3 V	-0.9 V	0.9 V
Input Capacitor Bank 4	146.4 V	148.1 V	-1.7 V	1.7 V
Input Capacitor Bank 5	146.4 V	146.7 V	-0.3 V	0.3 V
Input Capacitor Bank 6	146.4 V	145.7 V	0.7 V	0.7 V
Average Difference				1.4 V
Maximum Difference				2.9 V
Minimum Difference				0.3 V
Standard Deviation				1.0 V

Table 3.3 Voltage Levels before Resistive Network Added

Second Testing of Banks Replacing Capacitors	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6
Initial Charging Voltage	620.0 V	620.0 V	619.0 V	619.0 V	620.0 V	619.0 V
1/2 of charging Voltage	310.0 V	310.0 V	309.5 V	309.5 V	310.0 V	309.5 V
Center Post A						
Respect to ground	348.0 V	306.5 V	216.1 V	257.2 V	192.6 V	413.0 V
Respect to High	271.0 V	311.3 V	402.0 V	361.0 V	422.0 V	204.0 V
Ground + High	619.0 V	617.8 V	618.1 V	618.2 V	614.6 V	617.0 V
Voltage Sharing High Cap	43.8%	50.4%	65.0%	58.4%	68.7%	33.1%
Voltage Sharing Ground Cap	56.2%	49.6%	35.0%	41.6%	31.3%	66.9%
Difference in Voltage Sharing	12.4%	0.8%	30.1%	16.8%	37.3%	33.9%
Center Post B						
Respect to ground	344.0 V	290.0 V	218.0 V	277.4 V	294.5 V	298.1 V
Respect to High	276.0 V	331.5 V	400.0 V	339.4 V	322.7 V	317.7 V
Ground + High	620.0 V	621.5 V	618.0 V	616.8 V	617.2 V	615.8 V
Voltage Sharing High Cap	44.5%	53.3%	64.7%	55.0%	52.3%	51.6%
Voltage Sharing Ground Cap	55.5%	46.7%	35.3%	45.0%	47.7%	48.4%
Difference in Voltage Sharing	11.0%	6.7%	29.4%	10.1%	4.6%	3.2%
Center Post C						
Respect to ground	294.6 V	304.3 V	406.0 V	281.4 V	330.0 V	322.4 V
Respect to High	328.0 V	309.5 V	216.0 V	331.0 V	289.7 V	290.5 V
Ground + High	622.6 V	613.8 V	622.0 V	612.4 V	619.7 V	612.9 V
Voltage Sharing High Cap	52.7%	50.4%	34.7%	54.0%	46.7%	47.4%
Voltage Sharing Ground Cap	47.3%	49.6%	65.3%	46.0%	53.3%	52.6%
Difference in Voltage Sharing	5.4%	0.8%	30.5%	8.1%	6.5%	5.2%
Center Post D						
Respect to ground	271.3 V	242.8 V	333.0 V	324.2 V	390.0 V	226.2 V
Respect to High	353.3 V	377.0 V	284.5 V	292.3 V	228.6 V	389.1 V
Ground + High	624.6 V	619.8 V	617.5 V	616.5 V	618.6 V	615.3 V
Voltage Sharing High Cap	56.6%	60.8%	46.1%	47.4%	37.0%	63.2%
Voltage Sharing Ground Cap	43.4%	39.2%	53.9%	52.6%	63.0%	36.8%
Difference in Voltage Sharing	13.1%	21.7%	7.9%	5.2%	26.1%	26.5%

Table 3.4 Voltage Levels after Resistive Network

Final Testing with Bank Resistors in Place	Bank 1	Bank 2	Bank 3	Bank 4	Bank 5	Bank 6
Initial Charging Voltage	621.0 V	620.0 V	618.0 V	622.0 V	621.0 V	620.0 V
1/2 of charging Voltage	310.5 V	310.0 V	309.0 V	311.0 V	310.5 V	310.0 V
Center point to Ground	312.7 V	272.2 V	292.5 V	313.6 V	281.6 V	336.0 V
Center Post A						
Respect to ground	313.2 V	263.3 V	286.5 V	312.5 V	281.8 V	340.0 V
Respect to High	309.1 V	355.0 V	331.0 V	309.0 V	341.0 V	281.1 V
Ground + High	622.3 V	618.3 V	617.5 V	621.5 V	622.8 V	621.1 V
Voltage Sharing High Cap	49.7%	57.4%	53.6%	49.7%	54.8%	45.3%
Voltage Sharing Ground Cap	50.3%	42.6%	46.4%	50.3%	45.2%	54.7%
Difference in Voltage Sharing	0.7%	14.8%	7.2%	0.6%	9.5%	9.5%
Difference ground and Center	-0.5 V	8.9 V	6.0 V	1.1 V	-0.2 V	-4.0 V
Center Post B						
Respect to ground	313.4 V	272.4 V	289.8 V	321.5 V	281.9 V	335.0 V
Respect to High	308.9 V	346.0 V	330.0 V	308.6 V	341.4 V	284.6 V
Ground + High	622.3 V	618.4 V	619.8 V	630.1 V	623.3 V	619.6 V
Voltage Sharing High Cap	49.6%	56.0%	53.2%	49.0%	54.8%	45.9%
Voltage Sharing Ground Cap	50.4%	44.0%	46.8%	51.0%	45.2%	54.1%
Difference in Voltage Sharing	0.7%	11.9%	6.5%	2.0%	9.5%	8.1%
Difference ground and Center	-0.7 V	-0.2 V	2.7 V	-7.9 V	-0.3 V	1.0 V
Center Post C						
Respect to ground	308.9 V	272.2 V	303.2 V	312.7 V	281.4 V	334.0 V
Respect to High	311.7 V	345.0 V	321.8 V	308.3 V	341.0 V	284.4 V
Ground + High	620.6 V	617.2 V	625.0 V	621.0 V	622.4 V	618.4 V
Voltage Sharing High Cap	50.2%	55.9%	51.5%	49.6%	54.8%	46.0%
Voltage Sharing Ground Cap	49.8%	44.1%	48.5%	50.4%	45.2%	54.0%
Difference in Voltage Sharing	0.5%	11.8%	3.0%	0.7%	9.6%	8.0%
Difference ground and Center	3.8 V	0.0 V	-10.7 V	0.9 V	0.2 V	2.0 V
Center Post D						
Respect to ground	309.9 V	277.2 V	295.0 V	315.6 V	279.2 V	331.0 V
Respect to High	311.3 V	343.0 V	324.4 V	306.0 V	344.0 V	288.1 V
Ground + High	621.2 V	620.2 V	619.4 V	621.6 V	623.2 V	619.1 V
Voltage Sharing High Cap	50.1%	55.3%	52.4%	49.2%	55.2%	46.5%
Voltage Sharing Ground Cap	49.9%	44.7%	47.6%	50.8%	44.8%	53.5%
Difference in Voltage Sharing	0.2%	10.6%	4.7%	1.5%	10.4%	6.9%
Difference ground and Center	2.8 V	-5.0 V	-2.5 V	-2.0 V	2.4 V	5.0 V
Total Gnd Center Differences	5.4 V	3.7 V	-4.5 V	-7.9 V	2.1 V	4.0 V

CHAPTER 4

TRANSFORMER

The H-Bridge directly drives the primary of the step-up transformer. Once the H-Bridge has turned the DC into AC, the voltage can be stepped up through the use of a simple transformer. The transformer is located after the H-Bridge, as shown in Figure 4.1. The custom built transformer is a high frequency, iron core model, constructed by Stangenes Industries. The transformer is designed to operate at 10 kHz, which keeps the size of the transformer small and is within the operating parameters of the H-Bridge. The turns ratio of the transformer is 1:60 which steps up the 650 V input from the H-bridge to a maximum of 39 kV output. The transformer parameters can be seen in Table 4.1. The Transformer is immersed in oil to increase the hold off voltage of the coils as seen in Figures 4.2 and 4.3.

Figure 4.1 Transformer Location in the Circuit

Table 4.1 Transformer Parameters

Stangenes Industries			
Model Number	SI-13267	Core	Iron
Turns Ratio	1:60	Operating Frequency	10 kHz
R Primary	150 mΩ	Primary Voltage	500 V
R Secondary	30 Ω	Primary Current	600 A
L1	4.45 mH	Secondary Voltage	30 kV
L2	16.5 H	Secondary Current	10 A
Coupling	0.999	Weight	9.05 kg

Figure 4.2 Transformer inside Oil Tank

Figure 4.3 Schematic of Transformer

CHAPTER 5

OUTPUT RECTIFIER

A full wave rectifier is needed to convert the AC voltage coming out of the transformer into DC needed to charge the capacitor. Particular care had to be taken in the selection of the rectifier. Even though the circuit shown in Figure 5.1 seems relatively simple, each diode shown in the output rectifier is actually made up of 64 diodes (D_{XrX}) each capable of 1000 V @ 3 A, creating a grading network.

Figure 5.1 Output Rectifier Location in the Circuit

The string of 64 resistors and capacitors provide voltage sharing across each diode, as shown in Figure 5.2. The 4.7 MΩ resistors (R_{XrX}) provide equal voltage sharing for the DC component of the network. The capacitors (C_{XrX}) provide equal voltage sharing for the AC component of the network. Current limiting resistors (R_{r1} and R_{r2}) were added to the input and output terminals of the rectifier, as shown in Figure 5.1. The current limiting resistors protect the rectifier from an accidental external ringing discharge of the load capacitor (C_2). During an external ringing discharge the resistor limits the current through the diodes for negative capacitor voltages. To further protect the diodes, the rectifier was

immersed in oil to increase the hold off voltage, as shown in Figure 5.3.

Figure 5.2 Diode arrangement

Figure 5.3 Diode Arrangement in Oil Tank

CHAPTER 6

THERMAL BATTERY

The load capacitor is to be charged from a thermal battery in the final configuration, as shown in Figure 6.1. The thermal battery is able to deliver 500 volts (V_B) at 360 amps which provides a very compact energy source. A thermal battery is a single use battery that burns itself out. The use of a thermal battery in testing of the power supply would not allow for flexibility in testing. For experimentation the thermal battery was replaced by a 480 V (V_S), 3-phase, 70 amp Variac stack (Y-Y auto transformer), as shown in Table 6.1 and Figures 6.2 and 6.3. The line to line voltage (V_{LL}) of the Variac stack has a maximum voltage of 648.2 V as in Eq. (6.1).

$$V_{LL} = V_S \frac{3}{\pi} \sqrt{2} \quad (6.1)$$

The output of the Variac stack is then passed through a full wave 3-phase rectifier which converts the output to DC, as shown in Table 6.2 and Figures 6.2 and 6.4. The output voltage of the rectifier is 648.2 Vdc at 70 amps.

Figure 6.1 Thermal Battery Location in Circuit

Table 6.1 Variac Stack Parameters

American HV Test Systems Inc.	
Model	Variac Stack
Phase	3 - Phase
Transformer	Y-Y Auto transformer
V_I	440 V
V_O	0 - 440 V
I_I	70 A
I_O	0 - 70 A

Figure 6.2 Variac Stack and Input Rectifier

Figure 6.3 Variac Stack

Table 6.2 Rectifier Parameters

Semikron	Semipack 1
Model	SKKD 46
V_{RRM}	400 ... 1800 V
I_{FRMS}	90 A
$I_{FAV} @ T_{case}$	45 A @ 86°C
$I_{FSM} 25^{\circ}C$	700 A
$T_{vj} \text{ max.}$	125°C
R_{thjc}	60 K/W

Figure 6.4 3-Phase AC Rectifier

CHAPTER 7

DUMP CIRCUITRY

In order to reduce the chance of accidental discharges, a number of electromagnetic switches and current limiting resistors were added to the experiment. Three switched resistors were added to protect the experiment.

In order to dump the load capacitors, an electric dump switch (S_1) and a $2.5\text{ k}\Omega$ resistor (R_{d1}) were added to the experiment, as shown in Figure 7.1. The resistor is used to discharge the load capacitors quickly but at the same time provide current limiting if it is accidentally left in the circuit during charging. The use of the $2.5\text{ k}\Omega$ resistor limits the discharging current to maximum of 12 amps when the load capacitor bank is at its full charge of 30 kV.

Figure 7.1 Load Capacitor Dump Circuit

In order to dump the charge of the input capacitors, an electric dump switch (S_2) and a $2.5\text{ k}\Omega$ resistor (R_{d2}) were added to the experiment, as shown in Figure 7.2. The resistor is used to discharge the input capacitors, and to provide current limiting of the charging supply if it is accidentally left in the circuit. The use of the $2.5\text{ k}\Omega$ resistor limits the

discharge current to a maximum of 0.26 amps when the input capacitor bank is at its full charge of 650 V.

Figure 7.2 Input Capacitor Dump Circuit

A problem arose when an MOV failed on the input capacitor banks. Along with the charge stored in the banks being discharged through the failed MOV, the charging supply continued to supply current to the DC arc until the fuses and breakers of the charging supply interrupted the current flow. A 50 Ω resistor (R_{d3}) was added to the experiment to provide current limiting protection for the charging supply to prevent this from happening again, as shown in Figure 7.3. The use of the 50 Ω resistor limits the charging current to maximum of 12 Amps when the load capacitor bank is being charged to its full charge of 650 V which is well below the 70 amps rating of the charging supply. Just prior to the activation of the H-Bridge, the 50 Ω resistor is taken out of the circuit by the closing of electromagnetic switch (S_3). With the resistor removed from the circuit, the charging supply can deliver the largest surge current possible. As soon as the H-bridge has been fired the switch is opened and the resistor is back in the circuit providing current protection.

Figure 7.3 Charging Resistor Circuit

The addition of protection circuits to the experiment has improved the safety and the reliability of the experiment. The total implementation of the switches and the resistors can be seen in Figures 7.4 and 7.5. During charging of the input capacitors switches S_2 and S_3 are open and switch S_1 is closed. During the activation of the H-Bridge switch S_3 is closed and switches S_2 and S_1 are open. When the system is off, switches S_1 and S_2 are closed and switch S_3 is open, as shown in Table 7.1.

Figure 7.4 Circuit Showing all Protective Dumps in Place

Figure 7.5 Photo Showing all Protective Dumps in Place

Table 7.1 Dump Switch Settings

	System Charging	System Firing	System Off
Switch 1 (Load Capacitor)	CLOSED	OPEN	CLOSED
Switch 2 (Input Capacitor)	OPEN	OPEN	CLOSED
Switch 3 (Charging Resistor)	OPEN	CLOSED	OPEN

CHAPTER 8

EXPERIMENTAL LAYOUT

The layout of the power supply took considerable thought to keep the power supply compact and accessible. The design took into consideration that modifications would need to be made as the experiment progresses. The experiment consists of three major components: the variac stack, the power supply cabinet and the load capacitors, as shown in Figure 8.1.

Figure 8.1 Variac Stack, Cabinet and Load Capacitor Bank

The H-Bridge, bus bars and the input capacitors (C_1) were assembled to determine the size of the assembly. Figure 8.2 shows parallel half bridges mounted back to back after the heat sinks have been removed. Figure 8.3 shows the AC bus attached to the parallel half bridges. Figure 8.4 shows the attachment of the negative DC bus and the placement of the insulator sheet. The insulator sheet has holes punched into the edge to match the terminal fingers. Figure 8.5 shows the attachment of the

positive DC bus. The positive DC bus is placed over the negative DC bus separated by the insulator sheet. Figure 8.6 shows the placement of aluminum spacers that are needed so that the extended terminals match the snubber terminals. Figure 8.7 shows the attachment of the DC bus snubbers. Figure 8.8 shows the insulator placed under the snubbers to insulate them from the positive DC bus and shows the layout of the H-Bridge bus work.

Figure 8.2 Parallel Half Bridges

Figure 8.3 Attachment of AC Bus

Figure 8.4 Attachment of Negative DC Bus and Insulator

Figure 8.5 Attachment of Positive DC Bus

Figure 8.6 Placement of Aluminum Spacers

Figure 8.7 Attachment of DC Bus Snubbers

Figure 8.8 Snubber Insulators and Layout of H-Bridge Bus Work

Figure 8.9 show the half bridges with the bus work attached. The half bridges are mounted back to back to reduce the stray inductance (L_S) and the overall size of the package. The AC bus bar is bolted to both parallel half bridges; an identical AC bus bar is attached to the other half bridge. The AC bus bars are isolated from the IGBT base plate with an insulating sheet. The negative DC bus bar is bolted to all of the negative terminals on the IGBT's. The negative bus bar is isolated from the IGBT base plate with an insulating sheet. The DC bus bar insulator is a rubber sheet that isolates the positive and negative bus bars channels with overlap added for additional voltage protection. The positive DC bus bar is bolted to all of the positive terminals on the IGBT's. The snubbers are attached across the DC terminals of the IGBT's

Figure 8.9 End View of IGBT with Bus Work Attached

Once the H-Bridge, bus work and input capacitors were assembled (as shown in Figure 8.10) measurements confirmed that the assembly could be hung vertically inside a standard 19" cabinet.

Figure 8.10 H-Bridge, Bus Work and Input Capacitors

The cabinet that was found had quick removal side panels which allowed all sides of the power supply to be easily accessible. The H-Bridge and bus work were hung from the top of the cabinet from a hanging plate that is connected to a sliding support. The use of a sliding connection allowed the H-Bridge to be moved inside of the cabinet allowing for great flexibility, as shown in Figure 8.11. The hanging plate has adjustable eyelets that gives the H-Bridge and bus work 4 inches of vertical travel. The input capacitors (C_1) are supported by adjustable support plates. The support plates are attached to vertical unistruts inside the cabinet which allows the input capacitor supports to be positioned anywhere along the side of the cabinet. Each input capacitor module can be removed simply by unplugging the module from the large plugs on the DC bus, as shown in Figure 8.12

Figure 8.11 H-Bridge Hanging inside Cabinet

Figure 8.12 Input Capacitor Terminals

The power supply cabinet contains all the power supply components. A number of shelves attached inside of the cabinet support the power supply components. The shelves are made of lucite to provide isolation of

the components from the cabinet. The microcontroller, interface board and the 15 V power supply used to control the H-Bridge are located on the microcontroller shelf, as shown in Figure 8.13. The input rectifier (D_{1v} through D_{6v}), input capacitor dump switch (S_2) and the input capacitor dump resistors (R_{d2}) are located on the input shelf, as shown in Figure 8.14. On the bottom of Figure 8.14, the load capacitor dump switch (S_3) and the charging resistor dump switch (S_1) can be seen bolted to the base of the cabinet. The center post balancing resistors (R_{Sa} through R_{Sd}) and the voltage divider resistors (R_{va} and R_{vb}) are located on the input capacitor resistor leveling shelf, as shown in Figure 8.15. The high frequency transformer and the Pearson current probe are supported by the transformer shelf, as shown in Figure 8.16. The output rectifier is supported by the rectifier shelf, as shown in Figure 8.16.

Figure 8.13 Micro-controller Shelf

Figure 8.14 Input Shelf

Figure 8.15 Input Capacitor Resistor Leveling Shelf

Figure 8.16 Transformer and Output Rectifier Shelf

The cabinet allowed for a very compact design with all of the components accessible from all sides. Each of the components listed before are shown in Figure 8.17. As shown, all of the components are easily accessible with the side panels removed from the cabinet.

Figure 8.17 Power Supply Cabinet Side and Front View

The $7.4 \mu\text{F}$ load capacitor (C_2) was constructed using 4 parallel Aerovox (PX300D25) capacitors, rated at $1.85 \mu\text{F}$ @ 60 kV each, as shown in Figure 8.18. The capacitors are encased in a protective shield to reduce the danger from a capacitor failure. Located at the end of the capacitor cart is the Gentec high voltage probe used to measure the voltage level of the load capacitors (C_2).

Figure 8.18 Load Capacitors

CHAPTER 9

H-BRIDGE CONTROL

The SKiiPPACK Dual-IGBT' modules are controlled by a Motorola HC12 micro-controller with a custom control board added, as shown in Figure 9.1. The Motorola HC12 micro-controller was chosen because of its versatility and features. The Motorola HC12 parameters are shown in Table 9.1. The microcontroller generates the control signals with varying pulse widths that drive the gates of the IGBT's through the interface port on each module, as shown in Figure 9.2. The micro-controller is isolated from the IGBT modules through the use of an interface board using HCPL2232 opto-couplers shown in Figures 9.3 and 9.4. Beside isolation, the opto-couplers provide the necessary level shifting to convert the HC12 signals from a range of 0-5 V to the range of 0-15 V needed to drive the gates on the IGBT modules.

Figure 9.1 Motorola HC12 with Control Board

Table 9.1 Motorola 68HC12A0 Features

68HC12A0 Features	
CPU	Low-Power, High-Speed M68HC12 CPU
Clock Speed	8MHz
Bus Size	16 Bit
Memory	1024-Byte RAM, 32 K Flash EEPROM
Timer	16-Bit Timer with Programmable Prescaler
A to D	8-Channel, 8-Bit Analog-to-Digital Converter

Figure 9.2 Interface Port on IGBT Module

Figure 9.3 Interface Board

Figure 9.4 Circuit Board Layout

The interface board monitors the H-Bridge modules for error detection from the integrated drivers and protection circuitry of the IGBT's, as shown in Figure 9.5. Each half bridge module contains on board monitoring circuitry that is designed to send out flag signals if a problem arises that will shut off the control signal from the microcontroller.

Figure 9.5 Error Detection for H-Bridge

The H-Bridge modules are controlled through pulse width modulation (PWM). Each half bridge is controlled by its own PWM signal from the microcontroller, as shown in Figure 9.6. The 40 ms charging time is

broken into 400 PWM cycles each lasting 100 μs . Each PWM cycle is broken into 800 clock cycles, the first 400 clock cycles control half bridge A and the second 400 clock cycles control half bridge B. The pulse width can be increased or decreased by an integral number of clock cycles. The rate of the PWM increase is controlled by the micro-controller with great flexibility, so that the optimum setting can be found experimentally.

Figure 9.6 Half Bridge Pulse Width Modulation

The H-Bridge directly drives the primary of the step-up transformer. The IGBT's are activated as opposing legs. When IGBT's 1 and 4 are activated the transformer has current flowing counter clockwise through the transformer as seen in Figure 9.7. When IGBT's 2 and 3 are activated the transformer has current flowing clockwise through the transformer as seen in Figure 9.8. The alternate switching of the H-Bridge produces the AC that is needed to drive the step-up transformer. The H-Bridge is cycled 400 times during the 40 ms charging period.

Figure 9.7 Activation of IGBT's 1 & 4

Figure 9.8 Activation of IGBT's 2 & 3

The initial duty cycle (D_i) is the starting duty cycle of the IGBT's. Each PWM cycle is broken into 400 clock cycles (T_s) with the maximum initial duty cycle (D_i) setting (t_{on}) of 308 which works out to a 77% duty cycle (D), as shown in Figure 9.9 and Eq. (9.1).

$$D = \frac{t_{on}}{T_s} \quad (9.1)$$

Dip switches control the rate at which the duty cycle is increased (Bank 1) and how often it is increased (Bank 2), as shown in Figure 9.10. Bank 2 (Dip switches 1-4) controls how often the increase takes place with a range of 0-15. Bank 1 (Dip switches 5-8) controls how much the

initial duty cycle (D_i) is increased with a range of 0-15. The Dip settings are listed as Y/X with Y stating the setting of bank 1 and X stating the setting of of bank 2. The fastest increase would be setting 15/1 which would increase the initial duty cycle (D_i) setting by 15 every cycle (as shown in Figure 9.11) until the maximum cycle of 308 is reached, as shown in Figure 9.12.

Figure 9.9 H-Bridge Operation at Full Duty Cycle of 77% (308/400)

Figure 9.10 DIP Switch Arrangement

Figure 9.11 Initial Duty Cycle setting 20, Dip setting at 15/1

Figure 9.12 Example of Initial Duty Cycle and Dip Settings

Each PWM cycle is controlled by a interrupt routine that controls the width of the cycle and adjusts the increase of the PWM for the opposite leg of the H-Bridge, as shown in Figure 9.13. Interrupts were used in the control of the PWM as they can be activated so that no other CPU functions will interrupt the duration of the pulse and the increase of the next pulse.

Figure 9.13 Interrupt Routine

CHAPTER 10

PULSE MODIFICATION

Examination of the parameters controlling the pulse width modulation (PWM) are an important aspect of understanding how to adjust the experiment. Numerous small tests were conducted to develop a better understanding of the control of the H-Bridge and to verify that the program was working as designed.

At first glance the dip setting of 1/1, 2/2 and 3/3 would seem to have the same slope, as shown in Figure 10.1 and Table 10.1. Tests showed that while the final voltage of the load capacitor was similar, the H-Bridge output currents and voltages showed different waveforms as can be seen in Figures 10.2, 10.3, 10.4 and 10.5. The variation in waveforms seems to have more to do with the coarse increase of the dip switch settings and not as much to do with the variation in the area under the the increase, as shown in Table 10.1. The percentage of change of the area based on the dip settings changes compared to the initial duty cycle setting. Figure 10.5 shows the comparison of the current and voltage waveforms and the variation of the current and voltage waveform envelopes “waistlines”. The current waveforms become uniform after 7 ms and the voltage waveforms become uniform after 15 ms, as shown in Figure 10.5. From the initial duty cycle setting of 81 (51 Hex) all of the dip settings (1/1, 2/2, 3/3) reach the maximum initial duty cycle setting of 308 in 22.7 ms, as shown in Figure 10.5.

Figure 10.1 Example of 1/1, 2/2 and 3/3 Settings

Table 10.1 Settings for 1/1, 2/2, 3/3 Shots

Shot	Initial Capacitors		Initial Duty Cycle				Load	Current		
	Voltage	Joules	(Hex)	DS	Dip	kV	Joules	P-P	kA	Bank
26	298	799.2	51	81	1 / 1	13.0	608.4	N/A	N/A	7.2 μ F
27	298	799.2	51	81	2 / 2	13.0	608.4	N/A	N/A	7.2 μ F
28	298	799.2	51	81	3 / 3	13.0	608.4	N/A	N/A	7.2 μ F

Figure 10.2 Screen Display of 1/1 shot

Figure 10.3 Screen Display of 2/2 shot

Figure 10.4 Screen Display of 3/3 shot

Figure 10.5 Variation of H-Bridge Current and Voltage

Table. 10.2 Variation in Initial Duty Cycle and Dip Settings

Initial Duty Cycle Setting Decimal	Setting (HEX)	Maximum Steps	Starting Cycle	Steps	Maximum Units under 1/1	Dip	Actual Units	Percentage of 1/1
0	0	308	0	308	47432	1/1	47432	100.00%
0	0	308	0	308	47432	2/2	47278	99.68%
0	0	308	0	308	47432	3/3	47124	99.35%
81	51	308	97	211	22165	1/1	22165	100.00%
81	51	308	97	211	22165	2/2	22060	99.53%
81	51	308	97	211	22165	3/3	21954	99.05%
96	60	308	116	193	18528	1/1	18528	100.00%
96	60	308	116	193	18528	2/2	18432	99.48%
96	60	308	116	193	18528	3/3	18336	98.96%
112	70	308	135	173	15008	1/1	15008	100.00%
112	70	308	135	173	15008	2/2	14921	99.42%
112	70	308	135	173	15008	3/3	14835	98.85%
144	90	308	173	135	9079	1/1	9079	100.00%
144	90	308	173	135	9079	2/2	9011	99.26%
144	90	308	173	135	9079	3/3	8944	98.52%
240	F0	308	289	19	185	1/1	185	100.00%
240	F0	308	289	19	185	2/2	176	94.81%
240	F0	308	289	19	185	3/3	166	89.61%

In order to verify that the microcontroller was sending the proper pulses to the IGBT's, samples were taken every 50 shots (5 ms), as shown in Table 10.3. From the initial initial duty cycle setting of 81 (51 Hex) and dip switch setting 1/1 the maximum initial duty cycle setting of 308 is reached in in 22.7 ms, as shown in Figure 10.6. Figures 10.7 through 10.16 verify the increase of the initial duty cycle setting up to the maximum of 308 match the values, as shown in Table 10.3. Channel 1 is the PWM signal driving half bridge A. Channel 2 is the current coming out of the H-Bridge. The current trace reduces in height as compared to the current value in Figure 10.6. Channel 3 is the voltage out of the H-Bridge. Channel 4 is the bus voltage on the input of the H-Bridge. Figure 10.16 shows the start of the end oscillation that occurs when the pulse is turned off at more than 40 ms.

Table 10.3 Changes in Initial Duty Cycle Settings

Initial Duty Cycle	Dip Setting	Time	Shot	Pulse Width	Pulse Width Increase
81	1/1	0 μ s	1	10.13 μ s	0.00 μ s
81	1/1	5 μ s	51	16.38 μ s	6.25 μ s
81	1/1	10 μ s	101	22.63 μ s	6.25 μ s
81	1/1	15 μ s	151	28.88 μ s	6.25 μ s
81	1/1	20 μ s	201	35.13 μ s	6.25 μ s
81	1/1	25 μ s	251	38.50 μ s	3.37 μ s
81	1/1	30 μ s	301	38.50 μ s	0.00 μ s
81	1/1	35 μ s	351	38.50 μ s	0.00 μ s
81	1/1	40 μ s	401	38.50 μ s	0.00 μ s

Figure 10.6 Pulse Number Location

Figure 10.7 Pulse 1

Figure 10.8 Pulse 51

Figure 10.9 Pulse 101

Figure 10.10 Pulse 151

Figure 10.11 Pulse 201

Figure 10.12 Pulse 251

Figure 10.13 Pulse 301

Figure 10.14 Pulse 351

Figure 10.15 Pulse 400

Figure 10.16 Pulse 400+

In order to verify that the microcontroller was sending the proper starting pulses to the IGBT's as seen in Table 10.4, additional examinations were made of the waveforms of the initial pulse (pulse 1) for various initial duty cycle settings. Figures 10.17 through 10.22 verify that the increase of the initial duty cycle setting matches the values shown in Table 10.4. Channel 1 is the PWM signal driving half bridge A. Channel 2 is the current coming out of the H-Bridge. Channel 3 is the voltage out of the H-Bridge. Channel 4 is the bus voltage on the input of the H-Bridge.

Table 10.4 Initial Pulse Width

Initial Duty Cycle Hex	Decimal	Pulse Width
10	16	2.00 μ s
20	32	4.00 μ s
30	48	6.00 μ s
51	81	10.13 μ s
70	112	14.00 μ s
90	144	18.00 μ s

Figure 10.17 Initial Pulse, Duty Cycle Setting of 10

Figure 10.18 Initial Pulse, Duty Cycle Setting of 20

Figure 10.19 Initial Pulse, Duty Cycle Setting of 30

Figure 10.20 Initial Pulse, Duty Cycle Setting of 51

Figure 10.21 Initial Pulse, Duty Cycle Setting of 70

Figure 10.22 Initial Pulse, Duty Cycle Setting of 90

CHAPTER 11

EXPERIMENTAL MEASUREMENTS

One of the most important aspects of any experiment is the measurement of the pertinent electrical parameters. Many parts of the experiment were designed to allow access for measurement that were required to verify the operation parameters of the experiment. The probes were selected to eliminate the need of any attenuation on the signals.

The charging voltage across the input capacitor is measured with a Fluke 79III multimeter. The charging voltage is recorded by hand before the H-Bridge is fired. The voltage meter is connected across the terminals of the input capacitor as seen in Figure 11.1. The voltage level of the input capacitors is 900 V, which is larger than the 650 V that the Variac stack can deliver.

Figure 11.1 Voltage Meter (1:1)

The current coming out of the parallel H-Bridge have to be closely monitored since the H-Bridges are rated at a maximum of 2400 amps. The current is measured with a Pearson 4997 current probe. The Pearson coil is rated at 100:1 outputting 1 V for every 100 amps that pass through the center of the coil. The bandwidth for the Pearson probe is 20

MHz for the upper bandwidth and 0.5 Hz for the lower bandwidth. The output of the current probe is fed into a Tektronix TDS 420A oscilloscope. The Pearson coil is positioned so that one of the bus lines coming out of the H-Bridge passes through the opening of the coil as seen in Figure 11.2.

Figure 11.2 Pearson 4997 Current Probe (100:1)

The voltage output busses of the parallel H-Bridge has to be under the rated 1200 volts. The voltage is measured with a Tektronix P5200 high voltage differential probe. The differential probe is rated at 500:1, outputting 1 V for every 500 V that is applied across the leads. The bandwidth for the P5200 voltage probe is 20 MHz. The output of the differential probe is fed into a Tektronix TDS 420A oscilloscope. The differential probe is connected across the output busses from the H-Bridge as seen in Figure 11.3.

Figure 11.3 P5200 Differential Probe H-Bridge (500:1)

The voltage across the load capacitor is measured with a Gentec high voltage probe. The high voltage probe is rated at 1000:1, outputting 1 V for every 1000 V that is applied across the leads. The output of the voltage probe is fed into a Tektronix TDS 420A oscilloscope. The high voltage probe is connected across the terminals of the load capacitor as seen in Figure 11.4.

Figure 11.4 Gentec High Voltage Probe (1000:1)

The voltage across the terminals of the input capacitor is measured with a Tektronix P5200 high voltage differential probe. The differential probe is rated at 500:1, outputting 1 V for every 500 V that is applied across the leads. The bandwidth for the P5200 voltage probe is 20 MHz. The output of the differential probe is fed into a Tektronix TDS 420A oscilloscope. The differential probe is connected across the output busses from the H-Bridge as seen in Figure 11.5.

Figure 11.5 P5200 Differential Probe Input Capacitors (500:1)

The voltage across the terminals of the interface board is measured with a Hewlett Packard 1160A Probe. The probe is rated at 10:1, outputting 1 V for every 10 V that is applied across the leads. The output of the probe is fed into a Hewlett Packard Infinium oscilloscope. The probe is connected across the opto-couplers on the interface board as seen in Figure 11.6.

Figure 11.6 HP 1160A Probe Connections on Interface Board

The Tektronix TDS 420A oscilloscope is a 4 channel, 200 MHz, 100 kSa/s digital oscilloscope, that is used to measure the waveforms of the currents and voltages during the 40 ms of the shot, as shown in Figure 11.7. The timebase of the oscilloscope is normally set to 5 ms per division so that the 40 ms shot covers 8 out of the 10 divisions on the screen. The oscilloscope is normally triggered by the H-Bridge output voltage through channel 3. Channel 1 measures the terminal voltage of the load capacitors through a Gentec high voltage probe (1000:1) normally set at 5 volts per division. Channel 2 measures the current of the H-Bridge through a Pearson 4997 current probe (100:1) normally set at 10 volts per division. Channel 3 measures the output voltage of the

H-Bridge through a Tektronix P5200 high voltage differential probe (500:1) was set at 0.5 volts per division for shots 0 to 49 and 1 volt per division for shots 50 to 57. Channel 4 measures the terminal voltage of the input capacitors through a Tektronix P5200 high voltage differential probe (500:1) normally set at 200 mV per division.

Figure 11.7 Tektronix TDS 420A Oscilloscope

The Hewlett Packard Infinium oscilloscope is a 4 channel, 500 MHz, 2 GSa/s digital oscilloscope, that is used to measure the waveforms of the currents and voltages during the 40 ms of the shot, as shown in Figure 11.8. The timebase of the oscilloscope is normally set to 5 ms per division so that the 40 ms shot covers 8 out of the 10 divisions on the screen. The oscilloscope is normally triggered by the load capacitor voltage through channel 3. Channel 1 measures the logic pulses from the interface board with a Hewlett Packard 1160A Probe (10:1) normally set at 1 volts per division. Channel 2 measures the current of the H-Bridge through a Pearson 4997 current probe (100:1) normally set at 10 volts per division. Channel 3 measures the output voltage of the H-

Bridge through a Tektronix P5200 high voltage differential probe (500:1) normally set at 1 volt per division. Channel 4 measures the terminal voltage of the input capacitors through a Tektronix P5200 high voltage differential probe (500:1) normally set at 200 mV per division.

Figure 11.8 Hewlett Packard Infinium Oscilloscope

Initial measurements were taken using the Tektronix TDS 420A oscilloscope which provided the data needed to complete the testing of the power supply. The oscilloscope was changed to the Hewlett Packard Infinium to examine the waveforms in greater detail. A problem arose when the Hewlett Packard Infinium oscilloscope was used to take measurements. A stray oscillatory signal appeared on the oscilloscope trace that had not been present on the Tektronix TDS 420A oscilloscope. After researching the problem it was found to be aliasing that was causing the stray oscillatory signal.

Aliasing occurs when the oscilloscope acquires a source waveform with frequency components outside of the frequency range for the current sample rate. In the FFT waveform, the actual higher frequency components are under sampled, and therefore, they appear as lower frequency aliases that “fold back” around the Nyquist point (as shown in Figure 11.9). The greatest frequency that can be input into any sampler without aliasing is $1/2$ the sample frequency.[Tektronix User Manual 3-36]

Signals with fast edge transitions, such as the switching of the IGBT's, create high frequency harmonics which are too fast for the sampling rate of the oscilloscope. The Tektronix TDS 420A oscilloscope was set to sample the signals using the peak detect mode which samples the highest and lowest values of a signal which allows it to detect faster signals for a given time.

Figure 11.9 Fold Back around the Nyquist Point

CHAPTER 12

EXPERIMENTAL DATA

The final goal of the experiment is to prove that the 7.4 μF capacitor bank could be charged to 30 kV in 40 ms. The testing of the power supply had to be done in small steps. The first 25 shots were for calibration and to get a feel for the initial duty cycle and dip switch settings. Shots 26 through 57 were the actual testing of the power supply. Shots 26 through 28 show what influence the dip switch settings have on the waveforms, as shown in Figure 12.1. Each of the settings 1/1, 2/2 and 3/3 increase the initial duty cycle settings at the same slope and produce the same load voltage of 13 kV with different current and voltage waveforms on the output of the H-Bridge. The value of this test shows that the wave forms can be customized to even greater extent than is shown here. The remainder of the shots were designed to get to the final goal of a load voltage of 30 kV. As the voltage was increased, the initial duty cycle and dip switches were adjusted to reach the load voltage of 30 kV without pushing the H-Bridge over the limits of 1200 V or 2400 A, as shown in Figures 12.1 through 12.10. The goal of 30 kV in 40 ms was reached on shot 57 with a maximum of 650 V @1480 A; well below the maximum ratings of the H-Bridge, as shown in Figure 12.10. Shot 55 proved that the load could be charged to at least 30 kV. Shots 35 and 41 were not included since the oscilloscope screen displays on the computer were lost. The volts per division was increased for shots 50 through 57.

Figure 12.1 Shots 26 through 28

Figure 12.2 Shots 29 through 31

Figure 12.3 Shots 32 through 34

Figure 12.4 Shots 36 through 38

Figure 12.5 Shots 39 through 42

Figure 12.6 Shots 43 through 45

Figure 12.7 Shots 46 through 48

Figure 12.8 Shots 49 through 51

Figure 12.9 Shots 52 through 54

Figure 12.10 Shots 55 through 57

Shot 57 reached the goal of charging a 7.2 μ F capacitor to 30.5 kV in 40 ms, as shown in Figure 12.11. A few things to note about the shot is that the voltage curve is almost linear when the input voltage is shut off at 40 ms, rough calculations show that the bank could be charged to a maximum of 39 kV from a input voltage of 650 V based on the step up ratio of the transformer.

Figure 12.11 Shot 57

Table 12.1 Shots 26 through 57

	Input Capacitors		Throttle				Load	Current		
Shot	Voltage	Joules	(Hex)	DS	Dip	kV	Joules	P-P	kA	Bank
26	298	799.2	51	81	1 / 1	13.0	625.3	N/A	N/A	7.4 μ F
27	298	799.2	51	81	2 / 2	13.0	625.3	N/A	N/A	7.4 μ F
28	298	799.2	51	81	3 / 3	13.0	625.3	N/A	N/A	7.4 μ F
29	401	1447.2	51	81	1 / 1	17.8	1172.3	N/A	N/A	7.4 μ F
30	402	1454.4	60	96	1 / 1	18.0	1198.8	25.4	1.27	7.4 μ F
31	402	1454.4	70	112	1 / 1	18.1	1212.2	29.2	1.46	7.4 μ F
32	402	1454.4	70	112	1 / 1	18.1	1212.2	29.4	1.47	7.4 μ F
33	500	2250.0	51	81	1 / 2	20.8	1600.8	43.6	2.18	7.4 μ F
34	400	1440.0	51	81	1 / 2	16.6	1019.6	21.6	1.08	7.4 μ F
36	451	1830.6	51	81	1 / 2	19.3	1378.2	24.4	1.22	7.4 μ F
37	400	1440.0	51	81	1 / 2	16.9	1056.8	21.0	1.05	7.4 μ F
38	451	1830.6	51	81	1 / 2	19.2	1364.0	22.8	1.14	7.4 μ F
39	500	2250.0	51	81	1 / 2	21.7	1742.3	26.6	1.33	7.4 μ F
40	500	2250.0	51	81	1 / 3	20.2	1509.7	20.2	1.01	7.4 μ F
42	400	1440.0	51	81	1 / 3	16.0	947.2	17.0	0.85	7.4 μ F
43	400	1440.0	60	96	1 / 3	16.7	1031.9	20.2	1.01	7.4 μ F
44	400	1440.0	60	96	1 / 3	16.1	959.1	23.2	1.16	7.4 μ F
45	400	1440.0	80	128	1 / 3	17.8	1172.3	27.8	1.39	7.4 μ F
46	400	1440.0	80	128	1 / 3	17.5	1133.1	30.6	1.53	7.4 μ F
47	500	2250.0	51	81	1 / 3	20.6	1570.1	20.6	1.03	7.4 μ F
48	500	2250.0	70	112	1 / 3	22.3	1840.0	32.4	1.62	7.4 μ F
49	550	2722.5	51	81	1 / 3	23.3	2008.7	24.0	1.20	7.4 μ F
50	550	2722.5	60	96	1 / 3	24.3	2184.8	30.6	1.53	7.4 μ F
51	550	2722.5	70	112	1 / 3	25.3	2368.3	31.8	1.59	7.4 μ F
52	600	3240.0	51	81	1 / 3	26.2	2539.8	28.2	1.41	7.4 μ F
53	600	3240.0	60	96	1 / 3	27.4	2777.8	32.8	1.64	7.4 μ F
54	600	3240.0	70	112	1 / 3	28.6	3026.5	40.6	2.03	7.4 μ F
55	600	3240.0	70	112	1 / 3	31.0	2666.8	34.2	1.71	5.6 μ F
56	650	3802.5	51	81	1 / 3	29.2	3154.8	27.8	1.39	7.4 μ F
57	650	3802.5	60	96	1 / 3	30.5	3441.9	29.6	1.48	7.4 μ F

CHAPTER 13

PROGRAM

The Motorola HC12 microcontroller controls the operation of the H-Bridge. The microcontroller generates the control signals with varying pulse widths that drive the gates of the IGBT's through the interface port on each module. The control of the H-Bridge is done through the use of PWM signals controlling the opposing legs. The rate of the PWM increase is controlled by the micro-controller program with great flexibility. The control program (listed as standard program in the appendix) is broken up into segments. The operation of each segment is described briefly to help in understanding the operation of the program.

The program comments are covered in the program introduction section, as shown in Figure 13.1

```
as12 (v1.2) absolute assembler for the Motorola CPU12
Executed: Sat Jun 17 11:03:38 2000

*****
*      Program to produce PWM Signals for 30 kV Rapid Charger      *
*      Written for Motorola M68EVB912B32 Eval Board                *
*      The Program uses the Output Compare 7 Function of the Timers *
*      The Program creates 10 kHz alternating Signals to drive a H-Bridge *
*      The Signals are provided at PT5 and PT6                     *
*      The low Nibble of the DIP Switches is the number of cycles between *
*      Duty Cycle increments. The High Nibble is the number to increment D *
*      IRQ-Switch turns the System on, XIRQ turns it off           *
*      Program uses Real Time Interrupt for Display Routine        *
*      PORT A controls Segm. A-G,dp, High Nibble of PORT P controls Digits *
*      Only the High Nibble of PORT P is written to by the Display Routine *
*      The Display Subroutine is burned into Flash-EEPROM          *
*      The Program uses the Extended Table Lookup Function to Scale the *
*      AD-Converter Output from 0-255 to 0-400                     *
*      ETBL Linearly Interpolates one of 256 result values that fall between *
*      each pair of data entries in a lookup table stored in memory *
*      X points to lower table entry, B holds binary fraction of XL location *
*      The formula for B is given below. The radix point of B is left of MSB *
*       $D = Y1 + [(B) \times (Y2 - Y1)], (B) = (XL - X1) / (X2 - X1)$  *
*      Written for AS12 Assembler, March 08, 2000, by Michael Giesselmann *
*****
                                                                    Courtesy of Dr. Giesselmann
```

Figure 13.1 Program Introduction

The program routines and equivalents that the micro-controller will need, are defined in the program, as shown in Figure 13.2.

* 68HC12 D-Bug 12 Callable Routines *				
* HC12 Regs and other Equivalents *				

0000	PORTA	EQU	\$0000	;Port A Register of HC12
0001	PORTB	EQU	\$0001	;Port B Register of HC12
0002	DDRA	EQU	\$0002	;Data Direction Register Port A
0003	DDRB	EQU	\$0003	;Data Direction Register Port B
000c	PUCR	EQU	\$000C	;Pull Up Resistor Register Port A,B,E
0010	INITRM	EQU	\$0010	;RAM Position Register
0011	INITRG	EQU	\$0011	;CPU Reg Position Register
0012	INITEE	EQU	\$0012	;EEPROM Position Register
0014	RTICTL	EQU	\$0014	;Real Time Interrupt Control Register
0015	RTIFLG	EQU	\$0015	;Real Time Interrupt Flag Register
0016	COPCTL	EQU	\$0016	;Watchdog Timer Control Register
0017	COPRST	EQU	\$0017	;Watchdog Timer Reset Register
001e	INTCR	EQU	\$001E	;Interrupt Control Register

Courtesy of Dr. Giesselmann

Figure 13.2 Program Routines and Equivalents Definitions

The program PWM equivalents, that the micro-controller will need, are defined in the program, as shown in Figure 13.3.

***** PWM Control *****				
0040	PWCLK	EQU	\$0040	;PWM Clocks and Concatenate
0041	PWPOL	EQU	\$0041	;PWM Clock Select and Polarity
0042	PWEN	EQU	\$0042	;PWM Enable Register
0044	PWSCAL0	EQU	\$0044	;PWM Scale Register 0, Channel 0/1
0046	PWSCAL1	EQU	\$0046	;PWM Scale Register 1, Channel 2/3
004c	PWPER0	EQU	\$004C	;PWM Period Register Channel 0
004d	PWPER1	EQU	\$004D	;PWM Period Register Channel 1
004e	PWPER2	EQU	\$004E	;PWM Period Register Channel 2
004f	PWPER3	EQU	\$004F	;PWM Period Register Channel 3
0050	PWDY0	EQU	\$0050	;PWM Duty Register Channel 0
0051	PWDY1	EQU	\$0051	;PWM Duty Register Channel 1
0052	PWDY2	EQU	\$0052	;PWM Duty Register Channel 2
0053	PWDY3	EQU	\$0053	;PWM Duty Register Channel 3
0054	PWCTL	EQU	\$0054	;PWM Control Register
0056	PORTP	EQU	\$0056	;Port P Data Register
0057	DDRP	EQU	\$0057	;Port P Data Direction Register

Courtesy of Dr. Giesselmann

Figure 13.3 Program PWM Equivalents Definitions

The program analog to digital equivalents, that the micro-controller will need, are defined in the program, as shown in Figure 13.4.

***** AD Control *****				
0062	ATDCTL2	EQU	\$0062	;ATD Control Register 2
0065	ATDCTL5	EQU	\$0065	;ATD Control Register 5
006f	PORTAD	EQU	\$006F	;Port AD Input Register
0070	ADR0H	EQU	\$0070	;ATD Converter Result Register 0
0072	ADR1H	EQU	\$0072	;ATD Converter Result Register 1
0074	ADR2H	EQU	\$0074	;ATD Converter Result Register 2

Courtesy of Dr. Giesselmann

Figure 13.4 Program Analog to Digital Equivalents Definitions

The program timer register equivalents, that the micro-controller will need, are defined in the program, as shown in Figure 13.5. Without equivalents the code that follows would be even harder to read. The equivalents specify memory locations and assign names to them. The names suggest what the function of the data at the memory location is.

***** Timer Registers *****				
0080	TIOS	EQU	\$0080	;Timer Input Capture, Output Compare Select
0081	CFORC	EQU	\$0081	;Timer Compare Force Register
0082	OC7M	EQU	\$0082	;Output Compare 7 Mask Register
0083	OC7D	EQU	\$0083	;Output Compare 7 Data Register
0084	TCNT	EQU	\$0084	;16 Bit Free Running Counter
0086	TSCR	EQU	\$0086	;Timer System Control Register
0088	TCTL1	EQU	\$0088	;Timer Control Register 1
0089	TCTL2	EQU	\$0089	;Timer Control Register 2
008a	TCTL3	EQU	\$008A	;Timer Control Register 3
008b	TCTL4	EQU	\$008B	;Timer Control Register 4
008c	TMSK1	EQU	\$008C	;Timer Mask 1
008d	TMSK2	EQU	\$008D	;Timer Mask 2
008e	TFLG1	EQU	\$008E	;Timer Interrupt Flag 1
008f	TFLG2	EQU	\$008F	;Timer Interrupt Flag 1
0090	TC0	EQU	\$0090	;Timer Input Capture / Output Compare Register 0
0092	TC1	EQU	\$0092	;Timer Input Capture / Output Compare Register 1
0094	TC2	EQU	\$0094	;Timer Input Capture / Output Compare Register 2
0096	TC3	EQU	\$0096	;Timer Input Capture / Output Compare Register 3
0098	TC4	EQU	\$0098	;Timer Input Capture / Output Compare Register 4
009a	TC5	EQU	\$009A	;Timer Input Capture / Output Compare Register 5
009c	TC6	EQU	\$009C	;Timer Input Capture / Output Compare Register 6
009e	TC7	EQU	\$009E	;Timer Input Capture / Output Compare Register 7
00a0	PACTL	EQU	\$00A0	;Pulse Accumulator Control Register
00a2	PACNT	EQU	\$00A2	;Pulse Accumulator Count Register
00ae	PORTT	EQU	\$00AE	;Port T Data Register
00af	DDRT	EQU	\$00AF	;Data Direction Register for Timer Port
f684	PutChar	EQU	\$F684	;Put Character out on Serial Port
f696	Out2Hex	EQU	\$F696	;Output Byte as 2 Hex Characters
f698	Out4Hex	EQU	\$F698	;Output Byte as 4 Hex Characters
f69a	INTSUP	EQU	\$F69A	;Address for D-Bug12 Interrupt Setup
f740	DISPLAY	EQU	\$F740	;Display Scan Subroutine
f790	DISPLYX	EQU	\$F790	;Display Scan Subroutine, X-Points to Data

Courtesy of Dr. Giesselmann

Figure 13.5 Program Timer Registers Equivalent Definitions

The program origin start code controls where in the HC12 micro-controllers memory the executable code is loaded in memory, as shown in Figure 13.5. The memory location \$0D00 is in the HC12's EEPROM.

* Start (ORIGIN) of Code in Memory *				

0d00	ORG	\$0D00	;Origin=Bottom of User EEPROM	

Courtesy of Dr. Giesselmann

Figure 13.6 Program Origin Start Code

The programs precautions and watchdog timer code is shown in Figure 13.7. The watchdog code monitors the program and checks for errors and timeouts that might occur.


```

*****
* First take a few Precautions; Lock in critical System Params *
* Turn on the Watchdog Timer and enable the Clock Monitor Reset *
*****
0d00 cf 0c 00      Start:  LDS    #$0C00      ;Set Stack Pointer
0d03 4c 0c 02      BSET    PUCR,    $02      ;Enable Pull-up Resistors for Port B
0d06 18 0b 08 00 10 MOVW    #$08,    INITRM ;Fix the Position of the RAM (Write Once)
0d0b 18 0b 00 00 11 MOVW    #$00,    INITRG ;Fix the Position of the CPU Regs (Write Once)
0d10 18 0b 01 00 12 MOVW    #$01,    INITEE ;Fix the Position of the EEPROM (Write Once)
0d15 18 0b c1 00 16 MOVW    #$C1,    COPCTL ;Keep the COP turned on ae Once)
0d1a 4c af 60      BSET    DDRT,    $60      ;Make Pins PT5 and PT6 Outputs
0d1d 4d ae 60      BCLR    PORTT,   $60      ;Clear Logic Levels on PT5 and PT6
0d20 18 03 00 00 08 00 MOVW    #$0000, Count ;Clear Runtime Counter
0d26 18 03 00 00 08 02 MOVW    #$0000, DCycle ;Clear DutyCycle Value
0d2c 18 03 00 00 08 04 MOVW    #$0000, ThUp ;Clear Throttle-Up Value
0d32 18 03 00 00 08 06 MOVW    #$0000, Cycles ;Clear Cycles & ResCycl
0d38 d6 01      LDAB    PORTB      ;Load Accu B with Port B
0d3a c4 0f      ANDB    #$0F      ;Mask out lower Nibble
0d3c 26 02      BNE     StCyl      ;Branch to StCyl if not Zero
0d3e c6 01      LDAB    #$01      ;Cycles between Throttle-Up at least 1
0d40 7b 08 06      StCyl: STAB    Cycles ;Initialize Cycles between Throttle-Up
0d43 7b 08 07      STAB    ResCycl ;Initialize 'Restore Cycles' Variable
0d46 d6 01      LDAB    PORTB      ;Load Accu B with Port B
0d48 c4 f0      ANDB    #$F0      ;Mask out higher Nibble
0d4a 54      LSRB      ;Logical Shift Right Port B, mask out high Nibble
0d4b 54      LSRB      ;Logical Shift Right Port B, mask out high Nibble
0d4c 54      LSRB      ;Logical Shift Right Port B, mask out high Nibble
0d4d 54      LSRB      ;Logical Shift Right Port B, mask out high Nibble
0d4e 7b 08 05      STAB    ThUp+1 ;Store Accu B at Throttle-Up Low Byte

```

Courtesy of Dr. GiesseImann

Figure 13.7 Program Precautions and Watchdog Timer Code

The programs external interrupt initialization code tells the HC12 that there is a special interrupt handler, as shown in Figure 13.8. The interrupt is caused by the trigger (gray button) on the HC12 control board. The interrupt starts the code for the 40 ms duration.

```

*****
* Initialize External Interrupt (IRQ) *
*****
0d51 18 03 0e 3d 0b 32 IRQon: MOVW #IRQInt,$B00+(2*25) ;Setup Address for IRQ Interrupt
0d57 4c 1e 80      BSET    INTCR,$80 ;Make IRQ Edge Sensitive

```

Courtesy of Dr. GiesseImann

Figure 13.8 Program External Interrupt Initialization Code

The programs real time interrupt and display initialization code, that the micro-controller will need, is shown in Figure 13.9.

```

*****
* Initialize Real Time Interrupt & Display *
*****
0d5a 4c 02 ff      BSET    DDRA,    $FF      ;Make Port A all Outputs
0d5d 4c 57 f0      BSET    DDRP,    $F0      ;Make High Nibble of Port P all Outputs
0d60 18 03 0e 33 0b 30 MOVW    #RTInt,$B00+(2*24) ;Setup Address for RTI Interrupt
0d66 4c 14 83      BSET    RTICTL,   $83      ;Enable RTI with a Timeout of 4.096ms

```

Courtesy of Dr. GiesseImann

Figure 13.9 Program Real Time Interrupt and Display Initializing Code

The programs analog to digital initialization code, that the micro-controller will need, is shown in Figure 13.10. Since the initial duty

cycle is only changed slowly (by turning a potentiometer on the micro-controller control board), the analog to digital converter is set to be free running, to avoid software overhead.

```
*****
*      Initialize AD Converter      *
*****
0d69 4c 62 80      BSET      ATDCTL2,$80      ;Turn AD-Converter on
0d6c 4c 65 22      BSET      ATDCTL5,$22      ;Turn on Scan Mode, Channel 2
                                                    Courtesy of Dr. Giesselmann
```

Figure 13.10 Program Analog to Digital Converter Initializing Code

The programs timer interrupts initialization code, that the micro-controller will need, is shown in Figure 13.11.

```
*****
*      Initialize Timer Interrupts  *
*****
0d6f 18 03 0d db 0b 22      MOVW      #OC6I,$B00+(2*17) ;Setup Address for Timer Channel 6 Interrupt
0d75 18 03 0e 0e 0b 24      MOVW      #OC5I,$B00+(2*18) ;Setup Address for Timer Channel 5 Interrupt

0d7b 18 03 01 90 00 9e      MOVW      #400,      TC7      ;Load Channel 7 Output Compare Register
0d81 18 03 01 f4 00 9a      MOVW      #500,      TC5      ;Load Channel 5 Output Compare Register
0d87 4c 8d 00      BSET      TMSK2, $00      ;Set Prescaler=1, No Auto Reset
0d8a 4c 80 e0      BSET      TIOS,  $E0      ;Select Channel 5,6,7 Output Compare
0d8d 4c 88 68      BSET      TCTL1, $68      ;Select OC 5 and 6 to Clear associated Pin and OC7 to Toggle
0d90 18 0b 20 00 82      MOVW      #$20,      OC7M      ;OC7 acts on (sets or clears depending on OC7D) PT5
0d95 18 0b 00 00 83      MOVW      #$00,      OC7D      ;OC7 clears PT5
0d9a 10 ef      CLI              ;Clear Interrupt Masking Bit, Interrupts enabled
                                                    Courtesy of Dr. Giesselmann
```

Figure 13.11 Program Timer Interrupts Initializing Code

The interface board monitors the H-Bridge modules for error signals from the integrated drivers and protection circuitry of the IGBT's. The HC12 program monitors the error outputs of the IGBT's and looks for flags sent out by the on board circuitry, as shown in Figure 13.12. Each half bridge module contains on board monitoring circuitry that is designed to send out flag signals if a problem arises. The signals are transmitted through opto-couplers to maintain the optical isolation. The HC12 code will shut off the control signal from the microcontroller if an error is detected.

```
*****
*      Check IGBT Status, Error & OverTemp      *
*****
0d9c 4f ae 01 0c      Wait:      BRCLR     PORTT,$01 IgbtOK ;Branch if Port T0 is clear -> IGBTs OK
0da0 4d 86 80      BCLR      TSCR,  $80      ;Disable Timer System
0da3 4d 8c 60      BCLR      TMSK1, $60      ;Disable Channel 5,6 Interrupts
0da6 4c af 60      BSET      DDRT,  $60      ;Make Pins PT5 and PT6 Outputs
0da9 4d ae 60      BCLR      PORTT, $60      ;Clear Logic Levels on PT5 and PT6
                                                    Courtesy of Dr. Giesselmann
```

Figure 13.12 Program IGBT Status Check Code

The program is designed to run for 40 ms and then shut off, as shown in Figure 13.13.

```

*****
*      Check for Runtime Setting      *
*****
0dac fc 08 00      IgbtOK:  LDD      Count      ;Load Accu D with Runtime Counter
0daf 27 13          BEQ      IniThr      ;Branch to Ini-Throttle if equal to zero
0db1 8c 01 90      CMPD      #400        ;Compare Accu D with 400 = 40ms
0db4 26 19          BNE      WatchD      ;Branch to WatchD(og) if not equal
0db6 4d 86 80      BCLR     TSCR,   $80    ;Disable Timer System
0db9 4d 8c 60      BCLR     TMSK1, $60    ;Disable Channel 5,6 Interrupts
0dbc 4c af 60      BSET     DDRT,   $60    ;Make Pins PT5 and PT6 Outputs
0dbf 4d ae 60      BCLR     PORTT, $60    ;Clear Logic Levels on PT5 and PT6
0dc2 20 0b          BRA      WatchD      ;Branch to WatchD(og)

```

Courtesy of Dr. Giesselmann

Figure 13.13 Program Run time Settings Code

The initial duty cycle is controlled by the dial (potentiometer) on the HC12 control board. The setting of the dial is converted to an 8 bit number, as shown in Figure 13.14.

```

*****
*      Find Initial Throttle Setting  *
*****
0dc4 ce 0e 6e      IniThr:  LDX      #Table      ;Load Table Start into X
0dc7 d6 74          LDAB     ADR2H      ;Load Binary Fraction (AD-Result) into Accu B
0dc9 18 3f 00      ETBL     0,X        ;Look-Up and Interpolate, Result in Accu D
0dcc 7c 08 02      STD      DCycle     ;Store Accu D at DutyCycle Memory Location

```

Courtesy of Dr. Giesselmann

Figure 13.14 Program Initial Duty Cycle Code

The programs watchdog timer service code, that the micro-controller will need, is shown in Figure 13.10.

```

*****
*      Service Watchdog Timer         *
*****
0dcf 18 0b 55 00 17 WatchD: MOVW  #$55,COPRST ;Initiate COP Service
0dd4 18 0b aa 00 17      MOVW  #$AA,COPRST ;Finish COP Service
0dd9 20 c1              BRA     Wait      ;Wait for Interrupts

```

Courtesy of Dr. Giesselmann

Figure 13.15 Program Watchdog Timer Service Code

The interrupt service routine sets up the next high and low transitions of pin PT5 and increments the “cycles” counter for cycles between increase in duty cycles, as shown in Figure 13.16.

```

*****
* Interrupt Service Routine Output Compare 6 Code starts here *
*****
0ddb 18 0b 20 00 82  OC6I:  MOVB  #$20,OC7M      ;OC7 acts on (sets or clears depending on OC7D) PT5
0de0 fc 08 02        LDD    DCycle           ;Load Accu D with Throttle Data
0de3 26 05           BNE    ADJ6              ;Branch to ADJ6 if Accu D is not equal to zero
0de5 79 00 83        CLR    OC7D             ;OC7 sets PT5 Low
0de8 20 05           BRA    ZERO6            ;Branch to ZERO6
0dea 18 0b 20 00 83  ADJ6:  MOVB  #$20,OC7D      ;OC7 sets PT5 High
0def c3 01 90        ZERO6:  ADDD   #400         ;Add 400 to Accu D
0df2 5c 9a           STD    TC5              ;Load Channel 5 Output Compare Register
0df4 18 03 01 8f 00 9e  MOVW  #399,TC7         ;Load Channel 7 Output Compare Register
0dfa 4d 8d 08        BCLR   TMSK2,$08        ;Disable OC7 Auto Reset
0dfd 18 0b 40 00 8e  MOVB  #$40,TFLG1        ;Reset Timer-Flag 6
* Increment Runtime Counter
0e02 fc 08 00        LDD    Count            ;Load Accu D with Runtime Counter
0e05 c3 00 01        ADDD   #001             ;Add 1 to the Count
0e08 7c 08 00        STD    Count            ;Store Accu D to Memory Location Count
0e0b 07 43           BSR    ChkThr           ;Branch to 'Check-Throttle' Subroutine
0e0d 0b             RTI                     ;Return from Interrupt

```

Courtesy of Dr. Giesselmann

Figure 13.16 Program Interrupt Routine Output Compare 6 Code

The next interrupt service routine sets up the next high and low transition of pin PT6, as shown in Figure 13.17

```

*****
* Interrupt Service Routine Output Compare 5 Code starts here *
*****
0e0e 18 0b 40 00 82  OC5I:  MOVB  #$40,OC7M      ;OC7 acts on (sets or clears depending on OC7D) PT6
0e13 fc 08 02        LDD    DCycle           ;Load Accu D with Throttle Data
0e16 26 05           BNE    ADJ5              ;Branch to ADJ5 if Accu D is not equal to zero
0e18 79 00 83        CLR    OC7D             ;OC7 sets PT6 Low
0e1b 20 05           BRA    ZERO5            ;Branch to ZERO5
0e1d 18 0b 40 00 83  ADJ5:  MOVB  #$40,OC7D      ;OC7 sets PT6 High
0e22 5c 9c           STD    TC6              ;Load Channel 6 Output Compare Register
0e24 18 03 03 1f 00 9e  MOVW  #799,TC7         ;Load Channel 7 Output Compare Register
0e2a 4c 8d 08        BSET   TMSK2,$08        ;Enable OC7 Auto Reset
0e2d 18 0b 20 00 8e  MOVB  #$20,TFLG1        ;Reset Timer-Flag 5
0e32 0b             RTI                     ;Return from Interrupt

```

Courtesy of Dr. Giesselmann

Figure 13.17 Program Interrupt Routine Output Compare 5 Code

Each PWM cycle is controlled by a interrupt routine that controls the width of the cycle and adjusts the increase of the PWM for the opposite leg of the H-Bridge, as shown in Figure 13.18. Interrupts were used in the control of the PWM as they can be activated so that no other CPU functions will interrupt the duration of the pulse and the increase of the next pulse. Each PWM cycle is broken into 400 clock cycles (T_s) with the maximum initial duty cycle (D_i) of 308 which works out to a 77% duty cycle. The limitation of a 77% duty cycle comes from the fact that the code needed to advance the duty cycle needs as much as 33% of the duty cycle to operate.

Figure 13.18 Interrupt Routine

The program that controls the output of the initial duty cycle readout is shown in Figure 13.19.

```

*****
* RTI-Interrupt Service Routine Code starts here *
*****
0e33 ce 08 02      RTInt:  LDX    #DCycle      ;Load X-Register with Position of DutyCycle Data
0e36 16 f7 90              JSR    DISPLAYX     ;Call Display Scan Subroutine
0e39 4c 15 80              BSET   RTIFLG, $80   ;Reset RTI-Flag
0e3c 0b              RTI                      ;Return from Interrupt

```

Courtesy of Dr. Giesselmann

Figure 13.19 Program RTI Service Code

The program that controls the interrupt from the start button is shown in Figure 13.20.

```

*****
* IRQ-Interrupt Service Routine Code starts here *
*****
0e3d 4d 1e 40      IRQInt:  BCLR   INTCR, $40   ;Disconnect IRQ Pin
0e40 79 00 14              CLR    RTICTL      ;Disable RTI Interrupt
0e43 79 00 02              CLR    DDRA        ;Make Port A all Inputs; shut off Display
0e46 4d 57 f0              BCLR   DDRP, $F0     ;Make High Nibble of Port P all Inputs
0e49 4c 86 80              BSET   TSCR, $80    ;Enable Timer System
0e4c 4c 8c 60              BSET   TMSK1, $60   ;Enable Channel 5,6 Interrupts
0e4f 0b              RTI                      ;Return from Interrupt

```

Courtesy of Dr. Giesselmann

Figure 13.20 Program IRQ Service Code

The initial duty cycle (D_i) is the starting duty cycle of the IGBT's. Dip switches control the rate at which the duty cycle is increased. Bank 1 controls how much the initial duty cycle (D_i) is increased with a range of 0-15. Bank 2 controls how often the increase takes place with a range of 0-15. The Dip settings are listed as X/Y with X stating the setting of bank 2 and Y stating the setting of of bank 1. The HC12 increase in duty

cycle is shown in Figure 13.21.

```
*****
*      Check for and Perform Throttle-Up      *
*****
0e50 73 08 06      ChkThr:  DEC      Cycles      ;Decrement 'Cycles between Throttle-Up' Counter
0e53 27 01          BEQ      UpTrot          ;Branch to Throttle up if zero
0e55 3d              RTS              ;Early Return from Throttle-Up Subroutine
*      Restore Cycles      *
0e56 18 0c 08 07 08 06 UpTrot: MOVb  ResCycl  Cycles ;Restore 'Cycles between Throttle-Up'
*      Throttle-Up      *
0e5c fc 08 02          LDD      DCycle          ;Load Accu D with DutyCycle
0e5f f3 08 04          ADDD      ThUp          ;Add Increment to Throttle setting
0e62 8c 01 34          CMPD      #0308          ;Compare Accu D with 308 dec
0e65 23 03          BLS      LS308          ;Branch if Less or Same
0e67 cc 01 34          LDD      #308          ;Load Accu D with max. Throttle Value
0e6a 7c 08 02      LS308:  STD      DCycle          ;Store DutyCycle Value
0e6d 3d              RTS              ;Return from Throttle-Up Subroutine
                                         Courtesy of Dr. Giesselmann
```

Figure 13.21 Program Duty Cycle Increase Code

The duty cycle look up table, is shown in Figure 13.22. This table converts the data range from 0-255 to 0-310. The range of 0-255 corresponds to the output of the 8 Bit analog to digital converter.

```
*****
*      Throttle Lookup Table for ETBL      *
*****
0e6e 00 00      Table:  FDB      000          ;Zero Power
0e70 01 36          FDB      310          ;Full Power
                                         Courtesy of Dr. Giesselmann
```

Figure 13.22 Program Duty Cycle Look up Table

The variables in the program change often and need to be stored in RAM. This section of code points the data to RAM instead of EEPROM, as shown in Figure 13.23.

```
*****
*      Place for Variables in Memory      *
*****
0800          ORG      $0800          ;Origin=Bottom of User RAM
0800          Count:   RMB      2          ;Reserve 2 Bytes of Memory for Runtime Counter
0802          DCycle:  RMB      2          ;Reserve 2 Bytes of Memory for Throttle Setting
0804          ThUp:    RMB      2          ;Reserve 2 Bytes of Memory for # of Duty Cycle Increments
0806          Cycles:  RMB      1          ;Reserve 1 Byte of Memory for # of 'Cycles between Throttle-Up'
0807          ResCycl: RMB      1          ;Reserve 1 Byte of Memory for # of 'Cycles between Throttle-Up'
Total errors: 0
Total warnings: 0
                                         Courtesy of Dr. Giesselmann
```

Figure 13.23 Program Variable Locations in Memory Definitions

CHAPTER 14

CONCLUSION

The goal of this thesis was to design and construct a compact power supply (to eventually drive a pulsed microwave source), able to charge a 6.6 μF capacitor to 30 kV in 40 ms. Ultimately the DC source will be a thermal battery. The use of the variac stack in place of the thermal battery allowed extensive testing to determine the parameters of the experiment.

Experimentation has shown that the overall size of the project can be greatly reduced. A single H-Bridge might be able to charge the 6.6 μF load capacitor. The current and voltage on shot 57 are near or below the 1200 A @ 1200 V ceiling of the H-Bridge. Further manipulation of the dip switch setting and the initial duty cycle might be able to lower the voltage and current. The input capacitors can be greatly reduced, advancements in capacitor design have produced capacitors that are much smaller than the capacitors used, as shown in Figure 14.1 and Table 14.1. The new capacitors occupy 14% of the volume of the old capacitors. The new capacitors are designed to be mounted on printed circuit boards which can be used to connect the capacitors to the bus bars. The protective resistors can also be mounted directly on the circuit board making for a very compact input capacitor module. Modification in the code running the micro-controller will improve the efficiency of the charging. The program that was run in the experiment was limited to a maximum duty cycle of 77% due to limitations in the micro-controller logic. A new code storing in flash EEPROM will give that is included in the Appendix should allow a maximum duty cycle of 83%.

Figure 14.1 Capacitor Comparison

Table 14.1 Capacitor Parameters

	Old Capacitor	New Capacitor
Voltage	450 V	450 V
Capacitance	1.50E-03 F	1.20E-03 F
Energy	151.88 J	121.50 J
Height	14.50 cm	7.76 cm
Diameter	9.36 cm	4.80 cm
Volume	997.22 cm ³	140.35 cm ³
Energy Density	0.15 J/cm ³	0.87 J/cm ³

The experiment proved that a 6.6 μF capacitor can be charged to 30 kV from a thermal battery in 30 ms. Additional testing needs to be done to refine the process and reduce the overall size but the concept has been proven. The knowledge and understanding that has been gained from this design will allow for a new design that could fit into a large suitcase.

REFERENCES

- Giesselmann, M., Kristiansen, E., "Design of a 30 kV Power Supply for Capacitor Charging using short Duty Burst Mode," Proceedings of the 12th IEEE International Pulsed Power Conference, Monterey, California, June 27-30, 1999.
- Mohan, N., Robbins, W., Undeland, T., Power Electronics, Converters, Applications and Design, 2nd edition, ISBN 0-471-58408-8. John Wiley & Sons, INC., New York pp. 189, 1995
- Motorola Corporation "<http://www.motorola.com/>." Phoenix, Arizona
- Sensitron "<http://www.sensitron.com/Snubber.htm>." Sensitron, Deer Park, NY., Available: 6/6/00
- Semikron, Inc. "<http://www.semikron.com/>." Semikron Integrated Intelligent Power Pack, IGBT Datasheet. Hudson, New Hampshire.
- Steeg, T, "Selecting optimum electrolytic capacitors requires an understanding of their characteristics and technology." PCIM Power Electronics Systems pp. 38-55, Adams/Intertec International Inc. Solon, OH., June 2000.
- Tektronix User Manual, "TDS420A, TDS430A, TDS460A & TDS 510A Digitizing Oscilloscopes 070-9701-01." Wilsonville, OR. pp 3-36, 3-58
- Mohan, N., Robbins, W., Undeland, T., Power Electronics, Converters, Applications and Design, 2nd edition, ISBN 0-471-58408-8. John Wiley & Sons, INC., New York pp. 189, 1995

APPENDIX A
STANDARD PROGRAM


```

*****
*   Program to produce PWM Signals for 30 kV Rapid Charger   *
*   Written for Motorola M68EVB912B32 Eval Board           *
*   The Program uses the Output Compare 7 Function of the Timers *
*   The Program creates 10 kHz alternating Signals to drive a H-Bridge *
*   The Signals are provided at PT5 and PT6                 *
*   The low Nibble of the DIP Switches is the number of cycles between *
*   Duty Cycle increments. The High Nibble is the number to increment D *
*   IRQ-Switch turns the System on, XIRQ turns it off       *
*   Program uses Real Time Interrupt for Display Routine    *
*   PORT A controls Segm. A-G,dp, High Nibble of PORT P controls Digits *
*   Only the High Nibble of PORT P is written to by the Display Routine *
*   The Display Subroutine is burned into Flash-EEPROM      *
*   The Program uses the Extended Table Lookup Function to Scale the *
*   AD-Converter Output from 0-255 to 0-400                 *
*   ETBL Linearly Interpolates one of 256 result values that fall between *
*   each pair of data entries in a lookup table stored in memory *
*   X points to lower table entry, B holds binary fraction of XL location *
*   The formula for B is given below. The radix point of B is left of MSB *
*    $D = Y1 + [(B) \times (Y2 - Y1)], (B) = (XL - X1) / (X2 - X1)$  *
*   Written for AS12 Assembler, March 08, 2000, by Michael Giesselmann *
*****
      NAM      30kVf.asm
*****
*   68HC12 D-Bug 12 Callable Routines *
*   HC12 Regs and other Equivalents *
*****
0000      PORTA      EQU      $0000      ;Port A Register of HC12
0001      PORTB      EQU      $0001      ;Port B Register of HC12
0002      DDRA       EQU      $0002      ;Data Direction Register Port A
0003      DDRB       EQU      $0003      ;Data Direction Register Port B
000c      PUCR        EQU      $000C      ;Pull Up Resistor Register Port A,B,E
0010      INTRM       EQU      $0010      ;RAM Position Register
0011      INITRG      EQU      $0011      ;CPU Reg Position Register
0012      INITEE      EQU      $0012      ;EEPROM Position Register
0014      RTICTL      EQU      $0014      ;Real Time Interrupt Control Register
0015      RTIFLG      EQU      $0015      ;Real Time Interrupt Flag Register
0016      COPCTL      EQU      $0016      ;Watchdog Timer Control Register
0017      COPRST      EQU      $0017      ;Watchdog Timer Reset Register
001e      INTCR        EQU      $001E      ;Interrupt Control Register
***** PWM Control *****
0040      PWCLK       EQU      $0040      ;PWM Clocks and Concatenate
0041      WPOL        EQU      $0041      ;PWM Clock Select and Polarity
0042      PWEN        EQU      $0042      ;PWM Enable Register
0044      PWSCAL0     EQU      $0044      ;PWM Scale Register 0, Channel 0/1
0046      PWSCAL1     EQU      $0046      ;PWM Scale Register 1, Channel 2/3
004c      PWPER0      EQU      $004C      ;PWM Period Register Channel 0
004d      PWPER1      EQU      $004D      ;PWM Period Register Channel 1
004e      PWPER2      EQU      $004E      ;PWM Period Register Channel 2
004f      PWPER3      EQU      $004F      ;PWM Period Register Channel 3
0050      PWDY0       EQU      $0050      ;PWM Duty Register Channel 0
0051      PWDY1       EQU      $0051      ;PWM Duty Register Channel 1
0052      PWDY2       EQU      $0052      ;PWM Duty Register Channel 2
0053      PWDY3       EQU      $0053      ;PWM Duty Register Channel 3
0054      PWCTL       EQU      $0054      ;PWM Control Register
0056      PORTP       EQU      $0056      ;Port P Data Register
0057      DDRP        EQU      $0057      ;Port P Data Direction Register
***** AD Control *****
0062      ATDCTL2     EQU      $0062      ;ATD Control Register 2
0065      ATDCTL5     EQU      $0065      ;ATD Control Register 5
006f      PORTAD      EQU      $006F      ;Port AD Input Register
0070      ADR0H       EQU      $0070      ;ATD Converter Result Register 0
0072      ADR1H       EQU      $0072      ;ATD Converter Result Register 1
0074      ADR2H       EQU      $0074      ;ATD Converter Result Register 2
***** Timer Registers *****
0080      TIOS        EQU      $0080      ;Timer Input Capture, Output Compare Select
0081      CFORC       EQU      $0081      ;Timer Compare Force Register
0082      OC7M        EQU      $0082      ;Output Compare 7 Mask Register
0083      OC7D        EQU      $0083      ;Output Compare 7 Data Register
0084      TCNT        EQU      $0084      ;16 Bit Free Running Counter
0086      TSCR        EQU      $0086      ;Timer System Control Register
0088      TCTL1       EQU      $0088      ;Timer Control Register 1
0089      TCTL2       EQU      $0089      ;Timer Control Register 2
008a      TCTL3       EQU      $008A      ;Timer Control Register 3
008b      TCTL4       EQU      $008B      ;Timer Control Register 4

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008c      TMSK1      EQU      $008C      ;Timer Mask 1
008d      TMSK2      EQU      $008D      ;Timer Mask 2
008e      TFLG1      EQU      $008E      ;Timer Interrupt Flag 1
008f      TFLG2      EQU      $008F      ;Timer Interrupt Flag 1
0090      TC0        EQU      $0090      ;Timer Input Capture / Output Compare Register 0
0092      TC1        EQU      $0092      ;Timer Input Capture / Output Compare Register 1
0094      TC2        EQU      $0094      ;Timer Input Capture / Output Compare Register 2
0096      TC3        EQU      $0096      ;Timer Input Capture / Output Compare Register 3
0098      TC4        EQU      $0098      ;Timer Input Capture / Output Compare Register 4
009a      TC5        EQU      $009A      ;Timer Input Capture / Output Compare Register 5
009c      TC6        EQU      $009C      ;Timer Input Capture / Output Compare Register 6
009e      TC7        EQU      $009E      ;Timer Input Capture / Output Compare Register 7
00a0      PACTL      EQU      $00A0      ;Pulse Accumulator Control Register
00a2      PACNT      EQU      $00A2      ;Pulse Accumulator Count Register
00ae      PORTT      EQU      $00AE      ;Port T Data Register
00af      DDRT       EQU      $00AF      ;Data Direction Register for Timer Port
f684      PutChar    EQU      $F684      ;Put Character out on Serial Port
f696      Out2Hex    EQU      $F696      ;Output Byte as 2 Hex Characters
f698      Out4Hex    EQU      $F698      ;Output Byte as 4 Hex Characters
f69a      INTSUP     EQU      $F69A      ;Address for D-Bug12 Interrupt Setup
f740      DISPLAY    EQU      $F740      ;Display Scan Subroutine
f790      DISPLYX    EQU      $F790      ;Display Scan Subroutine, X-Points to Data
*****
*      Start (ORIGIN) of Code in Memory      *
*****
0d00      ORG        $0D00      ;Origin=Bottom of User EEPROM
*****
* First take a few Precautions; Lock in critical System Params *
* Turn on the Watchdog Timer and enable the Clock Monitor Reset *
*****
0d00 cf 0c 00      Start:      LDS      #$0C00      ;Set Stack Pointer
0d03 4c 0c 02      BSET      PUCR,    $02      ;Enable Pull-up Resistors for Port B
0d06 18 0b 08 00 10      MOVW     #$08,    INITRM    ;Fix the Position of the RAM (Write Once)
0d0b 18 0b 00 00 11      MOVW     #$00,    INITRG    ;Fix the Position of the CPU Regs (Write Once)
0d10 18 0b 01 00 12      MOVW     #$01,    INITEE    ;Fix the Position of the EEPROM (Write Once)
0d15 18 0b c1 00 16      MOVW     #$C1,    COPCTL    ;Keep the COP turned on ae Once)
0d1a 4c af 60      BSET      DDRT,    $60      ;Make Pins PT5 and PT6 Outputs
0d1d 4d ae 60      BCLR      PORTT,   $60      ;Clear Logic Levels on PT5 and PT6
0d20 18 03 00 00 08 00      MOVW     #$0000,   Count    ;Clear Runtime Counter
0d26 18 03 00 00 08 02      MOVW     #$0000,   DCycle   ;Clear DutyCycle Value
0d2c 18 03 00 00 08 04      MOVW     #$0000,   ThUp    ;Clear Throttle-Up Value
0d32 18 03 00 00 08 06      MOVW     #$0000,   Cycles   ;Clear Cycles & ResCycl
0d38 d6 01      LDAB      PORTB      ;Load Accu B with Port B
0d3a c4 0f      ANDB      #$0F      ;Mask out lower Nibble
0d3c 26 02      BNE       StCyl      ;Branch to StCyl if not Zero
0d3e c6 01      LDAB      #$01      ;Cycles beteen Throttle-Up at least 1
0d40 7b 08 06      StCyl:      STAB     Cycles    ;Initialize Cycles between Throttle-Up
0d43 7b 08 07      STAB     ResCycl   ;Initialize 'Restore Cycles' Variable
0d46 d6 01      LDAB      PORTB      ;Load Accu B with Port B
0d48 c4 f0      ANDB      #$F0      ;Mask out higher Nibble
0d4a 54      LSRB      ;Logical Shift Right Port B, mask out high Nibble
0d4b 54      LSRB      ;Logical Shift Right Port B, mask out high Nibble
0d4c 54      LSRB      ;Logical Shift Right Port B, mask out high Nibble
0d4d 54      LSRB      ;Logical Shift Right Port B, mask out high Nibble
0d4e 7b 08 05      STAB     ThUp+1    ;Store Accu B at Throttle-Up Low Byte
*****
*      Initialize External Interrupt (IRQ)      *
*****
0d51 18 03 0e 3d 0b 32      IRQon:  MOVW     #IRQInt,$B00+(2*25) ;Setup Address for IRQ Interrupt
0d57 4c 1e 80      BSET      INTCR,$80      ;Make IRQ Edge Sensitive
*****
*      Initialize Real Time Interrupt & Display      *
*****
0d5a 4c 02 ff      BSET      DDRA,    $FF      ;Make Port A all Outputs
0d5d 4c 57 f0      BSET      DDRP,    $F0      ;Make High Nibble of Port P all Outputs
0d60 18 03 0e 33 0b 30      MOVW     #RTInt,$B00+(2*24) ;Setup Address for RTI Interrupt
0d66 4c 14 83      BSET      RTICTL,   $83      ;Enable RTI with a Timeout of 4.096ms
*****
*      Initialize AD Converter      *
*****
0d69 4c 62 80      BSET      ATDCTL2,$80      ;Turn AD-Converter on
0d6c 4c 65 22      BSET      ATDCTL5,$22      ;Turn on Scan Mode, Channel 2
*****
*      Initialize Timer Interrupts      *
*****
0d6f 18 03 0d db 0b 22      MOVW     #OC6I,$B00+(2*17) ;Setup Address for Timer Channel 6 Interrupt
0d75 18 03 0e 0e 0b 24      MOVW     #OC5I,$B00+(2*18) ;Setup Address for Timer Channel 5 Interrupt

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0d7b 18 03 01 90 00 9e      MOVW    #400,    TC7      ;Load Channel 7 Output Compare Register
0d81 18 03 01 f4 00 9a      MOVW    #500,    TC5      ;Load Channel 5 Output Compare Register
0d87 4c 8d 00                BSET     TMSK2,    $00      ;Set Prescaler=1, No Auto Reset
0d8a 4c 80 e0                BSET     TIOS,     $E0      ;Select Channel 5.6.7 Output Compare
0d8d 4c 88 68                BSET     TCTL1,    $68      ;Select OC 5 and 6 to Clear associated Pin and OC7 to Toggle
0d90 18 0b 20 00 82          MOVW    #500,    OC7M      ;OC7 acts on (sets or clears depending on OC7D) PT5
0d95 18 0b 00 00 83          MOVW    #500,    OC7D      ;OC7 clears PT5
0d9a 10 ef                  CLI                      ;Clear Interrupt Masking Bit. Interrupts enabled
*****
*      Start of Main Program Loop      *
*****
*      Check IGBT Status, Error & OverTemp      *
*****
0d9c 4f ae 01 0c      Wait:  BRCLR PORTT,$01 IgbtOK      ;Branch if Port T0 is clear -> IGBTs OK
0da0 4d 86 80          BCLR     TSCR,     $80      ;Disable Timer System
0da3 4d 8c 60          BCLR     TMSK1,    $60      ;Disable Channel 5,6 Interrupts
0da6 4c af 60          BSET     DDRT,     $60      ;Make Pins PT5 and PT6 Outputs
0da9 4d ae 60          BCLR     PORTT,    $60      ;Clear Logic Levels on PT5 and PT6
*****
*      Check for Runtime Setting      *
*****
0dac fc 08 00      IgbtOK:  LDD      Count          ;Load Accu D with Runtime Counter
0daf 27 13          BEQ      IniThr          ;Branch to Ini-Throttle if equal to zero
0db1 8c 01 90          CMPD     #400          ;Compare Accu D with 400 = 40ms
0db4 26 19          BNE      WatchD          ;Branch to WatchD(og) if not equal
0db6 4d 86 80          BCLR     TSCR,     $80      ;Disable Timer System
0db9 4d 8c 60          BCLR     TMSK1,    $60      ;Disable Channel 5,6 Interrupts
0dbc 4c af 60          BSET     DDRT,     $60      ;Make Pins PT5 and PT6 Outputs
0dbf 4d ae 60          BCLR     PORTT,    $60      ;Clear Logic Levels on PT5 and PT6
0dc2 20 0b          BRA      WatchD          ;Branch to WatchD(og)
*****
*      Find Initial Throttle Setting      *
*****
0dc4 ce 0e 6e      IniThr:  LDX      #Table          ;Load Table Start into X
0dc7 d6 74          LDAB     ADR2H          ;Load Binary Fraction (AD-Result) into Accu B
0dc9 18 3f 00          ETBL     0,X          ;Look-Up and Interpolate, Result in Accu D
0dcc 7c 08 02          STD      DCycle          ;Store Accu D at DutyCycle Memory Location
*****
*      Service Watchdog Timer      *
*****
0dcf 18 0b 55 00 17      WatchD: MOVW    #55,COPRST      ;Initiate COP Service
0dd4 18 0b aa 00 17          MOVW    #AA,COPRST      ;Finish COP Service
0dd9 20 c1          BRA      Wait          ;Wait for Interrupts
*****
*      End of Main Program Loop      *
*****

*****
* Interrupt Service Routine Output Compare 6 Code starts here *
*****
0ddb 18 0b 20 00 82      OC6I:  MOVW    #500,    OC7M      ;OC7 acts on (sets or clears depending on OC7D) PT5
0de0 fc 08 02          LDD      DCycle          ;Load Accu D with Throttle Data
0de3 26 05          BNE      ADJ6          ;Branch to ADJ6 if Accu D is not equal to zero
0de5 79 00 83          CLR      OC7D          ;OC7 sets PT5 Low
0de8 20 05          BRA      ZERO6          ;Branch to ZERO6
0dea 18 0b 20 00 83      ADJ6:  MOVW    #500,    OC7D      ;OC7 sets PT5 High
0def c3 01 90      ZERO6:  ADDD     #400          ;Add 400 to Accu D
0df2 5c 9a          STD      TC5          ;Load Channel 5 Output Compare Register
0df4 18 03 01 8f 00 9e      MOVW    #399,TC7      ;Load Channel 7 Output Compare Register
0dfa 4d 8d 08          BCLR     TMSK2,$08      ;Disable OC7 Auto Reset
0dfd 18 0b 40 00 8e          MOVW    #500,TFLG1      ;Reset Timer-Flag 6
*      Increment Runtime Counter
0e02 fc 08 00          LDD      Count          ;Load Accu D with Runtime Counter
0e05 c3 00 01          ADDD     #001          ;Add 1 to the Count
0e08 7c 08 00          STD      Count          ;Store Accu D to Memory Location Count
0e0b 07 43          BSR      ChkThr          ;Branch to 'Check-Throttle' Subroutine
0e0d 0b          RTI          ;Return from Interrupt
*****
* Interrupt Service Routine Output Compare 5 Code starts here *
*****
0e0e 18 0b 40 00 82      OC5I:  MOVW    #500,    OC7M      ;OC7 acts on (sets or clears depending on OC7D) PT6
0e13 fc 08 02          LDD      DCycle          ;Load Accu D with Throttle Data
0e16 26 05          BNE      ADJ5          ;Branch to ADJ5 if Accu D is not equal to zero
0e18 79 00 83          CLR      OC7D          ;OC7 sets PT6 Low
0e1b 20 05          BRA      ZERO5          ;Branch to ZERO5
0e1d 18 0b 40 00 83      ADJ5:  MOVW    #500,    OC7D      ;OC7 sets PT6 High
0e22 5c 9c      ZERO5:  STD      TC6          ;Load Channel 6 Output Compare Register

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0e24 18 03 03 1f 00 9e      MOVW    #799,TC7      ;Load Channel 7 Output Compare Register
0e2a 4c 8d 08                BSET    TMSK2,$08     ;Enable OC7 Auto Reset
0e2d 18 0b 20 00 8e          MOVW    #520,TFLG1    ;Reset Timer-Flag 5
0e32 0b                      RTI                          ;Return from Interrupt
*****
* RTI-Interrupt Service Routine Code starts here *
*****
0e33 ce 08 02      RTInt:  LDW      #DCycle      ;Load X-Register with Position of DutyCycle Data
0e36 16 f7 90      JSR      DISPLYX      ;Call Display Scan Subroutine
0e39 4c 15 80      BSET    RTIFLG, $80      ;Reset RTI-Flag
0e3c 0b            RTI                          ;Return from Interrupt
*****
* IRQ-Interrupt Service Routine Code starts here *
*****
0e3d 4d 1e 40      IRQInt: BCLR    INTCR, $40      ;Disconnect IRQ Pin
0e40 79 00 14      CLR      RTICTL      ;Disable RTI Interrupt
0e43 79 00 02      CLR      DDRA        ;Make Port A all Inputs; shut off Display
0e46 4d 57 f0      BCLR    DDRP, $F0      ;Make High Nibble of Port P all Inputs
0e49 4c 86 80      BSET    TSCR, $80      ;Enable Timer System
0e4c 4c 8c 60      BSET    TMSK1, $60     ;Enable Channel 5,6 Interrupts
0e4f 0b            RTI                          ;Return from Interrupt
*****
* Check for and Perform Throttle-Up *
*****
0e50 73 08 06      ChkThr: DEC     Cycles      ;Decrement 'Cycles between Throttle-Up' Counter
0e53 27 01          BEQ     UpTrot      ;Branch to Throttle up if zero
0e55 3d            RTS                  ;Early Return from Throttle-Up Subroutine
* Restore Cycles *
0e56 18 0c 08 07 08 06 UpTrot: MOVW    ResCycl Cycles ;Restore 'Cycles between Throttle-Up'
* Throttle-Up *
0e5c fc 08 02      LDD      DCycle      ;Load Accu D with DutyCycle
0e5f f3 08 04      ADDD     ThUp        ;Add Increment to Throttle setting
0e62 8c 01 34      CMPD     #0308      ;Compare Accu D with 308 dec
0e65 23 03          BLS      LS308      ;Branch if Less or Same
0e67 cc 01 34      LDD      #308        ;Load Accu D with max. Throttle Value
0e6a 7c 08 02      LS308: STD      DCycle      ;Store DutyCycle Value
0e6d 3d            RTS                  ;Return from Throttle-Up Subroutine
*****
* Throttle Lookup Table for ETBL *
*****
0e6e 00 00      Table:  FDB      000      ;Zero Power
0e70 01 36      FDB      310      ;Full Power
*****
* Place for Variables in Memory *
*****
0800      ORG      $0800      ;Origin=Bottom of User RAM
0800      Count:   RMB      2      ;Reserve 2 Bytes of Memory for Runtime Counter
0802      DCycle:  RMB      2      ;Reserve 2 Bytes of Memory for Throttle Setting
0804      ThUp:    RMB      2      ;Reserve 2 Bytes of Memory for # of Duty Cycle Increments
0806      Cycles:  RMB      1      ;Reserve 1 Byte of Memory for # of 'Cycles between Throttle-
Up'
0807      ResCycl: RMB      1      ;Reserve 1 Byte of Memory for # of 'Cycles between Throttle-
Up'
Total errors: 0
Total warnings: 0

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APPENDIX B
PROGRAM IN FLASH EEPROM

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*****
*   Program to produce PWM Signals for 30 kV Rapid Charger   *
*   Written for Motorola M68EVB912B32 Eval Board           *
*   The Program uses the Output Compare 7 Function of the Timers *
*   The Program creates 10 kHz alternating Signals to drive a H-Bridge *
*       The Signals are provided at PT5 and PT6             *
*   The low Nibble of the DIP Switches is the number of cycles between *
*   Duty Cycle increments. The High Nibble is the number to increment D *
*   IRQ-Switch turns the System on, XIRQ turns it off      *
*   Program uses Real Time Interrupt for Display Routine   *
*   PORT A controls Segm. A-G,dp, High Nibble of PORT P controls Digits *
*   Only the High Nibble of PORT P is written to by the Display Routine *
*       The Display Subroutine is burned into Flash-EEPROM *
*   The Program uses the Extended Table Lookup Function to Scale the *
*       AD-Converter Output from 0-255 to 0-400             *
*   ETBL Linearly Interpolates one of 256 result values that fall between *
*       each pair of data entries in a lookup table stored in memory *
*   X points to lower table entry, B holds binary fraction of XL location *
*   The formula for B is given below. The radix point of B is left of MSB *
*        $D = Y1 + [(B) \times (Y2 - Y1)], (B) = (XL - X1) / (X2 - X1)$  *
*   Written for AS12 Assembler, June 17, 2000, by Michael Giesselmann *
*       Written for Flash EEPROM Auto-Start                 *
*****

NAM    FlashEE.asm
*****
* 68HC12 D-Bug 12 Callable Routines *
* HC12 Regs and other Equivalents *
*****

0000    PORTA EQU    $0000 ;Port A Register of HC12
0001    PORTB EQU    $0001 ;Port B Register of HC12
0002    DDRA EQU     $0002 ;Data Direction Register Port A
0003    DDRB EQU     $0003 ;Data Direction Register Port B
000c    PUCR EQU     $000C ;Pull Up Resistor Register Port A,B,E
0010    INITRM EQU    $0010 ;RAM Position Register
0011    INITRG EQU    $0011 ;CPU Reg Position Register
0012    INITEE EQU    $0012 ;EEPROM Position Register
0014    RTICTL EQU    $0014 ;Real Time Interrupt Control Register
0015    RTIFLG EQU    $0015 ;Real Time Interrupt Flag Register
0016    COPCTL EQU    $0016 ;Watchdog Timer Control Register
0017    COPRST EQU    $0017 ;Watchdog Timer Reset Register
001e    INTCR EQU     $001E ;Interrupt Control Register
***** PWM Control *****
0040    PWCLK EQU     $0040 ;PWM Clocks and Concatenate
0041    PWPOL EQU     $0041 ;PWM Clock Select and Polarity
0042    PWEN EQU      $0042 ;PWM Enable Register
0044    PWSCAL0 EQU    $0044 ;PWM Scale Register 0, Channel 0/1
0046    PWSCAL1 EQU    $0046 ;PWM Scale Register 1, Channel 2/3
004c    PWPER0 EQU     $004C ;PWM Period Register Channel 0
004d    PWPER1 EQU     $004D ;PWM Period Register Channel 1
004e    PWPER2 EQU     $004E ;PWM Period Register Channel 2
004f    PWPER3 EQU     $004F ;PWM Period Register Channel 3
0050    PWDTY0 EQU     $0050 ;PWM Duty Register Channel 0
0051    PWDTY1 EQU     $0051 ;PWM Duty Register Channel 1
0052    PWDTY2 EQU     $0052 ;PWM Duty Register Channel 2
0053    PWDTY3 EQU     $0053 ;PWM Duty Register Channel 3
0054    PWCTL EQU      $0054 ;PWM Control Register
0056    PORTP EQU     $0056 ;Port P Data Register
0057    DDRP EQU       $0057 ;Port P Data Direction Register
***** AD Control *****
0062    ATDCTL2 EQU    $0062 ;ATD Control Register 2
0065    ATDCTL5 EQU    $0065 ;ATD Control Register 5
006f    PORTAD EQU     $006F ;Port AD Input Register
0070    ADR0H EQU      $0070 ;ATD Converter Result Register 0
0072    ADR1H EQU      $0072 ;ATD Converter Result Register 1
0074    ADR2H EQU      $0074 ;ATD Converter Result Register 2
***** Timer Registers *****
0080    TIOS EQU       $0080 ;Timer Input Capture, Output Compare Select
0081    CFORC EQU       $0081 ;Timer Compare Force Register
0082    OC7M EQU        $0082 ;Output Compare 7 Mask Register
0083    OC7D EQU        $0083 ;Output Compare 7 Data Register
0084    TCNT EQU        $0084 ;16 Bit Free Running Counter
0086    TSCR EQU        $0086 ;Timer System Control Register
0088    TCTL1 EQU       $0088 ;Timer Control Register 1
0089    TCTL2 EQU       $0089 ;Timer Control Register 2

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008a      TCTL3 EQU $008A ;Timer Control Register 3
008b      TCTL4 EQU $008B ;Timer Control Register 4
008c      TMSK1 EQU $008C ;Timer Mask 1
008d      TMSK2 EQU $008D ;Timer Mask 2
008e      TFLG1 EQU $008E ;Timer Interrupt Flag 1
008f      TFLG2 EQU $008F ;Timer Interrupt Flag 1
0090      TC0 EQU $0090 ;Timer Input Capture / Output Compare Register 0
0092      TC1 EQU $0092 ;Timer Input Capture / Output Compare Register 1
0094      TC2 EQU $0094 ;Timer Input Capture / Output Compare Register 2
0096      TC3 EQU $0096 ;Timer Input Capture / Output Compare Register 3
0098      TC4 EQU $0098 ;Timer Input Capture / Output Compare Register 4
009a      TC5 EQU $009A ;Timer Input Capture / Output Compare Register 5
009c      TC6 EQU $009C ;Timer Input Capture / Output Compare Register 6
009e      TC7 EQU $009E ;Timer Input Capture / Output Compare Register 7
00a0      PACTL EQU $00A0 ;Pulse Accumulator Control Register
00a2      PACNT EQU $00A2 ;Pulse Accumulator Count Register
00ae      PORTT EQU $00AE ;Port T Data Register
00af      DDRT EQU $00AF ;Data Direction Register for Timer Port
f684      PutChar EQU $F684 ;Put Character out on Serial Port
f696      Out2Hex EQU $F696 ;Output Byte as 2 Hex Characters
f698      Out4Hex EQU $F698 ;Output Byte as 4 Hex Characters
f69a      INTSUP EQU $F69A ;Address for D-Bug12 Interrupt Setup
f740      DISPLAY EQU $F740 ;Display Scan Subroutine
f790      DISPLYX EQU $F790 ;Display Scan Subroutine, X-Points to Data

*****
* Place for Variables in Memory *
*****
0800      ORG $0800 ;Origin=Bottom of User RAM
0800      Count: RMB 2 ;Reserve 2 Bytes of Memory for Runtime Counter
0802      DCycle: RMB 2 ;Reserve 2 Bytes of Memory for Throttle Setting
0804      ThUp: RMB 2 ;Reserve 2 Bytes of Memory for # of Duty Cycle Increments
0806      Cycles: RMB 1 ;Reserve 1 Byte of Memory for # of 'Cycles between Throttle-Up'
0807      ResCycl: RMB 1 ;Reserve 1 Byte of Memory for # of 'Cycles between Throttle-Up'
*****
* Reserve Memory for Display variable *
*****
09fe      ORG $09FE ;Top of User RAM
09fe      Display: RMB 2 ;Reserve 2 Bytes of Memory for Display Bytes

*****
* Start (ORIGIN) of Code in Memory *
*****
8000      ORG $8000 ;Origin=Bottom of Flash EEPROM
*****
* First take a few Precautions; Lock in critical System Params *
* Turn on the Watchdog Timer and enable the Clock Monitor Reset *
*****
8000 cf 0c 00      Start: LDS #0C00 ;Set Stack Pointer
8003 4c 0c 02      BSET PUCR, $02 ;Enable Pull-up Resistors for Port B
8006 18 0b 08 00 10      MOVB #08, INITRM ;Fix the Position of the RAM (Write Once)
800b 18 0b 00 00 11      MOVB #00, INITRG ;Fix the Position of the CPU Regs (Write Once)
8010 18 0b 01 00 12      MOVB #01, INITEE ;Fix the Position of the EEPROM (Write Once)
8015 18 0b c1 00 16      MOVB #C1, COPCTL ;Keep the COP turned on and te Once)
801a 4c af 60      BSET DDRT, $60 ;Make Pins PT5 and PT6 Outputs
801d 4d ae 60      BCLR PORTT, $60 ;Clear Logic Levels on PT5 and PT6
8020 18 03 00 00 08 00      MOVW #0000, Count ;Clear Runtime Counter
8026 18 03 00 00 08 02      MOVW #0000, DCycle ;Clear DutyCycle Value
802c 18 03 00 00 08 04      MOVW #0000, ThUp ;Clear Throttle-Up Value
8032 18 03 00 00 08 06      MOVW #0000, Cycles ;Clear Cycles & ResCycl
8038 d6 01      LDAB PORTB ;Load Accu B with Port B
803a c4 0f      ANDB #0F ;Mask out lower Nibble
803c 26 02      BNE StCyl ;Branch to StCyl if not Zero
803e c6 01      LDAB #01 ;Cycles beteen Throttle-Up at least 1
8040 7b 08 06      StCyl: STAB Cycles ;Initialize Cycles between Throttle-Up
8043 7b 08 07      STAB ResCycl ;Initialize 'Restore Cycles' Variable
8046 d6 01      LDAB PORTB ;Load Accu B with Port B
8048 c4 f0      ANDB #F0 ;Mask out higher Nibble
804a 54      LSRB ;Logical Shift Right Port B, mask out high Nibble
804b 54      LSRB ;Logical Shift Right Port B, mask out high Nibble
804c 54      LSRB ;Logical Shift Right Port B, mask out high Nibble
804d 54      LSRB ;Logical Shift Right Port B, mask out high Nibble
804e 7b 08 05      STAB ThUp+1 ;Store Accu B at Throttle-Up Low Byte
*****
* Initialize External Interrupt (IRQ) *
*****
8051 4c 1e 80      IRQon: BSET INTCR,$80 ;Make IRQ Edge Sensitive
*****

```



```

* Initialize Real Time Interrupt & Display*
*****
8054 4c 02 ff      BSET  DDRA, $FF      ;Make Port A all Outputs
8057 4c 57 f0      BSET  DDRP, $F0     ;Make High Nibble of Port P all Outputs
805a 4c 14 83      BSET  RTICTL, $83    ;Enable RTI with a Timeout of 4.096ms
*****
* Initialize AD Converter *
*****
805d 4c 62 80      BSET  ATDCTL2,$80    ;Turn AD-Converter on
8060 4c 65 22      BSET  ATDCTL5,$22    ;Turn on Scan Mode, Channel 2
*****
* Initialize Timer Interrupts *
*****
8063 18 03 01 90 00 9e  MOVW  #400, TC7    ;Load Channel 7 Output Compare Register
8069 18 03 01 f4 00 9a  MOVW  #500, TC5    ;Load Channel 5 Output Compare Register
806f 4c 8d 00      BSET  TMSK2, $00    ;Set Prescaler=1, No Auto Reset
8072 4c 80 e0      BSET  TIOS, $E0    ;Select Channel 5,6,7 Output Compare
8075 4c 88 68      BSET  TCTL1, $68    ;Select OC 5 and 6 to Clear associated Pin and OC7 to Toggle
8078 18 0b 20 00 82  MOVB  #$20, OC7M    ;OC7 acts on (sets or clears depending on OC7D) PT5
807d 18 0b 00 00 83  MOVB  #$00, OC7D    ;OC7 clears PT5
8082 10 ef        CLI                ;Clear Interrupt Masking Bit, Interrupts enabled
*****
* Start of Main Program Loop *
*****
* Check IGBT Status, Error & OverTemp *
*****
8100                ORG  $8100    ;Origin=Start of Main Program
8100 4f ae 01 0c    Wait: BRCLR PORTT,$01 IgbtOK ;Branch if Port T0 is clear -> IGBTs OK
8104 4d 86 80      BCLR  TSCR, $80    ;Disable Timer System
8107 4d 8c 60      BCLR  TMSK1, $60    ;Disable Channel 5,6 Interrupts
810a 4c af 60      BSET  DDRT, $60    ;Make Pins PT5 and PT6 Outputs
810d 4d ae 60      BCLR  PORTT, $60    ;Clear Logic Levels on PT5 and PT6
*****
* Check for Runtime Setting *
*****
8110 fc 08 00      IgbtOK: LDD  Count    ;Load Accu D with Runtime Counter
8113 27 13        BEQ  IniThr    ;Branch to Ini-Throttle if equal to zero
8115 8c 01 90      CMPD  #400    ;Compare Accu D with 400 = 40ms
8118 26 19        BNE  WatchD    ;Branch to WatchD(og) if not equal
811a 4d 86 80      BCLR  TSCR, $80    ;Disable Timer System
811d 4d 8c 60      BCLR  TMSK1, $60    ;Disable Channel 5,6 Interrupts
8120 4c af 60      BSET  DDRT, $60    ;Make Pins PT5 and PT6 Outputs
8123 4d ae 60      BCLR  PORTT, $60    ;Clear Logic Levels on PT5 and PT6
8126 20 0b        BRA  WatchD    ;Branch to WatchD(og)
*****
* Find Initial Throttle Setting *
*****
8128 ce f6 60      IniThr: LDX  #Table    ;Load Table Start into X
812b d6 74        LDAB  ADR2H    ;Load Binary Fraction (AD-Result) into Accu B
812d 18 3f 00      ETBL  0,X      ;Look-Up and Interpolate, Result in Accu D
8130 7c 08 02      STD  DCycle    ;Store Accu D at DutyCycle Memory Location
*****
* Service Watchdog Timer *
*****
8133 18 0b 55 00 17 WatchD: MOVB #$55,COPRST ;Initiate COP Service
8138 18 0b aa 00 17 MOVB #$AA,COPRST ;Finish COP Service
813d 20 c1        BRA  Wait      ;Wait for Interrupts
*****
* End of Main Program Loop *
*****

*****
* Sub-Routines *
*****

*****
* Check for and Perform Throttle-Up *
*****
8200                ORG  $8200    ;Origin=Start of General Subroutines
8200 73 08 06      ChkThr: DEC  Cycles    ;Decrement 'Cycles between Throttle-Up' Counter
8203 27 01        BEQ  UpTrot    ;Branch to Throttle up if zero
8205 3d            RTS          ;Early Return from Throttle-Up Subroutine
* Restore Cycles *
8206 18 0c 08 07 08 06 UpTrot: MOVB  ResCycl Cycles ;Restore 'Cycles between Throttle-Up'
* Throttle-Up *
820c fc 08 02      LDD  DCycle    ;Load Accu D with DutyCycle
820f f3 08 04      ADDD  ThUp     ;Add Increment to Throttle setting

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8212 8c 01 34      CMPD  #0308      ;Compare Accu D with 308 dec
8215 23 03          BLS   LS308      ;Branch if Less or Same
8217 cc 01 34      LDD   #308      ;Load Accu D with max. Throttle Value
821a 7c 08 02      LS308: STD   DCycle ;Store DutyCycle Value
821d 3d            RTS              ;Return from Throttle-Up Subroutine

*****
*   Interrupt Service Routines   *
*****

*****
* Interrupt Service Routine Output Compare 5 Code starts here *
*****

8500      ORG   $8500      ;Origin = Start of OC5 Service Routine
8500 18 0b 40 00 82  OC5I: MOVB  #$40,OC7M ;OC7 acts on (sets or clears depending on OC7D) PT6
8505 fc 08 02      LDD   DCycle ;Load Accu D with Throttle Data
8508 26 05          BNE   ADJ5      ;Branch to ADJ5 if Accu D is not equal to zero
850a 79 00 83      CLR   OC7D      ;OC7 sets PT6 Low
850d 20 05          BRA   ZERO5     ;Branch to ZERO5
850f 18 0b 40 00 83  ADJ5: MOVB  #$40,OC7D ;OC7 sets PT6 High
8514 5c 9c          ZERO5: STD   TC6 ;Load Channel 6 Output Compare Register
8516 18 03 03 1f 00 9e  MOVW  #799,TC7 ;Load Channel 7 Output Compare Register
851c 4c 8d 08      BSET  TMSK2,$08 ;Enable OC7 Auto Reset
851f 18 0b 20 00 8e  MOVB  #$20,TFLG1 ;Reset Timer-Flag 5
8524 0b            RTI              ;Return from Interrupt

*****
* Interrupt Service Routine Output Compare 6 Code starts here *
*****

8600      ORG   $8600      ;Origin = Start of OC6 Service Routine
8600 18 0b 20 00 82  OC6I: MOVB  #$20,OC7M ;OC7 acts on (sets or clears depending on OC7D) PT5
8605 fc 08 02      LDD   DCycle ;Load Accu D with Throttle Data
8608 26 05          BNE   ADJ6      ;Branch to ADJ6 if Accu D is not equal to zero
860a 79 00 83      CLR   OC7D      ;OC7 sets PT5 Low
860d 20 05          BRA   ZERO6     ;Branch to ZERO6
860f 18 0b 20 00 83  ADJ6: MOVB  #$20,OC7D ;OC7 sets PT5 High
8614 c3 01 90      ZERO6: ADDD  #400 ;Add 400 to Accu D
8617 5c 9a          STD   TC5 ;Load Channel 5 Output Compare Register
8619 18 03 01 8f 00 9e  MOVW  #399,TC7 ;Load Channel 7 Output Compare Register
861f 4d 8d 08      BCLR  TMSK2,$08 ;Disable OC7 Auto Reset
8622 18 0b 40 00 8e  MOVB  #$40,TFLG1 ;Reset Timer-Flag 6
*   Increment Runtime Counter
8627 fc 08 00      LDD   Count ;Load Accu D with Runtime Counter
862a c3 00 01      ADDD  #001 ;Add 1 to the Count
862d 7c 08 00      STD   Count ;Store Accu D to Memory Location Count
8630 16 82 00      JSR   ChkThr ;Jump to 'Check-Throttle' Subroutine
8633 0b            RTI              ;Return from Interrupt

*****
* RTI-Interrupt Service Routine Code starts here *
*****

8700      ORG   $8700      ;Origin = Start of RTI-Interrupt Service Routine
8700 ce 08 02      RTInt: LDX   #DCycle ;Load X-Register with Position of DutyCycle Data
8703 16 f7 90      JSR   DISPLYX ;Call Display Scan Subroutine
8706 4c 15 80      BSET  RTIFLG, $80 ;Reset RTI-Flag
8709 0b            RTI              ;Return from Interrupt

*****
* IRQ-Interrupt Service Routine Code starts here *
*****

8800      ORG   $8800      ;Origin = Start of IRQ-Interrupt Service Routine
8800 4d 1e 40      IRQInt: BCLR  INTCR, $40 ;Disconnect IRQ Pin
8803 79 00 14      CLR   RTICTL ;Disable RTI Interrupt
8806 79 00 02      CLR   DDRA ;Make Port A all Inputs; shut off Display
8809 4d 57 f0      BCLR  DDRP, $F0 ;Make High Nibble of Port P all Inputs
880c 4c 86 80      BSET  TSCR, $80 ;Enable Timer System
880f 4c 8c 60      BSET  TMSK1, $60 ;Enable Channel 5,6 Interrupts
8812 0b            RTI              ;Return from Interrupt

*****
*   Watchdog Timer Expiration Reset Handler   *
*****

8900      ORG   $8900 ;Origin = Start of Watchdog Timer / Clock Monitor Reset Handler
8900 cf 0c 00      LDS   #$0C00 ;Initialize Stack Pointer
8903 18 0b 08 00 10  MOVB  #$08,INITRM;Fix the Position of the RAM (Write Once)
8908 18 0b 00 00 11  MOVB  #$00,INITRG;Fix the Position of the CPU Regs (Write Once)
890d 18 0b 01 00 12  MOVB  #$01,INITEE;Fix the Position of the EEPROM (Write Once)
8912 18 0b 00 00 16  MOVB  #$00,COPCTL;Turn COP off (Write Once)

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*      The following Registers should have been cleared by the Reset already *
8917 79 00 86      CLR    TSCR    ;Disable Timer System
891a 79 00 af      CLR    DDRT    ;Make Port T all Inputs
891d 79 00 ae      CLR    PORTT   ;Clear all Bits on Port T
8920 20 fe      COPBRA: BRA    COPBRA ;Wait here for Hardware Reset

*****
* Set up Default Interrupt Sercive Routine in Memory *
*****
9000      ORG    $9000 ;Select Location for Default Interrupt Handler
9000 0b      RTI      ;Return from Interrupt - do nothing as a default

*****
* Set up Symbol Table in Memory *
*****
f650      ORG    $F650 ;Beginning of Free Space in Flash EEPROM
f650 3f      SegCde: FCB    $3F    ;$3F = Code for 0
f651 06      FCB    $06    ;$06 = Code for 1
f652 5b      FCB    $5B    ;$5B = Code for 2
f653 4f      FCB    $4F    ;$4F = Code for 3
f654 66      FCB    $66    ;$66 = Code for 4
f655 6d      FCB    $6D    ;$6D = Code for 5
f656 7d      FCB    $7D    ;$7D = Code for 6
f657 07      FCB    $07    ;$07 = Code for 7
f658 7f      FCB    $7F    ;$7F = Code for 8
f659 6f      FCB    $6F    ;$6F = Code for 9
f65a 77      FCB    $77    ;$77 = Code for A
f65b 7c      FCB    $7C    ;$7C = Code for B
f65c 39      FCB    $39    ;$39 = Code for C
f65d 5e      FCB    $5E    ;$5E = Code for D
f65e 79      FCB    $79    ;$79 = Code for E
f65f 71      FCB    $71    ;$71 = Code for F

*****
*      Throttle Lookup Table for ETBL      *
*****
f660 00 00      Table: FDB    000    ;Zero Power
f662 01 36      FDB    310    ;Full Power

*****
* Subroutine to Multiplex 4 Digit Display on Port A using Port P*
* This Subroutine assumes the Display Data at $09FF and $09FE *
*****
f740      ORG    $F740 ;Beginning of Free Space in Flash EEPROM
f740 96 56      Displ: LDAA    PORTP ;Load PORTP contents into Accu A
f742 4d 56 f0      BCLR    PORTP,$F0 ;Clear High Nibble of Port P
f745 84 f0      ANDA    #$F0 ;Mask Out Higher Nibble
f747 44      LSRA      ;Logical Shift Right Accu A, advance to next (lower) Digit
f748 81 10      CMPA    #$10 ;Compare Accu A with $10
f74a 27 2e      BEQ     Digit1 ;Branch to Digit1 if equal
f74c 81 20      CMPA    #$20 ;Compare Accu A with $20
f74e 27 1c      BEQ     Digit2 ;Branch to Digit2 if equal
f750 81 40      CMPA    #$40 ;Compare Accu A with $40
f752 27 0e      BEQ     Digit3 ;Branch to Digit3 if equal

f754 4c 56 80      Digit4: BSET    PORTP,$80 ;Turn Digit 4 on
f757 f6 09 fe      LDAB    Display ;Load Accu B with contents of 'Display'
f75a ce 00 04      Dig4a: LDX     #4 ;Load X with decimal 4 (bits to shift)
f75d 16 f7 8b      JSR     ShiftR ;Jump to Right-Shift Sub-Routine
f760 20 20      BRA     Show ;Branch to Show Label

f762 4c 56 40      Digit3: BSET    PORTP,$40 ;Turn Digit 3 on
f765 f6 09 fe      LDAB    Display ;Load Accu B with contents of 'Display'
f768 c4 0f      Dig3a: ANDB    #$0F ;Mask out Digit 4
f76a 20 16      BRA     Show ;Branch to Show Label

f76c 4c 56 20      Digit2: BSET    PORTP,$20 ;Turn Digit 2 on
f76f f6 09 ff      LDAB    Display+1 ;Load Accu B with contents of 'Display'+1
f772 ce 00 04      Dig2a: LDX     #4 ;Load X with decimal 4 (bits to shift)
f775 16 f7 8b      JSR     ShiftR ;Jump to Right-Shift Sub-Routine
f778 20 08      BRA     Show ;Branch to Show Label

f77a 4c 56 10      Digit1: BSET    PORTP,$10 ;Turn Digit 1 on
f77d f6 09 ff      LDAB    Display+1 ;Load Accu B with contents of 'Display'+1
f780 c4 0f      Dig1a: ANDB    #$0F ;Mask out Digit 2

f782 ce f6 50      Show: LDX     #SegCde ;Load start of Code Lookup table into X
f785 18 0d e5 00 00      MOV    B,X PORTA ;Put 7_seg Code to Port A

```



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f78a 3d      RTS      ;Return from Diplay Subroutine

*****
* Subroutine to shift Accu B (content of) X times *
*****
f78b 54      ShiftR: LSRB      ;Logical Shift Right Accu B
f78c 04 35 fc DBNE X, ShiftR ;Decrement X and branch to ShiftR if X>0
f78f 3d      RTS      ;Return from ShiftR Subroutine

*****
* Subroutine to Multiplex 4 Digit Display on Port A using Port P*
* Here X points to the Position of the Display Data *
*****
f790      ORG    $F790 ;Beginning of Free Space in Flash EEPROM
DispX: LDA    PORTP ;Load PORTP contents into Accu A
      BCLR    PORTP,$F0 ;Clear High Nibble of Port P
f792 4d 56 f0 ANDA    #$F0 ;Mask Out Higher Nibble
f795 84 f0      LSRA      ;Logical Shift Right Accu A, advance to next (lower) Digit
f797 44      CMPA    #$10 ;Compare Accu A with $10
f798 81 10      BEQ     Dig1 ;Branch to Dig1 if equal
f79a 27 1d      CMPA    #$20 ;Compare Accu A with $20
f79c 81 20      BEQ     Dig2 ;Branch to Dig2 if equal
f79e 27 12      CMPA    #$40 ;Compare Accu A with $40
f7a0 81 40      BEQ     Dig3 ;Branch to Dig3 if equal
f7a2 27 07

f7a4 4c 56 80 Dig4: BSET    PORTP,$80 ;Turn Digit 4 on
f7a7 e6 00      LDAB    0,X ;Load Accu B with Display High Byte
f7a9 20 af      BRA     Dig4a ;Branch to Dig4a Label

f7ab 4c 56 40 Dig3: BSET    PORTP,$40 ;Turn Digit 3 on
f7ae e6 00      LDAB    0,X ;Load Accu B with Display High Byte
f7b0 20 b6      BRA     Dig3a ;Branch to Dig3a Label

f7b2 4c 56 20 Dig2: BSET    PORTP,$20 ;Turn Digit 2 on
f7b5 e6 01      LDAB    1,X ;Load Accu B with Display Low Byte
f7b7 20 b9      BRA     Dig2a ;Branch to Dig2a Label

f7b9 4c 56 10 Dig1: BSET    PORTP,$10 ;Turn Digit 1 on
f7bc e6 01      LDAB    1,X ;Load Accu B with Display Low Byte
f7be 20 c0      BRA     Dig1a ;Branch to Dig1a Label

*****
* Set up Vector Table in Memory *
*****
f7d0      ORG    $F7D0 ;Start of Vector Table
f7d0 90 00      DW     $9000 ;BDLC Interrupt Vector -> Default Interrupt Handler
f7d2 90 00      DW     $9000 ;ATD Interrupt Vector -> Default Interrupt Handler
f7d4 90 00      DW     $9000 ;reserved Interrupt Vector -> Default Interrupt Handler
f7d6 90 00      DW     $9000 ;SCIO Interrupt Vector -> Default Interrupt Handler
f7d8 90 00      DW     $9000 ;SPI Interrupt Vector -> Default Interrupt Handler
f7da 90 00      DW     $9000 ;PAI Edge Interrupt Vector -> Default Interrupt Handler
f7dc 90 00      DW     $9000 ;PAOverflow Interrupt Vector -> Default Interrupt Handler
f7de 90 00      DW     $9000 ;TIOverflow Interrupt Vector -> Default Interrupt Handler
f7e0 90 00      DW     $9000 ;Timer Ch 7 Interrupt Vector -> Default Interrupt Handler
f7e2 86 00      DW     $8600 ;Timer Ch 6 Interrupt Vector -> Ch 6 Interrupt Handler
f7e4 85 00      DW     $8500 ;Timer Ch 5 Interrupt Vector -> Ch 5 Interrupt Handler
f7e6 90 00      DW     $9000 ;Timer Ch 4 Interrupt Vector -> Default Interrupt Handler
f7e8 90 00      DW     $9000 ;Timer Ch 3 Interrupt Vector -> Default Interrupt Handler
f7ea 90 00      DW     $9000 ;Timer Ch 2 Interrupt Vector -> Default Interrupt Handler
f7ec 90 00      DW     $9000 ;Timer Ch 1 Interrupt Vector -> Default Interrupt Handler
f7ee 90 00      DW     $9000 ;Timer Ch 0 Interrupt Vector -> Default Interrupt Handler
f7f0 87 00      DW     $8700 ;RTI Interrupt Vector -> RTI Interrupt Handler
f7f2 88 00      DW     $8800 ;IRQ Interrupt Vector -> IRQ Interrupt Handler
f7f4 90 00      DW     $9000 ;XIRQ Interrupt Vector -> Default Interrupt Handler
f7f6 90 00      DW     $9000 ;SWI Interrupt Vector -> Default Interrupt Handler
f7f8 90 00      DW     $9000 ;Illegal OC Interrupt Vector -> Default Interrupt Handler
f7fa 89 00      DW     $8900 ;COP Failure Reset Vector -> Start of Reset Handler
f7fc 89 00      DW     $8900 ;Clock Monitor Reset Vector -> Start of Reset Handler
f7fe 80 00      DW     $8000 ;Hardware Reset Vector -> Start of Flash EEPROM

Total errors: 0
Total warnings: 0

```

APPENDIX C
DATA SHEETS

SKiiP 1242 GB 120 - 407 CTV

Absolute Maximum Ratings			
Symbol	Conditions ¹⁾	Values	Units
V_{ISCL} ⁴⁾	AC, 1min	3000	V
T_{op}, T_{stg}	Operating / stor. temperature	-25...+85	°C
IGBT and Inverse Diode			
V_{CES}		1200	V
V_{CC} ⁵⁾	Operating DC link voltage	900	V
I_C	IGBT	1200	A
T_j ³⁾	IGBT + Diode	-40...+150	°C
I_F	Diode	1200	A
I_{FM}	Diode, $t_p < 1$ ms	2400	A
I_{FSV}	Diode, $T_j = 150$ °C, 10ms; sin	8640	A
I^2t (Diode)	Diode, $T_j = 150$ °C, 10ms	373	kAs ²
Driver			
V_{S1}	Stabilized Power Supply	18	V
V_{S2}	Non-stabilized Power Supply	30	V
f_{smax}	Switching frequency	14	kHz
dV/dt	Primary to secondary side	75	kV/μs

Characteristics					
Symbol	Conditions ¹⁾	min.	typ.	max.	Units
IGBT ¹⁾					
V_{IBRCES}	Driver without supply	$\geq V_{CES}$			V
I_{CES}	$V_{CE} = 0, T_j = 25\text{ }^{\circ}\text{C}$ $V_{CE} = V_{CES} T_j = 125\text{ }^{\circ}\text{C}$		60	1,8	mA
V_{IC}	$T_j = 125\text{ }^{\circ}\text{C}$			1,38	V
r_i	$T_j = 125\text{ }^{\circ}\text{C}$			1,8	mΩ
V_{CESat}	$I_C = 1000\text{A}, T_j = 125\text{ }^{\circ}\text{C}$			3,2	V
V_{CESat}	$I_C = 1000\text{A}, T_j = 25\text{ }^{\circ}\text{C}$			3,05	V
$E_{on} + E_{off}$	$V_{CC}=600/900\text{V}, I_C=1200\text{A}$ $T_j = 125\text{ }^{\circ}\text{C}$			360/586	mJ
C_{CH}	per SkiiP, AC side		5,6		nF
L_{CH}	Top, Bottom		4		nH
Inverse Diode ²⁾					
$V_F = V_{EC}$	$I_F = 1000\text{A}; T_j = 125\text{ }^{\circ}\text{C}$			2,43	V
$V_F = V_{EC}$	$I_F = 1000\text{A}; T_j = 25\text{ }^{\circ}\text{C}$			2,55	V
$E_{on} + E_{off}$	$I_F = 1200\text{A}; T_j = 125\text{ }^{\circ}\text{C}$			48	mJ
V_{IC}	$T_j = 125\text{ }^{\circ}\text{C}$		0,91		V
r_i	$T_j = 125\text{ }^{\circ}\text{C}$		1,0		mΩ
Thermal Characteristics					
$R_{th,js}$ ¹⁰⁾	per IGBT			0,023	$^{\circ}\text{C/W}$
$R_{th,js}$ ¹⁰⁾	per Diode			0,063	$^{\circ}\text{C/W}$
$R_{th,sa}$ ⁶⁾	P16 heatsink; see case S4			0,033	$^{\circ}\text{C/W}$
Driver					
I_{S1}	Supply current 15V-supply	$290+580 \cdot f_s / f_{smex} + 1,3 \cdot I_{AC} / A$			mA
I_{S2}	Supply current 24V-supply	$220+420 \cdot f_s / f_{smex} + 1,0 \cdot I_{AC} / A$			mA
$t_{interlock-driver}$	Interlock-time		3,3		μs
SKiiPPACK protection					
I_{RFS}	Short circuit protection		$1500 \pm 2\%$		A
I_{RFL}	Ground fault protection		-		A
T_{RP}	Over-temp. protection		$115 \pm 5\%$		$^{\circ}\text{C}$
$U_{DC-PROT}$ ⁹⁾	U_{DC} -protection		$920 \pm 2\%$		V
Mechanical Data					
M1	DC terminals, SI Units	4		6	Nm
M2	AC terminals, SI Units	8		10	Nm

SKiiPPACK®

SK integrated intelligent
Power PACK
halfbridge

SKiiP

1242 GB 120 - 407 CTV ^{7,9)}

Preliminary Data

Case S4

Features

- Short circuit protection, due to evaluation of current sensor signals
- Isolated power supply
- Low thermal impedance
- Optimal thermal management with integrated heatsink
- Pressure contact technology with increased power cycling capability, compact design
- Low stray inductance
- High power, small losses
- Over-temperature protection

- ¹⁾ $T_{ambient} = 25$ °C, unless otherwise specified
- ²⁾ CAL = Controlled Axial Lifetime Technology (soft and fast)
- ³⁾ without driver
- ⁴⁾ Driver input to DC link/ AC output to heatsink
- ⁵⁾ with Semikron-DC link (low inductance)
- ⁶⁾ other heatsinks on request
- ⁷⁾ C - Integrated current sensors
T - Temperature protection
V - 15 V or 24 V power supply
- ⁸⁾ AC connection busbars must be connected by the user; copper busbars available on request
- ⁹⁾ options available for driver:
U - DC link voltage sense
F - Fiber optic connector
- ¹⁰⁾ "s" referenced to temperature sensor
- ¹¹⁾ NPT-technology with homogeneous current-distribution

Figure C.1 Semikron IGBT Data Sheet

The MC68HC12A0 microcontroller unit (MCU) is a 16-bit device composed of standard on-chip peripheral modules connected by an intermodule bus. Modules include a 16-bit central processing unit (CPU12), a Lite integration module (LIM), two asynchronous serial communications interfaces (SCI0 and SCI1), a serial peripheral interface (SPI), a timer and pulse accumulation module, an 8-bit analog-to-digital converter (ATD), 1-Kbyte RAM, and memory expansion logic with chip selects, key wakeup ports, and a phase-locked loop (PLL).

8HC12A0 Features

- Low-Power, High-Speed M68HC12 CPU
- Power Saving STOP and WAIT Modes
- Memory
- 1024-Byte RAM
- On-Chip Memory Mappings Allows Expansion to over 5-Mbyte Address Space
- Single-Wire Background Debug Mode
- Non-Multiplexed Address and Data Buses
- Seven Programmable Chip Selects with Clock Stretching (Expanded Modes)
- 8-Channel, Enhanced 16-Bit Timer with Programmable Prescaler
- All Channels Configurable as Input Capture or Output Compare
- Flexible Choice of Clock Source
- 16-Bit Pulse Accumulator
- Real-Time Interrupt Circuit
- Computer Operating Properly (COP) Watchdog
- Clock Monitor
- Phase-Locked Loop
- Two Enhanced Asynchronous Non-Return to Zero (NRZ) Serial Communication Interfaces (SCI)
- Enhanced Synchronous Serial Peripheral Interface (SPI)
- 8-Channel, 8-Bit Analog-to-Digital Converter (ATD)
- Up to 24 Key Wakeup Lines with Interrupt Capability
- Available in 112-Pin Thin Quad Flat Pack (TQFP) Packaging

[top]

68HC12A0 Parametrics

RAM (KBytes)	Timer	I/O	Serial	A/D	Operating Voltage (V)	Bus Frequency (Max) (MHz)
1	8-CH 16-Bit IC or OCRTI, pulse accumulator	Up to 61	Dual SCI, SPI	8-CH 8-Bit	5, 3.3	8,5

<http://ebus.mot-sps.com/ProdCat/psp/0,1250,68HC12A0~M98637,00.html>

Figure C.2 68HC12A0 Data Sheet

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