DEVELOPMENT OF A SECOND BREAKDOWN MODEL
FOR BIPOLAR TRANSISTORS

by

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ABSTRACT

Semiconductor devices are often driven into operating regions in which conventional models, representing normal regions of operation, are inadequate. An example of such an operating region is frequently obtained when bipolar transistors are operated as switches in circuits containing inductors. In this case, the transistor may experience large voltages and currents simultaneously.

In an actual transistor, the collector-emitter voltage is constrained by avalanche breakdown between the collector and emitter regions; under conditions of breakdown or near-breakdown and high collector current, an instability, known as second breakdown, may occur. This instability often results in catastrophic device failure.

The library bipolar transistor model contained within the circuit analysis code, SPICE, is quite sophisticated, within a normal region of transistor operation. However, it does not model either avalanche or second breakdown. Several models, in the form of augmentations to the SPICE transistor model, have been developed in this work. These models permit SPICE to predict accurately voltages and currents associated with the transient response of circuits containing both energy storage elements and active devices, which the standard SPICE code alone is incapable of doing.

In this work avalanche breakdown has been modeled in a manner not previously encountered by the author. This model recognizes the interdependence of the two transistor junctions, with regard to breakdown between the collector and emitter regions. A second breakdown model that previously did not exist, is presented. The concept of a dependent subcircuit is introduced to model second breakdown, in which case the subcircuit also performs diagnostic and controlling functions, as an integral part of the model. A subcircuit such as used in this work to model second breakdown is analogous to an analog computer.

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CHAPTER I

INTRODUCTION

Semiconductor devices are often driven into operating regions in which conventional models representing normal regions of operation are inadequate. This may occur when the device is operated in an electromagnetic pulse (E.M.P.) environment, in which case the circuit may encounter large induced voltages and consequent currents. Alternatively, high levels of drive stress may produce similar results. The purpose of this work is to obtain an improved bipolar transistor (BJT) model, suitable for use in circuit modeling and to perform the analysis of a typical circuit incorporating this model in order to predict circuit upset and failure.

This work has concentrated on accurately obtaining the response of a circuit to a high input stress, using the simulation program SPICE. SPICE automatically constructs equivalent circuits to model the active elements; the circuit used for BJTs is based on the Ebers-Moll model [1]. The internal nodes of these circuits are inaccessible to the user, but a faithful representation of the device to be modeled is assured by providing the SPICE program with a comprehensive and accurate set of model parameters. The complete BJT model is quite complex, requiring a set of forty parameters, although frequently only a subset of these is required, depending on the specific type of analysis to be performed. If certain parameters are omitted, SPICE will use default values, which in some cases will cause the model to default to a simpler version; for example, omission of any ohmic resistance (base, emitter or collector resistance) will result in a zero default value.

Although the SPICE generated BJT model is generally quite sophisticated (for example, it can model second order effects such as base width modulation and the current dependence of common-emitter current gain), it does not model breakdown of any kind. The major three types of breakdown, or failure, observed in BJTs are modeled in this work. These are reverse breakdown of the base-emitter junction; avalanche breakdown between the collector and emitter regions; and reverse-bias second breakdown. The physical mechanism responsible for second breakdown has been extensively investigated over a period of several decades, by numerous researchers [2,3,4,5,6,7,8]; to date, no single hypothesis can explain all of the experimental data, or is universally accepted. None of these proposed physical mechanisms can predict circuit-level behavior and it is therefore justifiable and

desirable to seek a circuit-level model for second breakdown. The models detailed in this work are circuit-level models and have been realized, primarily by the addition of circuit elements to the external nodes of the device and subnetworks used for control purposes. These external additions to the BJT model and concepts applied have general applicability to other circuits.

The author has been unable to discover any reference to the circuit-level modeling of second breakdown. The only known attempt to model avalanche breakdown [9], which represents the consensus of a number of people, is erroneous; its major flaw is that it treats the transistor as two independent semiconductor junctions. In reality, each junction has a functional dependence on the other junction and this must be reflected in any authentic circuit-level model.

Of the three breakdown models developed, the second breakdown model is the most sophisticated. This model includes the avalanche breakdown model as a necessary element. Consequently, the development and evaluation of the second breakdown model are the primary foci of this work.

CHAPTER II

THEORY OF SECOND BREAKDOWN

Second breakdown is categorized as either forward- or reverse-bias second breakdown [10]. Forward-biased breakdown can occur during turn-on of a device. The base-emitter potential, V_{BE} , decreases with increasing temperature; if the emitter structure is slightly nonhomogeneous or suffers from uneven current distribution, localized hot spots may develop during turn-on. V_{BE} will decrease in the vicinity of these hot spots, resulting in an increase of current through these regions, inasmuch as current flows preferentially through areas with the lowest V_{BE} . Any increase in current will result in further localized heating. This sequence of events is unstable and can lead to failure within a few microseconds of turn-on.

Reverse-bias second breakdown is encountered more frequently than forward-bias breakdown; the former more severely restricts the safe operating area than does the latter, because simultaneously large collector-emitter voltage, V_{CE} , and collector current, I_C , may exist, particularly when inductive loads are switched. Consider a transistor operating in saturation or quasi-saturation, with collector current flowing; if a reverse-bias voltage is applied to the emitter-base junction, the transistor will begin to turn-off, once the stored charge has been extracted from the base region. However, it is not possible to reverse-bias the complete emitter structure simultaneously, i.e., the edges of the emitter are biased off first, resulting in the restriction of the collector current to the center of the emitter region. This focused current may lead to very high localized current densities which, coupled with high collector voltages, can lead to failure.

Snyder [11] has postulated that the phenomenon observed during second breakdown in a semiconductor is the occurrence of a current controlled negative resistance region. Once this event has occurred, the semiconductor may be modeled as a solid state plasma which undergoes a plasma pinch, as a consequence of its own self-magnetic field.

Reverse-bias second breakdown is characterized by a rapid collapse of V_{CE} . The form of V_{CE} and I_C immediately preceding this collapse allows second breakdown to be categorized as either type A, B or C; these types are shown in figures 1a, 1b, and 1c, respectively. The type of breakdown which occurs depends upon the operating region of the device and the magnitudes of both the forward and reverse

a.

b.

c.

Figure 1. Characterization of second breakdown. The horizontal scale, for all curves, is time. a. type A; b. type B; c. type C.

base current drives.

Type A breakdown (figure 1a) is normally observed when the transistor is initially in the normal active region or quasi-saturated, which implies small forward current drives. Low reverse current drives are also usually characteristic. After a short delay following the application of the reverse pulse, V_{CE} increases to the collector-emitter sustaining voltage or the collector-emitter breakdown voltage, BV_{CEO} ; these two voltages are essentially identical. After remaining in this state for a short time (depending on the device type), V_{CE} increases to the second breakdown voltage. I_C begins to decrease approximately linearly after the collector-emitter voltage reaches BV_{CEO} .

Type B breakdown (figure 1b) is normally observed when the transistor is in quasi-saturation prior to turn-off. V_{CE} reaches BV_{CEO} and remains constant until breakdown. I_C may decrease linearly, although not at a rate as high as that observed with type A. Type C breakdown (figure 1c) is usually associated with high forward base currents. V_{CE} does not reach BV_{CEO} before second breakdown and I_C remains essentially constant.

It is to be noted that second breakdown and failure are not necessarily synonymous; the former usually leads to the latter, unless measures are taken to protect the device. These measures predominantly involve diversion or "crowbarring" of the collector current.

CHAPTER III

SPICE PARAMETERS

The SPICE user's guide [12] contains a listing of 40 BJT model parameters. SPICE was originally developed for integrated circuit analysis and some of these parameters, for example, CJS, the zero bias collector-substrate capacitance, are not relevant for the type of analysis performed in this work. Other parameters are required for specific types of analysis only, such as a noise calculation. Consequently, only a subset of the complete parameter set is required for the simulations performed in this work. These simulations and measurements utilized the 2N6551 transistor for the device under investigation. This transistor is a general purpose, medium power device, capable of switching currents of up to 1.5 A.

Supplemental measurements are generally required for an accurate SPICE analysis because there exists no comprehensive data base from which SPICE parameters may be obtained. Allowing SPICE to default to its most basic BJT model will generally not produce authentic results, especially for transient analyses. The SPICE parameters used to model the 2N6551 transistor in this work were obtained from a report [9] describing a previous analysis. The report specifies twenty-one BJT model parameters; of the remaining unspecified parameters, the parasitic base resistance, R_B , is very important at high levels of drive stress. The parasitic emitter resistance, R_E , is required to obtain R_B , and although a value of R_E was provided, this parameter was remeasured for accuracy.

R_E can be found from the relationship [1]

$$V_{CE} = (kT/q) \cdot [\ln(1/\alpha_R)] + I_B R_E,$$

where k is Boltzmann's constant, T is the absolute temperature, q is the electronic charge, α_R is the inverse current gain and I_B is the forward base current. This expression is obtained assuming that the collector terminal is open-circuited (which implies that $I_B = I_E$) and that positive base current flows, so that the transistor is saturated. If α_R is considered constant, then R_E can be obtained from a plot of I_B vs. $V_{CE(sat)}$; figure 2 shows such an oscilloscope trace for a typical 2N6551 transistor. V_{CE} was measured with a 10X, high impedance probe and I_B was obtained from a differential voltage measurement across a 10 Ω sampling base resistance. In order to

Figure 2. Oscilloscope trace used for obtaining R_E . Vertical (I_B) and horizontal (V_{CE}) magnitudes per large division are, respectively, 50 mA and 50 mV.

obtain a continuous waveform, a variable amplitude, full-wave rectified sine wave, obtained from the collector-emitter terminals of a curve tracer, was used as the base drive. R_E was calculated to be 0.18Ω from the inverse slope of the linear portion of the curve.

There are several different methods which may be used to measure R_B ; however, the particular procedure chosen depends on the operating conditions of the device. For large signal switching applications, the pulse measurement technique is the most appropriate, and was used in this work; the test circuit is shown in figure 3. Ideally, the measurement should be performed with the transistor operating in the region of required simulation. The high drives used in this work will cause the transistor under test (TUT) to operate more often in the saturation region than in the normal active region; the measurement was therefore made with the transistor saturated.

If a known base current is applied and then rapidly decreased to zero, R_B may be determined from the time-dependent behavior of the base-emitter voltage, V_{BE} . Two regions of V_{BE} fall may be identified: an initial rapid decay associated with resistive effects and a subsequent slower decay associated with charge storage effects. If ΔV_{BE} is the magnitude of the initial drop in V_{BE} , R_B may be determined from the general expression:

$$\Delta V_{BE} = R_B I_B + (I_B + I_C) R_E.$$

As I_B falls to zero, the voltage-drops across R_B and R_E vanish, so that V_{BE} becomes equal to the voltage across the internal base-emitter capacitance, which cannot decay instantaneously. Then ΔV_{BE} is the total voltage-drop across R_B and R_E . (It should be emphasized that, in the preceding equation, I_C is not equal to βI_B .)

The equation for ΔV_{BE} can be simplified if R_L is chosen infinitely large, i.e., if the collector is open circuited. This ensures that the device is saturated, provided that a positive base current flows. The resulting expression for ΔV_{BE} becomes:

$$\Delta V_{BE} = I_B (R_B + R_E).$$

The measurement of R_B was performed single shot, with a drive pulse of variable amplitude and of $100 \mu\text{s}$ duration. R_S was chosen to be 50Ω , which permitted sufficient base current to flow. A fast switching diode was included for

Figure 3. Pulse measurement circuit used for determining the base resistance, R_B .

isolation. The observed base-emitter voltage is shown in figure 4. The essentially linear voltage fall observed after the ΔV_{BE} transition is associated with excess charge storage in the base (the undershoot is considered to be an artifact); ΔV_{BE} in figure 4 was found to be 520 mV. The steady-state base current of 336 mA (considering the current shunted by the base probe), was obtained by measuring the voltage-drop across R_S . Using these values of I_B , ΔV_{BE} and the previously determined value of R_E , R_B was found to be 1.366 Ω .

Appendix A contains a complete listing of all the SPICE parameters used to model the behavior of the transistor.

Figure 4. Base-emitter voltage observed in the R_B measurement. Vertical (V_{BE}) and horizontal (time) magnitudes per large division are, respectively, 200 mV and 2 μ S.

CHAPTER IV

JUNCTION AND THERMAL FAILURE

4.1. Junction Breakdown

Emitter-base and collector-emitter breakdown are modeled by the addition of external elements to the BJT model. It should be noted that, even while these elements are actively influencing circuit operation, the SPICE BJT model remains in effect. Consequently, the additional elements used to model breakdown do not replace the SPICE BJT model, but augment it; as breakdown becomes more pronounced, the avalanche circuitry begins to dominate. The complete augmented breakdown model is shown in figure 5. When prespecified breakdown voltages are exceeded, the current is allowed to increase at a rate determined by a resistive term, empirically matched to the actual breakdown curves. SPICE does not contain an avalanche breakdown model because avalanche is divergent; the model used in this work does not allow the current to increase indefinitely, and no convergence problems have been encountered with this part of the model.

Reverse emitter-base breakdown is modeled by the resistor R_{EB} , voltage source V_{EBO} and the diode D_2 ; these elements are connected directly between the base and emitter nodes of the transistor. For base-emitter voltages of less than V_{EBO} , D_2 is reverse biased and hence no current flows through this branch. As the reverse voltage increases beyond V_{EBO} , a current begins to flow, increasing with increasing reverse bias, to a value determined by R_{EB} . This current flows out of the base terminal of the augmented BJT model and may be considered the effective reverse base-emitter current. Source V_{BT} in figure 5 serves as a monitor for this current.

Collector-emitter breakdown is modeled in a similar fashion by resistor R_{CE} , voltage source V_{CEO} and diode D_1 , connected between the collector and emitter nodes of the transistor. When collector-emitter breakdown occurs, the network contributes additional forward collector current. Under most operating conditions, the collector-emitter voltage, V_{CE} , is constrained by the collector-emitter breakdown curve, measured with the base open-circuited, that is, the BV_{CEO} curve. The point on the BV_{CEO} curve where the collector current begins to increase significantly beyond its leakage current value was chosen as the value of V_{CEO} . This procedure for modeling collector-emitter breakdown is considerably more realistic

Figure 5. The augmented BJT breakdown model.

than simply modeling breakdown of the junctions independently, because each junction has a functional dependence upon the other. Collector-emitter breakdown does not necessarily imply breakdown of the collector-base junction; the former, as distinguished from the latter, is a consequence of transistor action, as opposed to being solely a high-field phenomenon. Under most operating conditions, the collector-emitter breakdown voltage is significantly less than that of the collector-base junction.

The diodes referred to as D_1 and D_2 are modeled principally using the default diode parameters contained in SPICE; this results in a very close approximation to an ideal diode, inasmuch as the model provides low ohmic resistance ($0.5\ \Omega$) and infinite reverse breakdown voltage. (Reasons for choosing some non-default values of the diode and BJT parameters will be discussed in greater detail in subsequent sections.)

The values of the components required for the breakdown model were determined empirically from curve tracer data. The emitter-base breakdown curve provides values for both V_{EBO} (BV_{EBO}) and the dynamic breakdown resistance, R_{EB} . R_{EB} is obtained from the slope of the linear region of the breakdown curve. V_{EBO} corresponds to the intersection of the line used to calculate R_{EB} and the V_{EB} axis. R_{EB} and V_{EBO} were found to be $1.0\ \Omega$ and $9.3\ \text{V}$, respectively.

Figure 6 shows typical characteristic curves for a 2N6551 device; figure 6a shows the form of the BV_{CEO} breakdown, while figure 6b shows a portion of the curves obtained for high base current steps ($1\ \text{mA/step}$). Because of curve tracer limitations, it was not possible to drive the device into avalanche at these higher drives. BV_{CEO} , which corresponds to V_{CEO} , was found to be around $116\ \text{V}$ from figure 6a. Initially, the collector-emitter dynamic breakdown resistance, R_{CE} , was also obtained from the curves. However, the slope, that is R_{CE} , is temperature dependent and considerable power is dissipated in the transistor during the curve tracer measurement. In order to circumvent this problem, a pulsed measurement was performed. The circuit used to perform this measurement is shown in figure 7. R_C ($200\ \Omega$) is a current limiting resistor and V_{CC} is a variable DC supply. The mercury-wetted reed relay was triggered repetitively; the pulse generator drive was adjusted to close the relay contacts for approximately $500\ \mu\text{s}$ and to open them for several milliseconds. Exact adjustment of the relay duty cycle was difficult, owing to the coil activation and deactivation times (of the order of milliseconds) associated with a contact change. V_{CE} and the voltage across R_C (which provides I_C) were measured

a.

b.

Figure 6. Characteristic curves for the 2N6551 device. Vertical (I_C) and horizontal (V_{CE}) magnitudes per large division and base drive (I_B) per step are, respectively, a. 2 mA, 20 V and 0.01 mA; b. 0.1 A, 1 V and 1mA.

Figure 7. Circuit used to obtain R_{CE} .

while the relay was closed. As expected, appreciable conduction did not occur until BV_{CEO} was reached. Each variation of V_{CC} provided a $V_{CE}-I_C$ data point. The slope of the locus of these points corresponds to R_{CE} , which was found to be $32\ \Omega$.

A set of characteristic curves, using the modified model, was generated to test the validity of the model and the values of the components used; these curves are plotted in figure 8. Each curve corresponds to an individual SPICE simulation, obtained by driving the base with a specific constant current. The collector current was monitored while V_{CE} was varied linearly to 150 V, over a 10 mS period. The value of the β was 116, obtained from figure 6b. The theoretical curves are generally in good agreement with the empirical curves shown in figure 6a ; the SPICE generated curves used a base current step of 1mA.

4.2. Thermal Base-Emitter Model

The breakdown model permits the flow of large reverse base currents. These, and the large forward currents that may also flow under high stress conditions, are unrealistic, requiring an addition to the model in order to limit these physically unsustainable currents.

A theoretical upper limit on the energy dissipated at the base can be calculated by assuming adiabatic heating; then the total thermal energy delivered to the base is $mC_p(T_{max}-T_0)$, where m is the mass of the transistor chip, C_p is the specific heat capacity of silicon, and $(T_{max}-T_0)$ is the difference between the maximum allowable junction temperature and the ambient temperature. For the specific case of the 2N6551 transistor, the chip size was estimated to be 0.1 cm by 0.1 cm by 0.02 cm thick; the density of silicon is 2.33 gcm^{-3} , so that the chip mass is $4.66\times 10^{-4}\text{ g}$. The maximum allowable junction temperature was assumed to be $175\text{ }^\circ\text{C}$, that is, a maximum junction temperature of $150\text{ }^\circ\text{C}$ above ambient ($25\text{ }^\circ\text{C}$) was permitted. These values and a specific heat capacity of $0.695\text{ Jg}^{-1}\text{K}^{-1}$ provide a maximum permissible base dissipation of 0.05 J. This calculation is valid for short times only because of the assumption of adiabatic heating. It is generally accepted [13] that, for the first 100 nS of applied stress heating is adiabatic, i.e., heat does not have time to diffuse; from 100 nS to approximately 10 μS , heating is quasiadiabatic, beyond this time steady-state heating occurs. An upper time limit of 1 μS , after which the adiabatic assumption is considered invalid, has been selected for this work. At times after 1 μS there will probably be enough energy transferred to the device package, so that the mass of the package can no longer be ignored.

Figure 8. SPICE generated characteristic curves for the 2N6551 transistor. The curves begin at zero base current, which is then incremented in 1 mA steps.

In order to determine whether maximum permitted base-emitter dissipation has been exceeded in any SPICE simulation, it is necessary to obtain the value of the energy simultaneously with the other circuit data. SPICE does not calculate power or energy dissipated in a circuit element (other than some initial values); additional circuit elements must be introduced. In this case, a network acting as an analog computer was used and the base-emitter energy dissipation obtained by integrating the base-emitter power dissipation. The network is shown in figure 9. The sources in this network are all dependent, permitting its connection to the main circuit by way of the reference node only; connected in this manner it cannot influence the main circuit in any way. FIBE is a dependent current source, whose value is equal to the current through source V_{BT} in the main circuit, that is, the effective base current. It creates a voltage across R_{100} equal in magnitude to the base current. EPINST is a two-dimensional voltage source, with all polynomial coefficients set to zero except the first order product term, which is unity. The value of EPINST is equal to the product of the voltage across R_{100} and the instantaneous base-emitter voltage calculated by SPICE for the transistor whose thermal behavior is being modeled. In the thermal model, this voltage is designated $V(1,0)$. EPINST is therefore equal to the instantaneous power dissipation at the base; it is fed to an analog integrator which provides the energy dissipated at the base-emitter junction. EPAVE is equal to the area under the EPINST curve, divided by the product $R_{OP}C_{OP}$, which was normalized to unity ($R_{OP}=1\text{ M}\Omega$, $C_{OP}=1\text{ }\mu\text{F}$), hence EPAVE yields energy. EPAVE is equal to the voltage at node 212, multiplied by a large constant, which was chosen to be 1000. No significant increase in accuracy was obtained for larger values of the constant, also large proportionality constants should be avoided in dependent sources, because large values can lead to non-convergence. Operation of the integrator was confirmed by using a known input, such as a sine wave, for which the expected output is known. The subnetwork provides a value of the energy dissipated at the base-emitter junction during the SPICE simulation, which can be compared with the maximum permissible value, established with the adiabatic thermal model. If a value exceeding the maximum is obtained, within $1\text{ }\mu\text{S}$, the device is assumed to have failed because of excessive temperature rise during stress. The adiabatic assumption provides a worst-case estimate, inasmuch as the junction can dissipate higher energies if heat is allowed to diffuse.

```

FIBE 0 101 VBT 1
EPINST 202 0 poly(2) 101 0 1 0 0 0 0 0 1
EPAVE 0 222 212 0 1k

```

Figure 9. Circuit used to obtain the energy dissipated at the base-emitter junction.

CHAPTER V

DEVELOPMENT OF THE SECOND BREAKDOWN MODEL

The second breakdown model must perform two main functions. The first is a diagnostic function; i.e., the model should recognize certain device currents and voltages, which in an actual device would be a prelude to second breakdown. When these currents and voltages occur, the diagnostic circuitry should activate the second breakdown model. The second function of the model is to mimic the behavior of an actual device entering second breakdown. The model must also remain active, once triggered, even after device currents and voltages have changed from their activating values, so that a rudimentary memory is required.

5.1. The Diagnostic Circuit

Before any diagnostic circuit can be implemented, second breakdown criteria must be established, i.e., the model must know what behavior constitutes breakdown. Reverse bias second breakdown is only completely defined by a relatively large parameter set, that is, forward and reverse base currents, collector current, collector-emitter breakdown voltage (BV_{CEO}), and the rate of fall of collector current (which is partially a function of the external collector inductance). The point at which a device enters second breakdown is determined by all of the above and also varies with device type.

5.1.1. Choice of Breakdown Criteria

A high fidelity model would require complete specification of all the second breakdown parameters. However, the model should have general applicability, i.e., it should not be necessary to perform an exorbitant set of measurements in order to obtain a simulation. With this consideration, the governing parameters were chosen to be collector current, I_C , and collector-emitter voltage, V_{CE} . The model may be easily expanded to include additional control parameters. The values of I_C and V_{CE} are obtained from a reverse bias safe operating area, RBSOA, tester [14], at drive levels corresponding to the desired simulation. In order to avoid problems with an "exact equality," the second breakdown model is activated if I_C and V_{CE} fall within certain value-windows.

5.1.2. Implementation of the Diagnostic Circuit

The approach used in the development of the diagnostic circuit was to design a simple logic circuit with rudimentary memory, that is, a circuit that would cause the level of an activating signal to change and remain changed.

A multiple-input NAND gate was chosen as the first logic element, the schematic of which is shown in figure 10. The output of this gate (the collector terminal) remains high unless the voltages at the cathodes of all four diodes, which constitute the control inputs, go high. If any of the four diodes is forward biased, i.e., if any cathode is low, then the transistor is depleted of base current as a result of the current being shunted through the forward biased diode; the voltage across DQ5 and the base-emitter junction is held at one forward voltage drop, which prohibits the transistor from turning on; hence, the collector is high.

The transistor and the diodes used in the NAND gate simulation are modified SPICE default versions. It was found that specifying a small base-emitter capacitance (0.1 pF), a base resistance (10 Ω) and the built-in base-emitter potential (0.6 V), for the transistor, considerably improved convergence and time of execution. Less significant, but nevertheless important, was the specification of a series resistance (0.5 Ω) and the built-in potential (0.6 V) for the diode model. Specification of these transistor parameters in the latter stages of the model was essential for convergence, because of the inherent feedback present. Failure to specify any transistor parameters results in a device theoretically capable of switching indefinitely quickly, which is incompatible with the use of feedback.

The four controlling inputs are related to I_C and V_{CE} . It was determined that the most straightforward method to detect I_C and V_{CE} entering a prescribed value window was to employ a "greater-than" and a "less-than" constraint for each. These are implemented by means of four dependent sources connected directly to the inputs. The value of each source is determined by a two-dimensional relationship between a source of constant value and either I_C or V_{CE} . There are four voltage sources of constant value, which designate the four threshold values. The voltage thresholds (V_{CE}) correspond directly to the voltage of the sources; the I_C thresholds in mA equal the voltage of the respective sources in volts; i.e., a threshold voltage of 40 V corresponds to a collector current of 40 mA. Greater accuracy was obtained by selecting the threshold value of current in milliamperes rather than in amperes; the input change required for a "hard" logic transition at the output is indeterminate by a few tenths of a volt, which in this case translates to an accuracy within a few

Figure 10. The first stage of the diagnostic circuit, consisting of a quad-input NAND gate.

tenths of a mA, as opposed to tenths of an ampere.

The positive voltages required to trigger the NAND gate are realized by setting the value of the dependent sources equal to V_{CE} or $I_C \cdot 1000$, less the threshold voltage (V_{th}), for the "greater-than" constraints; and V_{th} less V_{CE} or $I_C \cdot 1000$, for the "less-than" constraints. (Multiplication by 1000 converts I_C into mA.) Consider, for example, the input to DQ1, which implements the "greater-than" condition for V_{CE} . The dependent source connected to DQ1 is ECON (node 82 in figure 10) and is defined by the following line of code:

ECON 82 0 poly(2) 2 0 130 0 0 1 -1.

The value of this source is determined by V_{CE} [designated V(2,0)] and the "greater-than" threshold voltage for V_{CE} , V_{GV} [designated V(130,0)]. The final three digits of this line of code are the polynomial coefficients relating V_{CE} and V_{GV} . In this case the value of ECON is given by:

$$ECON = V_{CE} - V_{GV}.$$

Hence ECON is positive when $V_{CE} > V_{GV}$, satisfying one of the four necessary logic conditions. A similar arrangement is employed for the V_{CE} "less-than" constraint. Here the dependent source is ECON2 and the "less-than" controlling voltage is V_{LV} . The signs of the last two polynomial coefficients are interchanged in order to yield:

$$ECON2 = V_{LV} - V_{CE}.$$

ECON2 is positive when $V_{CE} < V_{LV}$, which satisfies another of the four logic conditions.

The dependent voltage sources governing the I_C constraints are established in an analogous fashion, except that it is necessary to convert I_C into an equivalent voltage. This is accomplished by using a dependent current source, whose value is equal to I_C and a 1 Ω resistor connected across it. In this manner the two dependent voltage sources, EICON and EICON2, have their values determined by a difference of voltages. The I_C constraints are satisfied when EICON and EICON2 are both positive, in direct analogy to the procedure described for V_{CE} , except that the polynomial

coefficient representing the voltage source equivalent to I_C is ± 1000 , depending on the constraint, to facilitate direct computation in mA.

When the V_{CE} and I_C constraints are satisfied, the logic level of the NAND gate changes. If the NAND gate output signal were directly to actuate the model, the transistor would go into second breakdown, resulting in dramatic changes in V_{CE} and I_C ; these would no longer satisfy the constraints and the output of the NAND gate would go high, deactivating the second breakdown model. This is clearly undesirable and must not be permitted; once triggered, the second breakdown model should remain in operation indefinitely. In order to prevent deactivation, the second breakdown model must either exhibit regenerative switching or the actuating signal must persist, once triggered, even though V_{CE} and I_C will exit their window values.

The second option was chosen for reasons which will be discussed later. This option requires a rudimentary memory, which is implemented by a flip-flop. A monostable multivibrator is a circuit that, once triggered, remains activated for a preset time period. If this period is large compared to the interval of simulation, then the monostable may be considered as being activated indefinitely, which is the form of response required for the actuating element.

The circuit schematic of the monostable is shown in figure 11. The circuit has one stable state with Q3 off and Q4 on. When a negative pulse is applied to the cathode of diode DM1, the base of Q4 is pulled negative, reverse biasing the base-emitter junction. This results in Q4 turning off, its collector voltage rising, which in turn causes Q3 to turn on and its collector potential to fall. Capacitor CM1 will momentarily maintain its charge and voltage, approximately V_{CC} . In the absence of the trigger pulse this causes the base of Q4 to fall to $-V_{CC}$. CM1 will attempt to recharge via RM2 to $+V_{CC}$, a total voltage of approximately $2V_{CC}$. However, once CM1 has charged sufficiently to raise the base of Q4 to 0.6 V, Q4 will turn on and the circuit will again enter the stable state previously described. The duration of the quasi-stable state is determined by the time required to charge CM1, which is given approximately by:

$$T = CM1 \cdot RM2 \cdot \ln(2).$$

The second breakdown model is designed to operate with an actuating signal of 1 V, representing normal circuit behavior, or 0 V, representing second breakdown. By choosing this signal to be the collector potential of Q3, a high voltage is obtained,

Figure 11. The final stage of the diagnostic circuit, consisting of a monostable multivibrator.

except when the circuit is triggered, resulting in a voltage close to 0 V. Hence the quasi-stable state is equated with second breakdown; selecting CM1 and RM2 to be 1 mF and 60 k Ω , respectively, activates this state for some 40 seconds, which is more than adequate for the times of simulation being used. In order for these voltages to approach more closely the ideal values of 1 and 0, V_{CC} was chosen to be 100.4 V and a potential divider network incorporating RM5 and RM6 used. Taking the final actuating signal from the RM5/RM6 node results in voltage values within two decimal places of 1 and 0.

Since the output of the NAND gate cannot assume voltages less than 0 V, the output of the gate is connected to the trigger of the monostable by way of an RC differentiator, as shown in figure 10. Utilizing stored charge, this converts the transition from high to low, into the required negative voltage.

It should be mentioned that calamitous convergence problems were encountered when the SPICE default model was used to represent Q4 and Q4. Specification of the parameters described earlier in this section was essential.

5.2. The Second Breakdown Model

Several circuit schemes and elements were examined before the final second breakdown model was chosen. In addition to being activated by a control signal, the model must satisfy two self-evident requirements from the viewpoint of the collector, base and emitter terminals of the transistor under test (TUT):

(i) under normal circuit operation, the model should not influence or degrade the ordinary performance of the TUT in any way.

(ii) once activated, the model should cause V_{CE} to fall rapidly to a value of a few tenths of a volt and I_C to assume a value constrained only by the circuit. Ideally, the collector-emitter terminals should appear as an ideal voltage source of approximately 0.1 to 0.2 V.

The simultaneous fall in V_{CE} and rise in I_C represents movement along a path of negative resistance. SPICE permits the specification of negative resistances; several attempts were made to use a negative resistance, in various schemes and in conjunction with other circuit elements, connected between the collector and emitter terminals. However, in addition to other difficulties, none of the simulations could be made to converge.

A second scheme was examined which utilized a thyristor connected in parallel with the collector-emitter terminals (anode to collector). Thyristors possess

excellent forward blocking capability, exhibiting a large impedance in the blocking mode and would satisfy requirement (i). When gated on, a thyristor becomes a unidirectional conductor (anode to cathode), with a small forward voltage drop. The anode current is constrained by external circuitry; that is to say, the behavior of a thyristor when gated on is very similar to that of a transistor entering second breakdown.

A SPICE compatible model of a thyristor [15] was considered for use as a second breakdown element. One of the SPICE parameters, which can be derived for a specified thyristor from manufacturer's data sheets, determines the forward breakover voltage of the device. One possibility was the specification of the breakover voltage, turn-on occurring at a prescribed value of V_{CE} by means of an overvoltage. Another possibility was to use the output of the NAND gate (a thyristor latches and hence the monostable is not necessary) to trigger the thyristor, via a transistor inverter. Convergence was again a problem, and these simulations were abandoned in favor of a simpler model.

The successful model, for which the diagnostic circuit was tailored, consists of a dependent voltage source in series with a diode. This model, with the avalanche breakdown model included, is shown in figure 12. The dependent source is ESEC (in the lower left-hand circuit) and is described by the following line of code:

ESEC 132 0 poly(2) 2 0 127 0 0 0 0 0 1.

The value of ESEC is determined by a two-dimensional relationship between V_{CE} [V(2,0)] and the final actuating signal from the monostable circuit, V(127,0). The last five digits of the line of code are the polynomial coefficients which cause ESEC to assume the value:

$$ESEC = V_{CE} \cdot V(127,0).$$

Under normal circuit conditions, V(127,0) is 1 V, so that ESEC is equal to V_{CE} . This results in the voltage across DSEC (also in the lower left-hand circuit) being close to zero; consequently, no current flows through this circuit branch and the model in no way influences circuit behavior. When V_{CE} and I_C enter their prescribed value windows, the monostable is triggered and V(127,0) falls to about 0 V. This sets the value of ESEC to approximately 0 V, where it will remain indefinitely.

Figure 12. The diagnostic circuit, including avalanche and second breakdown models (but not the thermal model).

DSEC is specified by the same diode parameters as used in the diagnostic circuit; hence V_{CE} is held at the anode-cathode voltage of the diode, which is typically less than one volt. I_C is unconstrained by the model.

The active elements used in the NAND gate and the monostable models are almost ideal; i.e., the diagnostic circuit changes output state rapidly. In an actual device, the second breakdown transition occurs during a very small time period (tens of nS), so that the model faithfully represents the temporal aspect of breakdown.

While under development, the diagnostic circuit was connected to the simulated circuit only through unidirectional dependent sources and the reference node, hence, the two circuits were effectively electrically isolated. As a final requirement to permit greater ease of use, the complete avalanche, diagnostic and second breakdown circuits were written as a subcircuit. A subcircuit defined in a SPICE simulation is analogous to a subroutine in an upper level language. This subcircuit will henceforth be referred to as the "second breakdown subcircuit."

5.3. Use of the Second Breakdown Model

The second breakdown subcircuit contains all augmentations to the SPICE BJT model, with the exception of the thermal model. Internal subcircuit nodes are inaccessible to the user, once defined as such, consequently, the thermal model must remain a part of the circuit under analysis, in order to permit the instantaneous energy to be monitored.

Subcircuits are defined in SPICE using the .SUBCKT card. A listing of the breakdown subcircuit is given in Appendix B. The numbers assigned to each node in a subcircuit are local to that subcircuit. This permits the subcircuit listing to be inserted immediately preceding the .END statement of the main SPICE listing. The subcircuit requires access to the corresponding V_{CE} and I_C of each transistor to be modeled. Access to V_{CE} is assured by defining and referencing the subcircuit by a set of nodes that includes the collector and emitter nodes. In order to access collector currents the subcircuit cannot simply refer to a designated collector current monitor in the main circuit listing, as there may be several of these. The subcircuit monitors the collector currents by inserting its own current monitors. In order to accomplish this an open-circuit must be specified in the main SPICE listing, immediately adjacent to the collector node, i.e., the circuit element that would normally connect to the collector node terminates in an open-circuit, which is designated by the unique node number, NS. The subcircuit is defined as SECBRK and is invoked for

each BJT in the main circuit by means of a subcircuit calling statement, which has the general form: X NS NC NB NE SECBRK. The calling statement must begin with the letter X; NC, NB and NE are the collector, emitter and base node numbers, respectively, corresponding to a BJT in the main circuit. Electrically nodes NS and NC are identical; the subcircuit inserts a 0 V DC source between these nodes (designated VQ1 in the subcircuit), which SPICE uses to monitor the collector currents and to electrically complete the circuit. (Additional sources are required for user access to the collector currents.) Apart from the specification of these open-circuits, the SPICE code representing the circuit to be investigated is written without consideration for the breakdown model. A separate calling statement is required for each BJT in the main circuit. These calling statements are the only reference to the subcircuit, that are contained within the main SPICE listing.

The subcircuit requires that eight breakdown parameters be entered; identified as VALUE 1 through VALUE 8, in the subcircuit listing. VALUE 1 through VALUE 4 are associated with avalanche breakdown and correspond to the following parameters:

VALUE 1: collector-emitter, dynamic breakdown resistance, R_{CE} ;

VALUE 2: open base, collector-emitter breakdown voltage, BV_{CEO} ;

VALUE 3: emitter-base, dynamic breakdown resistance, R_{EB} ;

VALUE 4: open collector, emitter-base breakdown voltage, BV_{EBO} .

These parameters were fully discussed in Section 4.1, (junction breakdown).

VALUE 5 through VALUE 8 are associated with second breakdown; however, the avalanche breakdown parameters are also required for authentic second breakdown modeling. The remaining four breakdown parameters are defined as follows:

VALUE 5: greater-than threshold for V_{CE} , V_{GV} ;

VALUE 6: less-than threshold for V_{CE} , V_{LV} ;

VALUE 7: greater-than threshold for I_C , V_{GI} ;

VALUE 8: less-than threshold for I_C , V_{LI} .

The four second breakdown parameters are obtained empirically. In this work this data was obtained using a reverse bias safe operating area (RBSOA) transistor tester[8]. This piece of apparatus permits a single transistor to be driven into second breakdown repeatedly, while avoiding catastrophic device failure. The operation of this tester will be further discussed in Chapter VI.

CHAPTER VI

TEST AND EVALUATION CIRCUIT

The circuit used to evaluate the performance of the various second breakdown models is shown in figure 13. This circuit was chosen on the basis of simplicity and because it essentially represents the RBSOA tester. The TUT is in the common emitter configuration, with a series inductor-resistor combination as the load. Source E_B provides the circuit excitation; the form of E_B is also shown in figure 13 and is obtained from a piecewise linear source.

A specific forward or reverse base current is obtained by adjustment of the amplitudes of the forward (V_F) and reverse (V_R) voltage pulses and resistor, R_S . Difficulties may be encountered if it is attempted to drive the base directly with a current source, as SPICE will insist upon the specified reverse base current flowing, which is often not feasible.

The voltage, V_F , assumes an initial constant value, at which it remains for the duration of the forward pulse. SPICE uses this constant value of V_F to compute a constant initial base current. This ensures that the inductor is initially in a steady-state energized condition. If V_F were to assume an initial value of zero volts, simulation times of the order of 1 mS would be required in order to reach a steady-state collector current. This is undesirable inasmuch as computation times can become excessive when a small time step, i.e., high time resolution, is desired. A steady-state condition is also desirable, because it permits ease of repeatability and correlation with the experimental data.

Turn-off of the transistor is initiated by the reverse voltage pulse. The value of V_R was chosen to be less than the emitter-base breakdown voltage at all times; this is analogous to the RBSOA tester, in which the base-emitter voltage is clamped to avoid breakdown. Large values of reverse current were obtained by setting V_R to its maximum allowable value and then decreasing R_S . This procedure does not impede adjustment of the forward base current, as V_F is unconstrained. The value of reverse base current is defined as the peak value observed. This value may persist at a constant level, depending upon the quantity of stored charge in the base region, from which the current originates.

After the stored charge has been removed from the base region, the transistor begins to turn off and the collector current to fall; the inductor, acting as a current

Figure 13. The inductive test and evaluation circuit.

source, drives the collector voltage toward its avalanche value. The simultaneous presence of both high collector current and high collector voltage can result in second breakdown.

CHAPTER VII

TEST CIRCUIT RESULTS

7.1. Empirical Results

The circuit of figure 13, with the following differences, generally describes the operation of the RBSOA tester:

(i) There is no distinct collector resistance, R_C represents the finite winding resistance possessed by the 1 mH inductor and other resistive elements associated with the non-ideal power supply.

(ii) Source E_B and resistor R_S are replaced by a high resolution current drive. The forward and reverse current pulses persist for 5 mS each, with independently variable amplitudes.

(iii) In order to allow repetitive measurements on a single device without catastrophic failure, a protection circuit is employed. The rapid fall of V_{CE} , associated with breakdown, induces a displacement current in a detection capacitor, which triggers a high speed crowbar; the collector current is then diverted through the crowbar to an energy dump.

A complete characterization of the 2N6551 device (see Appendix A for manufacturer's data sheet and SPICE parameters) was obtained using the RBSOA tester. The characterization required some 400 measurements for a logarithmic range of forward and reverse base currents, from 1 mA to 100 mA. Forward drives of 200 mA were used with reverse base currents up to 60 mA, at which point the device catastrophically failed.

Only types B and C breakdown were observed in this work. The majority of breakdowns occurred as type C, with type B being observed only for reverse base currents of 6 mA or less and forward drives of 10 mA or less. At the lowest forward drives and at all reverse stress levels, with the exception of an intermediate range, the device turned off safely.

An example of safe turn-off is shown in figure 14. The forward base drive of 6 mA results in 720 mA of collector current just prior to the application of the 1 mA reverse base pulse. As the device turns off, I_C falls linearly, while V_{CE} increases to a current dependent point on the BV_{CEO} curve (approximately 150 V), remaining almost constant for the duration of turn-off. This curve is typical of the safe turn-off curves observed in this work. The width of the V_{CE} pulse is primarily dependent

Figure 14. Example of safe turn-off. The forward and reverse base drives were 6 mA and 1 mA, respectively. The scales are V_{CE} (pulsed shaped curve), 50 V, and I_C , 200 mA; the horizontal scale is 1 μ s; all per large division.

upon the time required for I_C to fall to zero.

As the base stress level is increased the device is no longer able to turn off safely. Type B breakdown is typically observed in this situation. Figure 15 shows an example of type B breakdown, for which the forward and reverse base drives were 4 mA and 2 mA, respectively. I_C falls from its initial value of 640 mA to a second breakdown value of 470 mA (the slight "glitch" in I_C will be discussed in Section 7.3), while V_{CE} increases to BV_{CEO} , where it remains constant until breakdown. Prior to breakdown, the V_{CE} and I_C curves are reminiscent of safe turn-off and indeed, the device appears to be turning off safely.

An example of breakdown which is not distinctly type B or C is shown in figure 16. These curves represent a transition region from type B to type C. I_C remains essentially constant at 1.3 to 1.4 A, while V_{CE} appears to level off at a value close to BV_{CEO} before breakdown occurs. The forward and reverse drives were 50 mA and 9 mA, respectively.

At the highest levels of forward and reverse base current, type C breakdown was observed, of which figure 17 is a clear example. I_C remains essentially constant at 1.54 A, while V_{CE} increases, but does not attain a constant value, prior to second breakdown. The forward and reverse drives were 70 mA and 40 mA, respectively.

7.1.1. Effects of BJT Parameters on Turn-Off

The switching curves obtained for the 2N6551 device show considerable variation from device to device. This implies that one, or several, of the BJT parameters also varies.

Some BJT parameters may have a relatively slight effect on switching performance, while others--and combinations of these--may have dramatic effects. One parameter exhibiting considerable variation is BV_{CEO} ; its value was found to vary from 114 V to 138 V, with a mean of 125.0 V and a standard deviation of 7.01 V, in the 15 2N6551 transistors measured.

The diversity in the observed switching waveforms is particularly evident in the region between safe turn-off and type B breakdown. Figure 18 shows two sets of waveforms obtained using a base current of 3 mA forward and 2 mA reverse, on two different devices. Figure 18a shows safe turn-off (the increase in V_{CE} , after BV_{CEO} has been reached, may be a prelude to type A breakdown, although this is speculation), whereas the same drive results in type B breakdown, in a different device, as shown in figure 18b. The device used to obtain the safe turn-off curves had

Figure 15. Example of type B breakdown. The forward and reverse base drives were 4 mA and 2 mA, respectively. The scales are V_{CE} (lower curve), 50 V, and I_C , 100 mA; the horizontal scale is 500 nS; all per large division.

Figure 16. Example of type B/C breakdown. The forward and reverse base drives were 50 mA and 9 mA, respectively. The scales are V_{CE} (lower curve), 50 V. and I_C , 0.5 A; the horizontal scale is 200 nS; all per large division.

Figure 17. Example of type C breakdown. The forward and reverse base drives were 70 mA and 40 mA, respectively. The scales are V_{CE} (lower curve), 50 V, and I_C , 0.5 A; the horizontal scale is 200 nS; all per large division.

a.

b.

Figure 18. V_{CE} (lower curves) and I_C , obtained for two different devices, using forward and reverse base drives of 3 mA and 2 mA, respectively. The scales are (for both a. and b.) 50 V and 100 mA for V_{CE} and I_C , respectively, and the horizontal scale is 500 ns; all per large division.
 a. Safe turn-off, $BV_{CEO}=114$ V.
 b. Type B breakdown, $BV_{CEO}=138$ V.

a BV_{CEO} of 114 V; for the type B breakdown, 138 V. Prior to second breakdown, V_{CE} and I_C behave similarly for both devices; however, V_{CE} plateaus at a higher level in the type B case, reflecting the higher BV_{CEO} associated with that device.

During safe turn-off, the power dissipated, P_d , in the device may be approximated by

$$P_d = BV_{CEO} \cdot I_C(t).$$

Considering the BV_{CEO} parameter in isolation, this implies that devices with low values of BV_{CEO} will have to dissipate less energy in a given time interval, Δt , during safe turn-off, than those devices possessing a higher BV_{CEO} voltage. This probably accounts for the events illustrated in figures 18a and 18b; here the device with the lower BV_{CEO} is able to sustain the lower energy and turn off safely, whereas the device with the higher value of BV_{CEO} , dissipates more energy per Δt , resulting in breakdown. While a low value of BV_{CEO} may be desirable, other factors may be influencing these sets of curves; for example, the initial value of I_C is 55 mA or approximately 12% higher in the type B case, as opposed to the safe turn-off curves. The higher initial value in the type B case might be a consequence of the higher BV_{CEO} , a higher value of β , a lower value of $V_{CE(sat)}$, or a combination of these and other unidentified parameters. Consequently the exact extent to which BV_{CEO} alone influences safe turn-off is unknown.

Some slight variations in the curves obtained close to the type B/C transition are observed, although not to the degree observed with the transition from safe turn-off to type B breakdown.

7.2. Simulation Results

SPICE simulations were performed on the test circuit described in Chapter VI and illustrated in figure 13. The complete circuit code, including the avalanche and second breakdown models corresponding to this circuit and the 2N6551 transistor used for these simulations, is given in Appendix C.

The effectiveness of the breakdown models may be best illustrated by a series of simulations, involving successively increasing levels of model sophistication. The utility of each level of breakdown model will be demonstrated by examining its ability authentically to model and predict safe turn-off, type B and type C breakdowns.

The lowest level of model sophistication involves only the library BJT model contained within SPICE. The next higher level of model includes both the SPICE BJT model and the avalanche breakdown model. The highest level of model sophistication is the complete second breakdown model, which contains both of the lower order models. The thermal model was not included in any of these simulations, inasmuch as it was not required for a comparison with the experimental data, which were obtained with the base-emitter junction clamped to a value below the base-emitter breakdown voltage. Emitter-base junction thermal effects are not considered important in this case.

7.2.1. The SPICE BJT Model

The SPICE code representing the test circuit, modeled using only the SPICE BJT model, may be obtained from Appendix C by deleting the second breakdown subcircuit and calling statement.

Figure 19 shows V_{CE} and I_C obtained for a base drive of 6 mA forward and 1 mA reverse current. As is the case for all of the simulated results contained in this work, reverse base current begins to flow at a time which is within several nS of 5 μ S. During turn-off, I_C falls linearly from its initial value of 693 mA, while V_{CE} reaches a peak of approximately 280 V, several μ S into turn-off. The initial value of V_{CE} was 9.45 V, indicating that the device was not initially saturated.

The drive levels used to generate figure 19 correspond directly to those used experimentally to obtain figure 14. This permits a direct comparison between the two figures; as can be seen, although the forms of I_C are similar, those of V_{CE} are not. The magnitude of V_{CE} , in the simulated result, is almost twice that observed empirically (greater than twice the value of BV_{CEO}); it also does not exhibit a trapezoidal form. This implies that the SPICE BJT model (the higher order version, not merely the default model) is ineffective for accurately modeling safe turn-off in this type of circuit.

The SPICE BJT model does not contain a procedure to model second breakdown and it should therefore not be expected to do so; however, the library model produces erroneous safe turn-off results. Consequently, this model cannot be used to predict accurately the form of V_{CE} and I_C prior to breakdown. The absence of a restraining mechanism for V_{CE} results in a device that can theoretically condition arbitrarily large amounts of power.

INDUCTIVE SWITCHING WITH BJT MODEL ONLY. SAFE TURN OFF--2N6551 DEVICE

Figure 19. SPICE generated safe turn-off, using the library BJT model. The forward and reverse base currents were 6 mA and 1 mA, respectively.

7.2.2. The Augmented SPICE Model

The augmented model includes the additional avalanche and junction breakdown circuitry, in addition to the BJT library model contained within SPICE. In order to use this level of model, all lines of code in the second breakdown subcircuit are deleted, except for the avalanche circuitry section. Alternatively unrealizable activation values of I_C and V_{CE} may be specified, ensuring that the second breakdown model cannot be activated.

Figure 20 shows V_{CE} and I_C obtained for a base drive of 6 mA forward and 1 mA reverse current; this corresponds to the empirically obtained safe turn-off curves of figure 14. As turn-off begins, I_C falls linearly from an initial value of 693 mA to zero, with a slight negative undershoot. During this time V_{CE} rises to an essentially constant value of from 116 to 130 V, where it remains for approximately 6 μ s, until I_C has first attained a zero value of current. V_{CE} is now effectively constrained by the current dependent BV_{CEO} curve, i.e., the avalanche circuitry. The steady state value of V_{CE} approaches the value of $V_{CC} - 15V$. The simulated curves compare favorably to the analogous experimental results shown in figure 14. This has been found to be generally true of other simulated safe turn-off curves and consequently, the augmented SPICE model is considered adequate to model safe turn-off authentically.

Prior to actual second breakdown, both I_C and V_{CE} resemble safe turn-off. The second breakdown curves follow the locus of safe turn-off until breakdown occurs, which depends upon the levels of drive stress. Type C breakdown, associated with high stress, occurs during initial turn-off, whereas type B breakdown occurs after V_{CE} has plateaued. Since the augmented SPICE model accurately models safe turn-off, it may be used to predict the form of V_{CE} and I_C prior to breakdown.

Condition (ii) of Section 5.2, which described the development of the second breakdown model, cited that the second breakdown model should not influence circuit behavior unless activated, and when activated, should mimic second breakdown. Hence, accurate modeling of events prior to second breakdown by the augmented model is essential for correct operation of the second breakdown model; otherwise the second breakdown model may never encounter the activation values of V_{CE} and I_C , in which case the model would not be activated and breakdown would not be predicted.

Modeling the junctions independently, as discussed in Section 4.1, results in similar curves to those obtained using only the SPICE BJT model. This is not

Figure 20. SPICE generated safe turn-off, using the library BJT model, augmented by the avalanche breakdown model. The forward and reverse base currents were 6 mA and 1 mA, respectively.

surprising, inasmuch as the collector-base breakdown voltage is approximately 300 V and the reverse base-emitter voltage is limited to a maximum of 9 V, resulting in a collector-emitter breakdown voltage of approximately 290 V.

7.2.3. The Second Breakdown Model

The second breakdown model may be considered as a discrete model, inasmuch as it is either active or inactive. In the inactive state circuit behavior is modeled by the augmented SPICE model, in which case the second breakdown model is uninvolved. Once activated, V_{CE} is held constant at a small voltage, while I_C assumes a value consistent with this.

Figure 21 shows V_{CE} and I_C , corresponding to 4 mA forward and 2 mA reverse base current. The upper and lower sets of curves are identical, except that the lower curves are presented on an expanded time scale for increased resolution. These curves were generated using identical drives as those used to produce the experimental curves of figure 15, permitting a direct comparison between the two. Under these conditions type B breakdown was observed to occur at $V_{CE}=132$ V and $I_C=470$ mA. Based on this data the $V_{CE}-I_C$ activation window was chosen to be $128 \text{ V} < V_{CE} < 136 \text{ V}$ and $455 \text{ mA} < I_C < 485 \text{ mA}$. Using this data, SPICE predicts second breakdown at approximately 1.5 μs after turn-off begins (this is indicated by the rapid fall in V_{CE} at about 6.5 μs), as shown in figure 21. The values of V_{CE} and I_C , at breakdown, are 128.6 V and 484.5 mA, respectively.

Prior to second breakdown V_{CE} is held reasonably constant, while I_C falls linearly. These simulated results demonstrate a close similarity to the empirical curves, both in terms of magnitudes and time to second breakdown, which occurs approximately 1.25 μs after turn-off begins in the experimental measurement. Comparisons between the predicted and experimental results after second breakdown, is not meaningful inasmuch as the collector current is crowbarred in the experimental test arrangement, while being determined by external circuitry in the simulations.

Figure 22 shows the simulated forms of V_{CE} and I_C obtained for drive currents of 50 mA forward and 9 mA reverse current; these correspond to the the empirical curves of figure 16. Again the upper and lower sets of curves are identical, except for an expanded time scale used for the lower set. Using these levels of stress, type B/C breakdown was empirically observed at $I_C=1.325$ A and $V_{CE}=120$ V. Based on this data the $V_{CE}-I_C$ activation window was chosen to be: $118 \text{ V} < V_{CE} < 122 \text{ V}$ and

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Figure 21. SPICE generated type B breakdown (the lower curves are displayed with increased time resolution). The forward and reverse base currents were 4 mA and 2 mA, respectively.

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Figure 22. SPICE generated type B/C breakdown (the lower curves are displayed with increased time resolution). The forward and reverse base currents were 50 mA and 9 mA, respectively.

$1.3\text{ A} < I_C < 1.35\text{ A}$. Utilizing these values, SPICE predicted second breakdown at about 150 nS after initial turn-off, at which point V_{CE} and I_C were equal to 118.6 V and 1.343 A, respectively. The breakdown is categorized as type B/C, because in both the simulated and experimental results V_{CE} sustains at BV_{CEO} for only a very small interval of time (tens of nS). Again, as with the type B breakdown, the SPICE prediction agrees favorably with the experimental results.

Figure 23 shows the simulated forms of V_{CE} and I_C produced for drive currents of 70 mA forward and 40 mA reverse; the empirical equivalents are shown in figure 17. As previously, the lower set of curves are displayed on an expanded time scale. With these levels of stress the RBSOA tester indicates type C breakdown at $V_{CE}=120\text{ V}$ and $I_C=1.5\text{ A}$ (the value of I_C at breakdown is ostensibly its initial steady state value of 1.54 A). Based on this data the $V_{CE}-I_C$ activation window was chosen to be: $118\text{ V} < V_{CE} < 122\text{ V}$ and $1.47\text{ A} < I_C < 1.53\text{ A}$. Using these parameters in the second breakdown model, SPICE predicted type C breakdown at approximately 75 nS after initial turn-off, at which point V_{CE} and I_C were equal to 118.4 V and 1.523 A, respectively; this is in good agreement with the experimental result. Comparison of figures 22 and 23 shows that the rate of increase of V_{CE} during turn-off is much greater in the latter case, as opposed to the former, i.e., in figure 23 the device initially turns off at twice the rate of that shown in figure 22. This is a direct consequence of the increased reverse base current used in the latter simulation.

The three specific simulations described above yield results which compare excellently with the equivalent experimental results. This has been found to be generally true for other type B, B/C and C breakdown curves, with the exception of some anomalous results. These results are discussed in the next section.

7.2.4. Anomalous Results

As discussed previously the initial rate of increase of V_{CE} , during turn-off, generally increases with increasing reverse base current. Some anomalous results have been observed for large reverse base currents, an example of which is shown in figure 24; the forward and reverse base currents were 20 mA and 70 mA, respectively. In this case, V_{CE} exhibits the form of type C breakdown, however, uncharacteristically, I_C falls at a significant rate. This fall of I_C is not predicted by SPICE and is believed to be a consequence of the rapid increase of V_{CE} , i.e., the high dV_{CE}/dt .

INDUCTIVE SWITCHING WITH 2nd BREAKDOWN 51

2N6551 DEVICE

Figure 23. SPICE generated type C breakdown (the lower curves are displayed with increased time resolution). The forward and reverse base currents were 70 mA and 40 mA, respectively.

Figure 24. Anomalous second breakdown behavior. The forward and reverse base currents were 20 mA and 70 mA, respectively. The scales are V_{CE} (lower curve), 50 V, and I_C , 200 mA; the horizontal scale is 200 nS; all per large division.

Small values of parasitic capacitance may have a significant effect on circuit behavior, when accompanied by high values of dV/dt . The effects of two types of parasitic capacitances on the performance of the test circuit of figure 13 were investigated. Initially, the effects of parasitic capacitance in parallel with the collector and emitter (ground) nodes of the transistor were investigated. A series of simulations were performed for various values of capacitance, ranging from 0 pF to 10000 pF, approximately logarithmically. As the value of capacitance was increased a trend was observed: the rate of increase of V_{CE} and fall of I_C decreased. The highest rates of dV_{CE}/dt and fall of I_C were observed in the absence of any capacitance, indicating that parasitic capacitance between the collector and the emitter nodes is not responsible for the atypical behavior of I_C .

Inter-winding parasitic shunt capacitance associated with the inductive load was next considered. Approximate calculations for a value of parasitic capacitance, based on figure 24, produced a value of about 700pF. These calculations required several assumptions, such as assuming constant values for dV_{CE}/dt and the fall of I_C , and also neglecting the effects of other parasitic elements. Consequently the calculated value of 700 pF provides an initial estimation only. Attempts to measure C_{PAR} produced somewhat ambiguous results, probably because there are actually several capacitances associated with the inductor. However, while not firmly corroborating the calculations, the measurements do not categorically disprove them. The effects of this capacitance on circuit performance were examined for a range of capacitor values, henceforth called C_{PAR} , ranging from 0 pF to 1000 pF. The results of these simulations are shown in figures 25a and 25b; figure 25a shows that dV_{CE}/dt is decreased as C_{PAR} is increased (although not to the extent observed with a parasitic collector-emitter capacitance), while figure 25b shows that I_C suffers an initial rapid fall, followed by an increase, i.e., a "notch" effect. The values of base current used to generate these curves, are identical to those used to generate the empirical curves of figure 24. Prior to breakdown, the form of I_C and V_{CE} exhibit similar form to that of the experimental data.

Figure 26 shows two sets of curves, both generated using the same base currents of 20 mA forward and 70 mA reverse: figure 26a shows V_{CE} and I_C , generated in the absence of C_{PAR} and with the second breakdown model inactive. Figure 26b shows curves generated in an identical fashion to figure 26a, except that C_{PAR} is included and set to 700 pF. In figure 26a the form of I_C , as turn-off begins, does not correspond to the experimental result, whereas the fall of I_C shown in figure

Vce AS A FUNCTION OF WINDING CAPACITANCE 54

Ic AS A FUNCTION OF WINDING CAPACITANCE

Figure 25. The effects of parasitic capacitance, associated with the inductor, on V_{CE} and I_C , during turn-off. Forward and reverse base currents were 20 mA and 70 mA, respectively.

a. V_{CE} .

b. I_C .

INDUCTIVE SWITCHING WITH AVAL.

55

a.

b.

Figure 26. V_{CE} and I_C obtained for a base drive of 20 mA forward, and 70 mA reverse base current.

a. The augmented SPICE model only.

b. The augmented SPICE model with 700 pF parasitic capacitance shunting the inductor.

26b does exhibit a similar initial response. This, and other simulations, indicates that the anomalous behavior of I_C is probably, attributable to parasitic interwinding capacitance associated with the inductor.

According to figure 24, second breakdown is observed to occur experimentally at $V_{CE}=130$ V and $I_C=880$ mA. If activation values of V_{CE} and I_C are chosen based on these values, the second breakdown model will not predict behavior consistent with the measurements, unless an approximately correct value of C_{PAR} is specified. This is not surprising, inasmuch as the SPICE code and the test circuit do not correspond, at this high level of reverse base current, without the addition of C_{PAR} . Figure 27 shows the second breakdown curves corresponding to figure 26b, with activation values of $110 \text{ V} < V_{CE} < 130 \text{ V}$ and $I_C < 1.0 \text{ A}$. The value of C_{PAR} (700 pF) represents an estimation; therefore, the form of V_{CE} and I_C do not correspond directly to experiment. This necessitates a larger than usual activation window, in this case the I_C constraint is relatively lax. Comparison of figure 27 with the experimental curves of figure 24 reveals reasonably strong correlation between the two. Again, comparison between the two after breakdown ($5.16 \mu\text{S}$) is not meaningful inasmuch as the collector current is crowbarred in the RBSOA tester. The SPICE curves show a rapid increase of I_C at second breakdown, owing to the inherently large values of negative dV_{CE}/dt associated with this event.

The slight notch observed in the collector current of the type B breakdown shown in figure 15 is probably also due to the effects of C_{PAR} . However, the majority of the experimental results observed do not exhibit anomalous I_C behavior and the second breakdown model can predict authentic results. The impact of C_{PAR} varies with dV_{CE}/dt ; its effects appear to be insignificant for the lower values of dV_{CE}/dt , but become evident as the device turns off more rapidly. The highest values of dV_{CE}/dt are observed for intermediate values of forward base currents and reverse base currents larger in magnitude than these. While the inclusion of C_{PAR} is able to explain the anomalous results, its presence does affect all of the simulations, to some degree. Consequently, although C_{PAR} appears to be the dominant parasitic element influencing the results described in this section, it is probable that circuit behavior is influenced by a complex combination of parasitic elements.

7.2.5. Accuracy of the Simulations

Early simulations produced some erroneous results; authentic results were assured by forcing SPICE to use the Gear method of numerical integration. The

Figure 27. SPICE generated second breakdown curves with 700 pF of parasitic capacitance shunting the inductor. The forward and reverse base drives were 20 mA and 70 mA reverse, respectively.

default routine used by SPICE is the trapezoidal method. (Higher orders of Gear's method are multi-step algorithms, i.e., they require more than just the previously computed data point in contrast to the single-step trapezoidal method.)

Figures 28a and 28b contrast the results obtained from two identical simulations, except that in (a), SPICE used the default integration method and in (b), the Gear method. A ripple is clearly evident in the upper curve of figure 28a; this is an artifact. Subsequently, the Gear method was used throughout this work, which eliminated this problem.

The variation of the BJT parameters and second breakdown curves from one device to the next (Section 7.1.1) places a limit on the accuracy of the simulated results. For example, BV_{CEO} varied by greater than $\pm 10\%$ of its mean value in the 15 devices measured, this variation translates to the empirical second breakdown curves. Consequently, SPICE predictions within 10% of the experimental data should be considered adequate.

The activation values chosen for the second breakdown model must lie along the locus of safe turn-off in order for the model to be activated. Again, because of scatter in the experimental data, the windows should be chosen quite large. As a general procedure, it is suggested that a symmetric window be chosen for both V_{CE} and I_C . For example, suppose the second breakdown value of V_{CE} has been experimentally determined to be V_S ; then the V_{CE} activation window should be chosen to be $(V_S - \Delta V) < V_{CE} < (V_S + \Delta V)$. ΔV should initially be quite large; if second breakdown is predicted, ΔV and the corresponding ΔI_C should be reduced, in order to achieve greater accuracy. If this procedure is repeated successively, a point will be reached when second breakdown is not predicted. In this case, the window is too narrow and the previous activation values of V_{CE} and I_C must be used. Using this procedure, the prediction of breakdown is assured with the greatest possible accuracy, i.e., V_{CE} and I_C correspond as closely as possible to the empirical values. This procedure was used to generate the results herein reported.

INDUCTIVE SWITCHING WITH AVAL. 2N6551 DEVICE

a.

INDUCTIVE SWITCHING WITH AVAL. 2N6551 DEVICE

b.

Figure 28. SPICE generated switching waveforms.
a. Using the trapezoidal method of integration.
b. Using the Gear method of integration.

CHAPTER VIII

CONCLUSIONS

This work clearly demonstrates the failure of SPICE to predict correctly voltages and currents associated with the transient response of circuits containing both energy storage elements and active devices, without important additions to the library models. Consequently, SPICE cannot be used to predict failure or failure thresholds for these types of circuits with any degree of confidence.

Considerable improvement in the simulations is obtained with only the addition of the avalanche breakdown circuitry. If excessive reverse base-emitter voltages are avoided, the augmented or avalanche BJT model requires the specification of only two parameters: BV_{CEO} and R_{CE} . Inclusion or specification of these two elements is sufficient to limit the collector-emitter voltage to reasonable values. Limiting reverse base-emitter voltages to values of less than the breakdown voltage of the junction allows BV_{EBO} to be arbitrarily chosen to be an unrealizably high voltage; this effectively removes the base-emitter breakdown circuitry from the model and eliminates the specification of two model parameters. It also removes the necessity of using the thermal base-emitter model; excessive energy dissipation at the base-emitter junction is not encountered under these circumstances. The augmented BJT model accurately models safe turn-off and the events prior to second breakdown, which SPICE alone cannot do.

The second breakdown model introduces a novel concept to circuit-level modeling; viz., the use of dependent subcircuits (an analogous extension of the use of dependent sources), for the diagnosis, control and implementation of second breakdown. In this manner the sophisticated features of the SPICE code are fully utilized. The second breakdown model has been shown to operate correctly and to model this event authentically. Prior to second breakdown the model may be considered inactive, voltages and currents being predicted by the augmented BJT model. The second breakdown model is activated when prespecified values of V_{CE} and I_C are encountered, consequently the model is as accurate as these empirical data points. The switching curves obtained for the 2N6551 device (and indeed any device), show some variation from one device to the next. The variance of the experimental data and curves, implies that a similar variance is to be expected in the simulated results. This variance is inherent in measured second breakdown and

therefore should be considered inherent in the simulations.

The empirical type B curves resemble safe turn-off prior to breakdown, lending support to the modeling of second breakdown as a discrete bilevel phenomenon, whereby the model assumes one of two states: active or inactive. The observed second breakdown event (a rapid transition from a high to low value of V_{CE}), is reflected in the model.

Although it might be possible to predict second breakdown from observation of I_C and V_{CE} alone, the complete model allows the effects on a circuit to be examined following the appearance of second breakdown in any one device. In this manner, second order events, such as failure of a device in response to failure of another device may be predicted; such a prediction could probably not be made on the basis of current and voltage observations alone. However, it is essential to note that any circuit modeling requires pre-specification of second breakdown values and windows before any predictions can be obtained; that is, an experimental parameter space must be obtained for every type of transistor in a circuit before effective transient circuit modeling can be performed. Variations in experimental results may be averaged, particularly if these are small.

Section 7.1.1 discussed the variation of BV_{CEO} from one device to the next. Since during safe turn-off and prior to type B breakdown, the power dissipated by the device is given approximately by: $BV_{CEO} \cdot I_C(t)$, it was suggested that the devices with the lowest values of BV_{CEO} , would sustain the least amount of energy dissipation, in a given time interval, Δt . After some time (approximately 1 μ S) the device is able to conduct heat from the semiconductor chip to the surrounding package and heat sink. A device may be able to sustain low energy levels for some time, but not higher energies, even for shorter times. Consequently, low values of BV_{CEO} are conducive to safe turn-off; however, these are undesirable from a circuit point of view, particularly power circuits.

A zener diode and resistor (cathode to collector) connected in parallel with the collector-emitter terminals may offer some protection against second breakdown. This arrangement is analogous to decreasing BV_{CEO} , it also offers the advantage of diverting some collector current (which may be substantial, depending on the value of the resistor), from the transistor to the diode. The addition of the zener diode will degrade device performance, in that it reduces the maximum attainable V_{CE} and increases turn-off time (di/dt is constrained by the inductor voltage which is related to V_{CE}). However, because both V_{CE} and $I_C(t)$ are decreased

during turn-off, the energy dissipated by the transistor in a given Δt is reduced. If this energy per Δt is sufficiently small, it may be possible for the transistor to turn-off safely.

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APPENDIX A
SPICE PARAMETERS AND MANUFACTURER'S DATA
SHEET FOR THE 2N6551 TRANSISTOR

Q2N6551

66

TYPE NPN

IS = 5.56D-14

BF = 116.000

NF = 1.000

VAF = 3.09D+02

IKF = 7.68D-01

ISE = 7.81D-13

NE = 1.697

BR = 8.440

NR = 1.000

IKR = 5.57D-01

ISC = 3.88D-12

NC = 1.387

RB = 1.366

RE = 0.180

RC = 0.660

CJE = 1.14D-10

VJE = 0.900

MJE = 0.500

TF = 1.00D-08

CJC = 1.42D-10

VJC = 0.850

MJC = 0.333

NPN SILICON ANNULAR
AMPLIFIER TRANSISTORS

designed for general-purpose, medium-voltage, medium power amplifier and driver applications; series, shunt and switching regulators, and low and high frequency inverters and converters

- High Collector-Emitter Breakdown Voltage –
BVCEO = 100 Vdc (Min) @ IC = 1.0 mAdc – 2N6553
- Duowatt Package – 2 Watts Free Air Dissipation @ TA = 25°C
- Complements to PNP 2N6554/5/6

DUOWATT
NPN SILICON
AMPLIFIER TRANSISTORS

MAXIMUM RATINGS

Rating	Symbol	2N6551	2N6552	2N6553	Unit
*Collector-Emitter Voltage	V _{CEO}	60	80	100	V _{dc}
*Collector-Base Voltage	V _{CBO}	60	80	100	V _{dc}
*Emitter-Base Voltage	V _{EB0}	5.0			V _{dc}
*Collector Current – Continuous	I _C	1.0			A _{dc}
– Peak (1)		2.0			
*Base Current	I _B	100			mA _{dc}
*Total Power Dissipation @ T _A = 25°C	P _D	2.0			Watts
Derate above 25°C		16			mW/°C
Total Power Dissipation @ T _C = 25°C	P _D	10			Watts
Derate above 25°C		80			mW/°C
*Operating and Storage Junction Temperature Range	T _J , T _{stg}	-55 to +150			°C
*Solder Temperature, 1/16" from Case for 10 Seconds	–	260			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Ambient	RθJA	62.5	°C/W
Thermal Resistance, Junction to Case	RθJC	12.5	°C/W

*Indicates JEDEC Registered Data.
(1) <10 ms, < 50% Duty Cycle

STYLE 1
PIN 1 EMITTER
2 BASE
3. COLLECTOR
4. COLLECTOR

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	21.84	22.35	0.860	0.880
B	9.91	10.41	0.390	0.410
C	4.39	4.65	0.173	0.183
D	0.58	0.74	0.023	0.029
F	3.56	4.06	0.140	0.160
G	2.41	2.67	0.095	0.105
H	1.70	1.96	0.067	0.077
J	0.48	0.66	0.019	0.026
K	12.19	12.95	0.480	0.510
L	1.65	2.03	0.065	0.080
N	9.91	10.16	0.390	0.400
Q	3.56	3.81	0.140	0.150
R	1.07	1.75	0.042	0.069
T	7.87	9.14	0.310	0.360

CASE 306-04
TO-202AC

*ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage ($I_C = 1.0\text{ mAdc}$, $I_B = 0$)	BV_{CEO}	60	—	Vdc
2N6551		80	—	
2N6552		100	—	
Collector-Base Breakdown Voltage ($I_C = 100\text{ }\mu\text{Adc}$, $I_E = 0$)	BV_{CBO}	60	—	Vdc
2N6551		80	—	
2N6552		100	—	
Emitter-Base Breakdown Voltage ($I_E = 100\text{ }\mu\text{Adc}$, $I_C = 0$)	BV_{EBO}	5.0	—	Vdc
Collector Cutoff Current ($V_{CB} = 40\text{ Vdc}$, $I_E = 0$)	I_{CBO}	—	100	nAdc
($V_{CB} = 60\text{ Vdc}$, $I_E = 0$)		—	100	
($V_{CB} = 80\text{ Vdc}$, $I_E = 0$)		—	100	
Emitter Cutoff Current ($V_{EB} = 4.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	—	100	nAdc
ON CHARACTERISTICS (1)				
DC Current Gain ($I_C = 10\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$)	h_{FE}	60	—	—
($I_C = 50\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$)		80	300	
($I_C = 250\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$)		60	—	
($I_C = 500\text{ mAdc}$, $V_{CE} = 1.0\text{ Vdc}$)		25	—	
Collector-Emitter Saturation Voltage ($I_C = 250\text{ mAdc}$, $I_B = 10\text{ mAdc}$)	$V_{CE(sat)}$	—	0.5	Vdc
($I_C = 1.0\text{ Adc}$, $I_B = 100\text{ mAdc}$)		—	1.0	
Base-Emitter On Voltage ($I_C = 250\text{ mAdc}$, $V_{CE} = 5.0\text{ Vdc}$)	$V_{BE(on)}$	—	1.2	Vdc
DYNAMIC CHARACTERISTICS				
Current-Gain – Bandwidth Product ($I_C = 100\text{ mAdc}$, $V_{CE} = 5.0\text{ Vdc}$, $f = 20\text{ MHz}$)	f_T	75	375	MHz
Collector-Base Capacitance ($V_{CB} = 20\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$)	C_{cb}	—	18	pF

* Indicates JEDEC Registered Data

(1) Pulse Test: Pulse Width $< 300\text{ }\mu\text{s}$, Duty Cycle $< 2.0\%$

TYPICAL CHARACTERISTICS

FIGURE 1 – CURRENT-GAIN – BANDWIDTH PRODUCT

FIGURE 2 – CAPACITANCES

TYPICAL CHARACTERISTICS (continued)

FIGURE 3 – DC CURRENT GAIN

FIGURE 4 – "ON" VOLTAGE

FIGURE 5 – COLLECTOR SATURATION REGION

FIGURE 6 – TEMPERATURE COEFFICIENTS

FIGURE 7 – COLLECTOR CHARACTERISTICS

FIGURE 8 – COLLECTOR CUTOFF REGION

TYPICAL CHARACTERISTICS (continued)

FIGURE 9 - THERMAL RESPONSE

FIGURE 10 - ACTIVE-REGION SAFE-OPERATING AREA

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate I_C - V_{CE} limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 10 is based on $T_C = 25^{\circ}\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^{\circ}\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 10 may be found at any case temperature by using the appropriate curve on Figure 11.

$T_{J(pk)}$ may be calculated from the data in Figure 9. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

FIGURE 11 - POWER DERATING

APPENDIX B
SPICE LISTING OF THE SECOND BREAKDOWN
SUBCIRCUIT

```
*****
* SECOND BREAKDOWN MODEL (SUBCIRCUIT)
.SUBCKT SECBRK 3 2 1 10
*****
```

```
* NAND GATE
```

```
RQ1 125 113 10K
RQ2 125 111 1K
RQ3 114 10 10K
CQ1 111 114 1NF
DQ1 113 82 DTRIG
DQ2 113 92 DTRIG
DQ3 113 83 DTRIG
DQ4 113 93 DTRIG
DQ5 113 110 DTRIG
Q2 111 110 10 QMON
```

```
*****
* MONOSTABLE
```

```
RM1 125 124 1K
RM2 125 121 60K
RM3 125 122 1K
RM4 122 123 60K
RM5 124 127 495K
RM6 127 10 5K
CM1 124 121 1MF
VMD 125 10 DC 100.4
Q3 124 123 10 QMON
Q4 122 121 10 QMON
DM1 121 114 DTRIG
```

```
*****
* AVALANCHE CIRCUITRY
```

```
D1 2 21 DTRIG
RCE 21 22 VALUE 1
VCEO 22 10 VALUE 2
D2 10 24 DTRIG
REB 24 23 VALUE 3
VEBO 23 1 VALUE 4
```

```
*****
* VCE CONTROL
```

```
VCON 130 10 VALUE 5
RCON 130 10 1
VCON2 133 10 VALUE 6
RCON2 133 10 1
ECON 82 10 POLY(2) 2 10 130 10 0 1 -1
ECON2 83 10 POLY(2) 2 10 133 10 0 -1 1
```

* IC CONTROL

VICON 131 10 VALUE 7

RICON 131 10 1

VICON2 134 10 VALUE 8

RICON2 134 10 1

VQ1 3 2 DC 0

HIC 136 10 VQ1 1

RIC 136 10 1

EICON 92 10 POLY(2) 136 10 131 10 0 1000 -1

EICON2 93 10 POLY(2) 136 10 134 10 0 -1000 1

* SECOND BREAKDOWN MODEL ELEMENTS

ESEC 132 10 POLY(2) 2 10 127 10 0 0 0 0 1

DSEC 2 132 DTRIG

.MODEL DTRIG D VJ=0.6 RS=0.5

.MODEL QMON NPN VJE=0.6 RB=10 CJE=0.1PF

.ENDS 2NDBR

.END

APPENDIX C
COMPLETE LISTING OF SPICE CODE USED TO MODEL
THE INDUCTIVE TEST AND EVALUATION CIRCUIT

.WIDTH IN=72 OUT=72

* INDUCTIVE SWITCHING CIRCUIT

RC 5 4 8

RS 6 1 4500

L1 4 3 1MH

VCC 5 0 DC 15

VEB 7 0 PWL(0 44 4995NS 44 5005NS -8.1 1MS -8.1)

VQ2 3 9 DC 0

VBL 7 6 DC 0

Q1 2 1 0 Q2N6551

X2NDBRK 9 2 1 0 SECBRK

.MODEL Q2N6551 NPN IS=55.6E-15 BF=116 NF=1.0 ISC=3.876E-12

+ISE=781E-15 NE=1.697 BR=8.44 NR=1.0 IKR=0.557 VAF=309

+RE=0.18 RC=0.66 CJE=114P MJE=0.5 VJE=0.9 CJC=142P

+VJC=0.85 TF=10N RB=1.366 IKF=0.768 MJC=0.333 NC=1.387

.OPTIONS LIMPTS=10000 ITL5=0 METHOD=GEAR

.TRAN 24NS 16000NS 4000NS

.PRINT TRAN V(2) I(VQ2)

* SECOND BREAKDOWN MODEL (SUBCIRCUIT)

.SUBCKT SECBRK 3 2 1 10

* NAND GATE

RQ1 125 113 10K

RQ2 125 111 1K

RQ3 114 10 10K

CQ1 111 114 1NF

DQ1 113 82 DTRIG

DQ2 113 92 DTRIG

DQ3 113 83 DTRIG

DQ4 113 93 DTRIG

DQ5 113 110 DTRIG

Q2 111 110 10 QMON

* MONOSTABLE

RM1 125 124 1K

RM2 125 121 60K

RM3 125 122 1K

RM4 122 123 60K

RM5 124 127 495K

RM6 127 10 5K

CM1 124 121 1MF

VMD 125 10 DC 100.4

Q3 124 123 10 QMON

Q4 122 121 10 QMON
DM1 121 114 DTRIG

* AVALANCHE CIRCUITRY

D1 2 21 DTRIG
RCE 21 22 32
VCEO 22 10 DC 116
D2 10 24 DTRIG
REB 24 23 1.0
VEBO 23 1 DC 9.3

* VCE CONTROL

VCON 130 10 DC 128
RCON 130 10 1
VCON2 133 10 DC 136
RCON2 133 10 1
ECON 82 10 POLY(2) 2 10 130 10 0 1 -1
ECON2 83 10 POLY(2) 2 10 133 10 0 -1 1

* IC CONTROL

VICON 131 10 DC 455
RICON 131 10 1
VICON2 134 10 DC 485
RICON2 134 10 1
VQ1 3 2 DC 0
HIC 136 10 VQ1 1
RIC 136 10 1
EICON 92 10 POLY(2) 136 10 131 10 0 1000 -1
EICON2 93 10 POLY(2) 136 10 134 10 0 -1000 1

* SECOND BREAKDOWN MODEL ELEMENTS

ESEC 132 10 POLY(2) 2 10 127 10 0 0 0 0 1
DSEC 2 132 DTRIG

.MODEL DTRIG D VJ=0.6 RS=0.5
.MODEL QMON NPN VJE=0.6 RB=10 CJE=0.1PF
.ENDS 2NDBR
.END