PIPELINED SIGMA-DELTA MODULATORS
WITH INTERSTAGE SCALING

by

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ABSTRACT

Sigma-Delta analog-to-digital converters ($\Sigma\Delta$ ADC) are capable of achieving high resolution (> 15 bits) for moderate signal frequencies ($< 100\text{kHz}$). Pipelined converters are capable of handling high signal frequencies (MHz) at lower resolution. In this report, a new family of $\Sigma\Delta$ converters that utilize the noise shaping properties of $\Sigma\Delta$ converters in conjunction with pipelined architecture and interstage scaling is proposed. N bit quantizers, external to the $\Sigma\Delta$ loop, provide a quantization error that is $1/2^N$ that of a single-bit quantizer. Pipelining M such stages with interstage scaling reduce the quantization error upto a factor of $1/2^{NM}$. Single-bit feedback $\Sigma\Delta$ modulators of any order L can be used to provide L^{th} -order noise shaping with the factor $(1-z^{-1})^L$. The single-bit quantization error can thus be multiplied by a factor of $(1-z^{-1})^L/2^{NM}$. This indicates that performance superior than either architecture is achieved by the proposed converter. Further, this concept of pipelining with interstage scaling can be extended to any unit $\Sigma\Delta$ modulator employing multibit internal quantizer. The implementation of a two-stage pipeline utilizing single-bit, first-order sigma-delta modulator and four-bit quantizers in silicon is described. Measurement results confirm the practicability of the proposed system.

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CHAPTER 1

INTRODUCTION

Of the many different types of analog-to-digital converters, those using the principle of Sigma-Delta modulation have become quite popular for digital audio applications. Unlike other schemes, sigma-delta analog-to-digital converters ($\Sigma\Delta$ ADCs) employ analog circuits having precision much less than the resolution of the overall converter and yet achieve high resolution. This has been made possible by the recent advances in VLSI technology, which enables the incorporation of the required digital signal processing on the same chip [1,2,3]. The low cost, due to low precision circuits, has enabled the use of these converters in consumer applications like audio, multimedia and personal communication systems.

The requirements of current state-of-art technology include information transmission at high bit rates, in the megahertz (MHz) range. The analog-to-digital converters utilized to convert the analog information to digital signals must be capable of converting high frequency signals, for example, video signals. Currently, the fastest conversion is achieved by the flash converters, that compare the signal with 2^N thresholds for a output N bit word. This requires 2^N comparators, which implies that the circuit gets prohibitively large for high-resolution converters. Typically, flash converters have resolutions below 10 bits, and can operate in the GHz range. Higher resolution can be obtained by pipelining the flash converters. The residual error from one stage is made full-scale (called interstage scaling) and is converted by the next stage to add resolution. However, in general, this results in a converter that is slower than the flash converter, depending on the number of stages used. The number of comparators required is significantly less than the full flash converter, for a given resolution. While any type of analog-to-digital converter may be pipelined, pipelined flash converters are loosely called pipelined converters. These can operate at resolution upto 15 bits in the MHz range. When resolution greater than 15 bits is required, successive-approximation or sigma-delta converters need to be utilized. However, the signal frequencies that can be converted at

high resolution is limited to less than 100 kHz.

Sigma-delta converters are capable of achieving high resolution by employing the concepts of oversampling and noise-shaping. When a signal is quantized, the quantization error is uniformly distributed in the frequency band that extends to half the sampling frequency. Hence, oversampling, i.e., sampling above the Nyquist rate leaves only a portion of the quantization noise in the baseband. Further, the transfer function for the quantization error in a sigma-delta modulator attenuates low frequencies and emphasizes high frequencies. This further reduces the quantization noise in the baseband. Thus, the resolution can be improved considerably by increasing the oversampling ratio or by increasing the transfer function order. Since for a given technology, the maximum operational speed is fixed, (for example, 50 MHz for switched capacitor CMOS circuits) the oversampling ratio determines the maximum signal frequency that can be converted for a specified resolution. For state-of-art applications with high signal bandwidth, low oversampling ratios are then required, while maintaining high resolution. In this report, a solution is presented by proposing a technique to integrate the key concept in pipelined converters – interstage scaling – with sigma-delta modulators. While the simplest system possible using this technique is presented as a proof-of-concept system, this technique, in general, can be incorporated in sigma-delta systems that utilize multibit internal quantizers.

The following chapter presents a brief discussion on sigma-delta modulators and pipelined converters. The proposed system, implementation in CMOS integrated circuitry, simulation and measurement results are presented in the subsequent chapters.

CHAPTER 2

SIGMA-DELTA AND PIPELINED ANALOG-TO-DIGITAL CONVERTERS

2.1 Sigma-Delta Analog-to-Digital Converters

2.1.1 First-order $\Sigma\Delta$ Modulators

Sigma-delta analog-to-digital converters incorporate a simple analog anti-aliasing filter, the $\Sigma\Delta$ modulator and digital signal processing to convert analog signals to digital signals as shown in Figure 2.1. The analog anti-aliasing filter can have a gradual roll-off as oversampling is used to reduce the quantization noise in the baseband. The $\Sigma\Delta$ converter further shapes the quantization noise out of the baseband, enabling high resolution. The bit stream from the modulator is then passed through low-pass filter to filter noise outside the baseband and a down-sampler to bring the output to Nyquist rate, which are implemented as digital decimators [1].

A linear analysis of a single-loop single-bit $\Sigma\Delta$ modulator shown in Figure 2.1 relates the input x to the output y of the modulator as

$$Y(z) = X(z) z^{-1} + (1 - z^{-1}) e(z) \quad (2.1)$$

where $e(z)$ is the quantization error introduced by the single-bit quantizer (comparator). The first term in the output is a delayed version of the input. The second term is the quantization error which is first-order noise shaped by the factor $(1 - z^{-1})$.

Figure 2.1. Sigma-Delta Analog-to-Digital Converter

Figure 2.2. Magnitude of NSFs of Orders $L = 1, 2$ and 3 as a Function of Frequency Normalized to the Sampling Frequency.

The factor $(1-z^{-1})$ is called the first-order “noise shaping function” (NSF) and it corresponds to the graph with $L = 1$ in Figure 2.2. The effect of oversampling is also illustrated in Figure 2.2, where the magnitude of NSFs are shown as a function of frequency normalized to the sampling frequency, F_s . If the signal bandwidth is $0.1 F_s$, the Nyquist sampling rate is $0.2 F_s$, and the quantization error power is assumed to be uniformly spread in the region 0 to half the sampling frequency ($0.1 F_s$) with a magnitude 5 (assuming total noise power is unity). If the signal is now sampled at F_s , i.e., with a oversampling ratio of 5 , that same noise power is spread from 0 to $0.5 F_s$, with a magnitude of 1 , leaving the noise power in the baseband reduced by a factor equal to the oversampling ratio. This noise is further multiplied by the noise shaping function $(1-z^{-1})^L$, where L is the order of the noise shaping function. The effect of the noise shaping function

Figure 2.3. Second-Order Sigma-Delta Modulator: the Candy Structure.

is to reduce the noise power in the baseband while emphasizing it outside the baseband. The digital decimator filters this out of band noise.

The step size of the comparator in Figure 2.1 is typically made equal to the maximum input signal swing as the signal to noise ratio (SNR) at the output decreases as the signal strength decreases, for a given step size. For reference, a step size and a signal swing of unity is assumed for the single-bit first-order modulator discussed above.

2.1.2 Higher-order $\Sigma\Delta$ Modulators

Performance improvement can be obtained by increasing the number of loops and/or by the inclusion of multibit feedback. Increasing the number of loops increases the order L to which the noise shaping function (NSF) is raised. Higher-order noise shaping functions can be attained by cascading [4] or by MASH [5] structures, as shown in Figure

Figure 2.4. Second-Order Sigma-Delta Modulator: the MASH Structure

2.3 and Figure 2.4, respectively. Both systems implement the second-order noise shaping function, $(1-z^{-1})^2$ which corresponds to the graph with $L = 2$ in Figure 2.2. It can be inferred that more of the quantization noise is shifted out of the baseband. While either topology can be extended to increase the order of the NSF, achieving NSF orders above 3 is difficult as cascaded loops suffer from stability constraints while traditional pipelined or MASH structures suffer from the effects of non-ideal implementation.

2.1.3 Multibit modulators

Instead of the single-bit comparator, a multibit analog-to-digital converter can be used to quantize the integrator output, reducing the quantization error, as shown in Figure 2.5. However, this approach requires a multibit digital-to-analog converter (DAC) in the feedback loop, increasing the cost of the system as linearity of the DAC should equal the overall converter resolution. High-resolution $\Sigma\Delta$ analog-to-digital converter have been generally implemented as a combination of the above three schemes.

A different but less popular approach to improving resolution uses multibit quantization for the integrator output but only single-bit feedback [6] as shown in Figure 2.6. The output of the single-bit modulator, y_1 , and that of the N bit ADC y_2 are given as

$$Y_1(z) = X(z) z^{-1} + (1 - z^{-1}) e_1(z) \quad (2.2)$$

Figure 2.5. Multibit Sigma-Delta Modulator.

$$Y_2(z) = (X(z) - Y_1(z)) \frac{z^{-1}}{1 - z^{-1}} + e_2(z) \quad (2.3)$$

where e_1 and e_2 are the quantization errors introduced by the single-bit comparator and multibit quantizers, respectively. As analog differentiators cause more errors, y_2 is differentiated digitally and added to the delayed single-bit output y_1 to get the output y as

$$Y(z) = X(z) z^{-1} + (1 - z^{-1}) e_2(z). \quad (2.4)$$

With the reference input signal swing of unity assumed, the maximum signal swing at the output of the integrator is 2 for sinusoidal input a few decibels below peak [7]. Since both quantizers see the same input and the quantization error of the multibit quantizer is $1/2^N$ that of the single-bit quantizer, the error in output y is reduced by a factor $1/2^N$, leading to a high-resolution converter. It should be noted that this approach reduces the total magnitude of the quantization error in the output in contrast to noise shaping, where the quantization error in the baseband is reduced and the noise power outside the baseband is increased, necessitating high-order digital filters for higher-order converters.

Further improvement can be obtained using the topology shown in Figure 2.7

Figure 2.6. Sigma-Delta Modulator with Multibit Quantizer External to the Feedback Loop.

Figure 2.7. Improved Sigma-Delta Modulator with Multibit Quantizer External to the Feedback Loop

[8,9]. While the output y remains the same as in (2.4), the multibit quantizer is now used to quantize the error e_1 introduced by the single-bit quantizer. The input range to the multibit quantizer is reduced to 1 as the magnitude of e_1 varies from $-1/2$ to $1/2$. In general, the input range to the multibit quantizer is reduced by the step size of the single-bit quantizer. The error e_2 introduced by the multibit quantizer is now half of $1/2^N$ if the number of bits in the multibit quantizer is kept the same as in the previous architecture. If the error is to be kept the same, a multibit quantizer with one less bit can be utilized. Thus, the total magnitude of the quantization error is still reduced, and high-resolution converters at modest oversampling ratios can be implemented using this approach.

In the pipelined or MASH structure discussed above, the output of the previous stage integrator, or the error out of a single-bit quantizer is at least full-scale, precluding the use of the concept of interstage scaling. In a $\Sigma\Delta$ modulator using multibit quantizers, however, the quantization error is less than full-scale and interstage scaling may be employed. Such a structure that uses multibit DACs in the sigma-delta feedback loop has been presented [10]. Since the use of precision DACs add to the cost of the system, the multibit structures that use single-bit feedback can incorporate the concept of interstage scaling. This forms the proposal presented in the following chapter.

2.1.4 Implementation Nonidealities in Sigma-Delta Converters.

The potentially high resolution obtained by sigma-delta modulators can be limited by nonidealities that occur in the implementation. Depending on the target of the particular

system being built, many of these nonidealities can be reduced to acceptable levels by careful design. Each modulator topology has its own specifications for the building blocks that comprise the modulator, like the integrator, comparator and coarse multibit analog-to-digital and digital-to-analog converters.

As ideal building blocks cannot be obtained, many tradeoffs exist between the system performance and building block specifications. Thus building block specifications need to be obtained for each particular design. The precision required for the coarse digital-to-analog converters in the feedback loop is that of the resolution of the entire modulator. Any errors in the DAC directly add to the signal. This places a tough design constraint on the DAC, and is a disadvantage for such converters. Converters with multiple loops and integrators as in the Candy structure require a large output swing of the integrator opamps in comparison to the input signal, and effectively reduce the dynamic range of signals that can be handled for a given supply voltage. The thermal noise associated with the sampling capacitors can be the limiting factor, but by the suitable choice of capacitor value, it can be reduced to a level lesser than the anticipated signal-to-noise ratio. Similarly, the switches can be sized to keep the capacitors charging time constants well below the clock speed to prevent errors due to incomplete settling. Clock jitter could be of concern in high-resolution modulators. Implementation nonidealities, like integrator leakage, can limit the performance of the proposed system and are discussed in Chapter 5.

2.2 Pipelined Analog-to-Digital Converters

2.2.1 Introduction

Analog-to-digital converters of a given resolution can be pipelined to achieve a converter with much higher resolution. The analog input is converted to a low-resolution digital signal initially by a low-resolution converter. A digital-to-analog converter converts this digital output to an analog value. The difference of this reconstructed analog value and the input constitutes the unconverted residue, or the quantization error, associated with the first low-resolution converter. This residue is amplified to full-scale

and fed to the second stage comprising of a low-resolution ADC and DAC, as shown in Figure 2.8. For each output code of the first stage, depending on the magnitude of the scaled residue, the second stage will output one of the codes that it is capable of, providing higher resolution. These stages can be cascaded to achieve the required resolution.

Each stage of the pipelined converter can operate faster than a single converter with the same overall resolution as the pipelined converter. This is because the individual stages convert only less number of bits that require signal settling to a lesser extent. Thus the pipelined converter can handle larger bandwidths. While the first stage is converting the present sample, the second stage converts the previous sample and so on. The output code for any given sample is available only after every stage has finished its conversion. Thus, latency is introduced in the overall conversion. This concept offers a trade off between circuit complexity, chip area, circuit operating speed, power consumption, resolution and other parameters that determine the analog-to-digital converter design.

In high frequency applications, usually flash converters are pipelined. Flash converters employ one comparator for every quantization level, resulting in the fastest conversion time. However a fully flash N bit converter requires $2^N - 1$ comparators which is 1023 for a 10 bit converter, and increase in resolution involves doubling the number of

Figure 2.8. M stage Pipelined Converter (top) and Stage K (bottom).

comparators for every bit. This results in prohibitively large power inefficient system. Pipelining flash converters reduces the number of comparators to $M \cdot (2^{N/M} - 1)$. Typically two to three bit flash converters are utilized per stage [11].

Pipelined converters can also be implemented with one-bit resolution per stage. This implies that a comparator would suffice for the ADC. The DAC consists of a switch that selects the reference voltages corresponding to the high and low outputs of the ADC. Every stage of a single-bit per stage pipelined converter with full-scale range between $-V_{\text{ref}}$ and $+V_{\text{ref}}$ can be ideally modeled by the following equations:

$$\begin{aligned} \text{if } V_{\text{in}} > 0, \quad V_{\text{D}} &= \text{HI} \quad V_{\text{res}} = 2V_{\text{in}} - V_{\text{ref}}; \\ \text{if } V_{\text{in}} < 0, \quad V_{\text{D}} &= \text{LOW} \quad V_{\text{res}} = 2V_{\text{in}} + V_{\text{ref}}; \end{aligned} \quad (2.5)$$

where V_{in} is the input voltage, V_{D} is the digital output voltage, and V_{res} is the residue transferred to the next stage. Strictly, the HI and LOW digital outputs correspond to the ADC output levels $\pm V_{\text{ref}} / 2$, respectively, resulting in a step-size of V_{ref} . Even though theoretically this implies N stages for N bit resolution, this is not the case practically for converters with resolution greater than 7 bits, as discussed next.

2.2.2 Implementation Nonidealities in Pipelined Converters

Error sources that can limit the achievable resolution in pipelined analog-to-digital converters include offset and gain errors associated with the amplifiers and nonlinearity of the ADC and the DAC in each stage [12]. Obtaining good performance with pipelined converters usually involves the use of redundant bits, digital error correction, trimming, calibration and other techniques that are particularly targeted towards the reduction of the effects of implementation nonidealities [13,14]. For high-resolution converters with more number of bits per stage, the error introduced by a nonideal DAC also contributes to the limitation. This is however not a limitation for the one-bit case where only a single reference voltage is required to implement a DAC.

An other source of error in pipelined converters is the comparator offset. Comparators with offsets in the order of tens of millivolts can be implemented. Resolution of the comparators can be increased by preamplifying the signal before

comparison. Offsets cause a particular digital code to be produced for a range of input analog voltages different from nominal. This also results in a residue larger than the full-scale input of the next stage, causing an overload, if the maximum allowable scaling is used. Gain errors can be caused by capacitor mismatches or by low opamp gain. An imperfect multiplication factor either overloads the next stage or produces a residue less than the expected value. Many techniques have been proposed to mitigate these problems to extend the resolution of the simple pipelined converters beyond eight bits.

The above discussions illustrated the basic concept of sigma-delta and pipelined analog-to-digital conversion and the limitations and error sources. The approach for ADC system design is to create a very robust and cost effective system that provides high performance while using components of only moderate precision. This is especially true for the integration of analog circuits in imprecise digital technologies, without the use of extensive calibration, trimming or component matching. The sigma-delta modulator is a robust system that trades resolution in time for resolution in voltage value, using the concept of noise shaping. In the following proposal, the advantages of pipelined conversion using interstage scaling is incorporated with the noise-shaping properties of sigma-delta modulators to achieve this goal.

CHAPTER 3

PIPELINED SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTERS WITH INTERSTAGE SCALING

3.1 Proposal

Implementation of pipelined $\Sigma\Delta$ analog-to-digital converter with interstage scaling is achieved by feeding the error in the multibit quantizer (Figure 2.7), after scaling, into the next $\Sigma\Delta$ loop in the pipeline as shown in Figure 3.1. In the simplest realization shown in Figure 3.1, one first-order $\Sigma\Delta$ loop and a multibit quantizer form a unit of the pipeline. The residue in the first unit is scaled and fed into the second unit, as in standard pipelined analog-to-digital converter architectures. The $\Sigma\Delta$ modulators provide noise shaping characteristics at each section of residue quantization.

The quantization error out of the first stage multibit quantizer of N_1 bits is the output of the first stage. As discussed previously, this is a signal with peak magnitude $1/(2 \cdot 2^{N_1})$ and peak-to-peak magnitude $1/2^{N_1}$. A scaling factor K of 2^{N_1} between stages returns the signal to the reference value of unity at the input to the next stage. This allows for the use of a $\Sigma\Delta$ modulator identical to the first stage.

A linearized system schematic is shown in Figure 3.1 b. The quantizers are shown as additive elements with the number of bits of the respective quantizer. The digitally compatible outputs y_1 to y_4 from the analog section are obtained as

$$Y_1(z) = X(z) z^{-1} + (1 - z^{-1}) e_1(z) \quad (3.1)$$

$$Y_2(z) = e_1(z) + e_2(z) \quad (3.2)$$

$$Y_3(z) = K e_2(z) z^{-1} + (1 - z^{-1}) e_3(z) \quad (3.3)$$

$$Y_4(z) = e_3(z) + e_4(z) \quad (3.4)$$

and the intermediate digital outputs y'_1 and y'_2 are obtained as

$$Y_1'(z) = Y_1(z) - Y_2(z)(1 - z^{-1}) = X(z) z^{-1} - (1 - z^{-1}) e_2(z) \quad (3.5)$$

$$Y_2'(z) = Y_3(z) - Y_4(z)(1 - z^{-1}) = K e_2(z) z^{-1} - (1 - z^{-1}) e_4(z) \quad (3.6)$$

The output from the second stage is now scaled digitally by a factor $1/K$ and the final output y is obtained as

$$Y(z) = Y_1'(z)z^{-1} + Y_2'(z)\frac{(1 - z^{-1})}{K} = X(z) z^{-2} - \frac{(1 - z^{-1})^2}{K} e_4(z) \quad (3.7)$$

The error e_4 that is present in the final output is the quantization error of the second-stage multibit quantizer with N_2 bits.

To compare the system with a standard second-order $\Sigma\Delta$ modulator, assumption is made that the $\Sigma\Delta$ modulators in the two stages of the pipeline are identical. The error e_4 is $1/2^{N_2}$ times the error in a single-bit quantizer. With K taken as $1/2^{N_1}$, the total quantization error introduced by the proposed system is less by a factor of $2^{N_1}2^{N_2}$ in comparison to the conventional second-order $\Sigma\Delta$ ADC. The first factor arises due to the first-stage multibit quantizer and interstage scaling and the second factor is due to the second multibit quantizer.

Higher-order pipelined $\Sigma\Delta$ modulators with interstage scaling can be implemented by using higher-order modulators in each stage or by extending the pipeline shown in Figure 3.1. In either case, the order to which the final error is noise shaped will correspond to the total of the orders of the $\Sigma\Delta$ modulators in each stage. If M stages are used, this noise shaped error is further reduced by a factor $2^{N_1}2^{N_2}\dots 2^{N_M}$, where N_i is the number of bits in the i^{th} -stage multibit quantizer. The following section examines the results for the second-order system discussed above.

3.2 Theoretical Predictions

Pipelined $\Sigma\Delta$ modulators with interstage scaling reduce the quantization error in $\Sigma\Delta$ ADCs both by noise shaping and by introduction of multiplying factors to the error term. This section investigates performance enhancement that is possible with the proposed architecture.

The second-order two stage pipeline shown in Figure 3.1 is considered for discussion, unless otherwise stated. It is assumed that the stages are identical, i.e., the $\Sigma\Delta$

Figure 3.1. Pipelined Sigma-Delta Loops with Interstage Scaling. (a) System, (b) System Schematic for Linear Analysis.

loops as well as the N bit quantizers are identical. From (3.7) and the discussion following it, the error in the final output is $(1-z^{-1})^2 e(z) / 2^{2N}$ where $e(z)$ is the quantization error introduced by a single-bit ADC (comparator) in the $\Sigma\Delta$ loop. The effective noise shaping function (ENSF) is now defined as $(1-z^{-1})^2 / 2^{2N}$ and is plotted in Figure 3.2 as a function of normalized frequency, with the sampling frequency (F_s) taken as unity. The number of bits used in the multibit quantizers is indicated as N .

For analog-to-digital converters in which noise shaping is not used, the quantization error has a magnitude unity, as assumed above, and is spread uniformly in the frequency range in Figure 3.2, from zero to half the sampling frequency. For the case $N=1$, the ENSF reduces to the second-order NSF of the traditional cascaded or MASH architectures. It can be seen that the error in the traditional noise shaping modulator is

Figure 3.2. (a) Magnitude of ENSF as Function of Normalized Frequency, with Sampling Frequency $F_s = 1$. The Number of Bits in the Multibit Quantizer is Indicated as N ;
(b) Magnitude in dB

reduced below unity for low frequency signals and amplified above unity for higher frequency signals. The higher frequency band where noise is amplified ($|NSF| > 1$) is filtered out using the digital low pass decimation filters. Thus the signal band that can be usefully converted is restricted to a low-frequency region, for a given sampling frequency, or stated alternatively, a minimum over sampling ratio (OSR) is required.

In contrast, the proposed topology reduces the quantization error in the entire frequency range of interest – up to half the sampling frequency. The advantage is then two-fold: (a) the OSR is reduced and (b) the requirements on digital low-pass decimation filters is reduced.

For general pipelined $\Sigma\Delta$ modulators with interstage scaling, the maximum value of the magnitude of the ENSF occurs at half the sampling frequency and has the value $2^L/2^{MN}$ where L is the order of the NSF and M identical stages are used. This maximum value is less than unity if $N > L/M$. This situation opens up a new possibility that, for a given signal input bandwidth, such converters can sample close to Nyquist rate, if :

- a. the area under the ENSF curves in Figure 3.2 (a) (indicative of the total noise power in the frequency range of integration) between 0 and $1/2F_s$, is less than the area under the $N=1$ curve in the range 0 to F_b / F_s (which implies an OSR of $F_s / 2F_b$, where F_b is the signal bandwidth) and
- b. the linearity required for the internal quantizer is less than the overall converter linearity.

Figure 3.3. The Oversampling Ratio Required to Obtain a 15 bit (90 dB) Converter with 2, 3 and 4 First-Order Pipelined Stages and N bit Internal Quantizers.

In Figure 3.2 (b), if a particular resolution is to be obtained from the ADC, the abscissa X of the points at which the horizontal through that resolution cuts the curves is indicative of the maximum allowed baseband frequency $F_b = XF_s$, or the minimum allowed $OSR = F_s/(2F_b) = 1/(2X)$. It can be inferred that for a given resolution, implying same noise power and same area under the ENSF curve, the OSR required is considerably reduced for any of the curves with $N > 2$. As an example, the OSR required to implement a 15 bit converter using first-order pipelined stages is shown in Figure 3.3. The figure indicates a pipeline of 2 to 4 first-order stages, implying $L = M = 2$ to 4 and the number of bits of the internal quantizer N varying from 1 to 6. Two orders of magnitude reduction in OSR is possible using the proposed pipelining technique, which enables the use of $\Sigma\Delta$ converters in high-frequency applications, with the limitation of operation being set by the switched capacitor circuits commonly used for the implementation of these ADCs.

Figure 3.4. Power Spectral Density (PSD) at the Output of a Second-Order MASH Sigma-Delta Modulator (top). PSD in the Baseband is shown at the bottom.

In the design of digital low-pass filters, the attenuation that must be provided should be at least equal to the maximum noise signal. This value is 2^L for the L^{th} order modulator in traditional architectures and is reduced to $2^L/2^{MN}$ in the proposed architecture, an improvement of $6MN$ dB. For example, if $N = 2$ and $M = 5$, the low-pass filter needs to provide 48 dB lesser attenuation than the corresponding traditional modulator. Thus, the order of the digital low-pass decimation filter is reduced, with possible reduction in power.

3.3 Simulation results

To verify the concepts developed above, results of the simulations done in MATLAB and SIMULINK are presented in this section. For comparison, the systems are tested for use in the audio band, i.e., a baseband of 20 kHz, with cut off at 24 kHz. The input to the systems is sinusoidal at 9 kHz. An oversampling ratio of 64 is used, with the Nyquist rate being 48 kHz. The spectrum of the output is a repetition of spectrum in the range 0 to 1.536 MHz, which is half the sampling frequency. Since adequate number of sample points in the baseband are necessary to compute the SNR, 128×1024 samples are

taken at the modulator output and 128×1024 bins are used for the Fourier transform and the power spectral density (PSD).

Dynamic simulation of second-order MASH $\Sigma\Delta$ system results in the output in Figure 3.4. Simulation results for the proposed second-order pipelined system with 4-bit internal quantizers and interstage scaling is shown in Figure 3.5. To compare the baseline noise in the systems, the sine input is sampled at the same sampling rate and the PSD of the sampled sine wave is shown in Figure 3.6. All the figures shows the PSD in the range 0 to $F_s/2$ (1.536 MHz) on top and in the baseband at the bottom. The signal peak at 9 kHz is visible in all the plots. Figure 3.6 shows the baseline noise when the signal is not quantized. It is clear that $\Sigma\Delta$ modulation and quantization introduces noise. In Figure 3.4, the noise power is suppressed in the baseband and is amplified (values greater than 0 dB) for frequencies above the baseband for traditional $\Sigma\Delta$ modulators. The peak signal to peak noise ratio is found to be 83 dB, close to about 14 bit resolution. Figure 3.4 shows that the noise in the baseband is close to the baseline noise in Figure 3.6, indicating that the maximum possible SNR of 137 dB (close to 23 bit resolution) is ideally achieved by the

Figure 3.5. Power Spectral Density (PSD) at the Output of a Second-Order Pipelined System with 4 bit Internal Quantizers and Interstage Scaling (top).

PSD in the Baseband is shown at the bottom.

Figure 3.6. Power Spectral Density (PSD) of a 9 kHz Sine Wave Sampled at 3.072 MHz (top). PSD in the Baseband is shown at the bottom.

proposed system. In addition, the high-frequency noise is now restrained to values below 0 dB, for the simulated system, as expected.

Each stage of the pipelined sigma-delta system may be made of higher-order systems, increasing the order of the noise shaping function L . More stages may be pipelined, increasing M . The number of bits in each stage N_i is also variable. All three factors are in the exponents and reduce the SNR considerably. For a given resolution and oversampling ratio, an additional degree of freedom is available for the designer and various trade-offs are made possible by the proposed system.

CHAPTER 4

SYSTEM IMPLEMENTATION

4.1 Overview

Analog-to-digital converters are usually used in the front-end of any signal processing or receiving system. For current day systems on chip, the analog-to-digital converter shares the chip area with digital signal processing, requiring that it be implemented in a digital integrated circuit fabrication process. This implies that extra features of the fabrication process usually used in analog circuit fabrication to achieve high precision are unavailable. This is also a reason why high-resolution sigma-delta analog-to-digital converters are attractive in system on chip applications. The most common low-power digital technology being CMOS, the pipelined sigma-delta modulator (PSDM) with interstage scaling has been implemented in Orbit 2 μ CMOS process through the MOSIS fabrication services. This process is, however, a low-noise analog process with double polysilicon layer for capacitor implementation.

The overall block diagram of the pipelined sigma-delta modulator with interstage scaling is composed of an analog section and a digital section (Figure 3.1). The analog section has pipelined stages that each have a sigma-delta modulator and a low-resolution pipelined analog-to-digital converter. This section has been implemented as an integrated circuit. The output of the integrated circuit is digital and is acquired into a computer in which the digital section is implemented in software. This chapter deals with the integrated circuit realization of the analog section.

Each stage in the PSDM is composed of a single-bit, first-order sigma-delta modulator and a four-stage, single-bit per stage pipelined ADC. Switched-capacitor (SC) circuits are ideally suited to implement these sampled-data discrete-time systems. The modulator consists of a switched-capacitor integrator and a comparator. Each stage in the pipelined ADC consists of a multiply-by-two unit and a comparator. The integrator as well as the multiply-by-two unit are built around an operational amplifier (opamp). Thus the opamp, comparator, capacitors and switches form the basic analog circuit blocks

required to implement the system. The digital timing signals for the comparators and switches are generated by the control logic, implemented with flip-flops and basic digital gates.

All circuits have been simulated using PSPICE using the “level 2” model, with parameters from different runs of the Orbit 2 μ process. LEdit has been used to layout the circuits using the MOSIS Orbit 2 μ design rules and to extract the circuit. The extracted circuit is further simulated in PSPICE to confirm operation with parasitic capacitances included.

The implementation of the modulator, pipelined ADC and the control logic are discussed in the sections 4.2, 4.3 and 4.4 of this chapter. Each of the analog circuit blocks is described in the section 4.5. The last section 4.6 describes the layout issues and the features of the fabricated chips.

4.2 Sigma-Delta Modulator

The single-bit first-order sigma-delta modulator, discussed in the previous chapters, comprises of an integrator, a comparator configured as the 1 bit analog-to-digital converter and a 1 bit digital-to-analog converter. An opamp forms the core of the integrator. The design and implementation of the opamp and the comparator are discussed in the following sections. The modulator itself is implemented using fully-differential switched capacitor circuits. In the following discussion, reference made to one capacitor (say C_1) implies both capacitors with that designation.

The circuit diagram of the modulator is shown in Figure 4.1. To cancel the effect of parasitic capacitances at signal nodes, stray-insensitive switched-capacitor circuit technique [15,16] is adopted. The circuit works using a two-phase non-overlapping clock scheme. In phase ϕ_1 , the sampling capacitor C_1 charges to the input voltage. In phase ϕ_2 , the negative of this voltage is integrated on to the integrating capacitor C_2 . In the later part of ϕ_2 , the signal FB_SWH (feedback switch high) triggers the comparator. This signal is connected to the PHI_COMP of the comparator, which is the strobe signal. FB_SWH is high for half of ϕ_2 (and changes state with ϕ_2) and the output of the

comparator is valid for this duration only. This digital output can be considered to be the output of the 1-bit analog-to-digital converter. When the output is valid, it selects the feedback voltage and is the equivalent of a 1-bit digital-to-analog converter. The feedback voltage is either the sigma-delta positive reference (SD+REF) or the negative reference (SD-REF). FB_SWH also connects the feedback voltage to capacitor C_3 which charges in this duration. Since the comparator delay time is a few nanoseconds, and the duration of FB_SWH is close to one-fourth the clock period (125 nSec for 2 MHz), there is sufficient time for this operation. In phase ϕ_1 , when the input capacitor is sampling, the voltage on C_3 is integrated on to C_2 . Thus, a quantity equal to the difference between SD+REF and SD-REF values is either added or subtracted from the integrator. This difference is the step size Δ of the 1-bit analog-to-digital converter. This also defines the input full-scale range as $\pm \Delta/2$. The peak to peak output of the integrator is 2Δ and should be within the linear range of the opamp output. Thus the choice of these reference voltages is important. For this reason, it is useful to control these voltages external to the experimental chip.

This scheme is advantageous because additional circuitry is not required to generate the quantization error introduced by the 1-bit quantizer [17]. The comparator inputs receive the integrated output in the later part of ϕ_2 for analog-to-digital conversion. In the later part of ϕ_1 , the integrator outputs the difference between the integrator output in previous ϕ_2 and the corresponding digital-to-analog converter output, which is the quantization error introduced by the coarse analog-to-digital converter. At this time, the output of the integrator is sampled by the multibit analog-to-digital converter for further processing.

The layout of the modulator is shown in Figure 4.2. The important feature of this layout is the 'cell' type of layout, enabling the adjacent placement of other cells that continue the horizontal flow of signal, supply, reference and clock voltages mostly in the metal 1 layer. The outputs are available along the vertical direction in the metal 2 layer. The functionality of the extracted circuit has been verified using PSPICE. The details of the various components that comprise this modulator are discussed in Section 4.5.

4.3 Multibit Pipelined Analog-to-Digital Converter

The multibit coarse quantizer samples the quantization error from the sigma-delta modulator and generates a digital signal with resolution much less than the overall converter. The quantization error introduced by this converter is scaled and fed to the next stage in the proposed pipelined sigma-delta modulator. If implemented as a flash converter this residue generation process can be accomplished only with the use of a multibit digital-to-analog converter. This situation is still better than using multibit coarse quantizer and attendant digital-to-analog converter inside the sigma-delta loop as the

Figure 4.1. Schematic of the First-Order Single-Bit Sigma-Delta Modulator

errors introduced by the digital-to-analog converter is noise shaped, in contrast to the latter situation where these errors add directly to the input signal. However, multiple voltage references need to be generated for the ADC as well as the DAC. Also, the residue needs to be scaled, which can be implemented, at best, with an accuracy of 0.1%. Moreover, this scaling cannot be the maximum possible for the given number of bits, as it is practically observed that the residues are larger than ideal due to implementation imperfections.

An important aspect of this research has been the identification of a solution to this issue. The pipelined multibit ADC with one-bit per stage provides, just as a consequence of its architecture, the fully scaled residue without the use of a multibit DAC and neither does it require multiple voltage references. This converter can not be used inside the sigma-delta loop because pipelined conversion involves a latency related to the number of bits while the loop requires an estimate of the integrator output for subtraction from the

Figure 4.2. Layout of the First-Order Single-Bit Sigma-Delta Modulator

Figure 4.3. Schematic of One Stage of the Pipeline Multibit Quantizer that samples in ϕ_1 .

input in the next clock cycle itself. External to the loop, pipelined converters can be used as the latency involved in conversion is not a factor [9].

Each stage of the pipelined multibit quantizer consists of an opamp and a comparator. The comparator generates a digital bit depending on whether the input is greater or lesser than the threshold voltage. If lesser, output is a logic '0' and is multiplied by 2 and passed to the next stage in the pipeline. If greater, then the output is a logic '1', the threshold voltage is subtracted from the input and the residue is multiplied by 2 and passed to the next stage. The opamp is used for the multiply-by-two and add operation.

For a system with the threshold of 0 V (which implies that the input ranges from $-V_{\text{ref}}$ to $+V_{\text{ref}}$) the required transfer function becomes

$$\begin{aligned} V_{\text{in}} < 0, & \quad V_{\text{res}} = 2 V_{\text{in}} + V_{\text{ref}} \quad \text{logic '0'} \\ V_{\text{in}} > 0, & \quad V_{\text{res}} = 2 V_{\text{in}} - V_{\text{ref}} \quad \text{logic '1'}. \end{aligned} \quad (4.1)$$

This transfer function is achieved by the circuit shown in Figure 4.3 [13]. In the following discussion, reference made to one capacitor (say C_1) implies both capacitors with that designation. During ϕ_1 , equal capacitors C_1 and C_2 are connected in parallel and sample the input. The opamp is connected in a unity gain configuration that serves to auto-zero the opamp. The input also is available to the comparator, but comparison is

Figure 4.5. Layout of One Stage of the Pipelined Multibit Quantizer that Samples in ϕ_1 .

Thus the odd and even stages have their output bits valid in later half of ϕ_1 and ϕ_2 , respectively, effecting conversion of two bits in one cycle. The schematic of this second stage is shown in Figure 4.4.

All digital outputs are available in the later part of ϕ_2 , in synchronization with FB_SWH signal referred to in the section 4.1. This signal is brought out of the chip as the data-ready signal for the entire chip. This signal triggers comparison and does not incorporate the additional delay required to ensure that all digital outputs have attained their steady state values. The expected value for this delay is the comparator delay time added to the delay time associated with the pad driver and the external load capacitor. Such delay must be incorporated external to the chip while testing.

The layouts of both units of the pipeline are similar and differ only in the connections of the switches. Hence the layout of the unit that samples in ϕ_1 alone is shown in Figure 4.5. This layout also conforms to the 'cell' type of layout, enabling the adjacent placement of modulator and pipeline cells that continue the horizontal flow of

Figure 4.6. Timing Signals

signal, supply, reference and clock voltages mostly in the metal 1 layer. The outputs are available along the vertical direction in the metal 2 layer. The functionality of the circuit has been verified with PSPICE. The details of the various components that comprise the pipeline unit will be discussed in the following sections.

4.4 Timing Circuits

The switched-capacitor circuit that implements the entire system works on a two-phase non-overlapping clock. Phase ϕ_1 is high for a duration less than half the sampling clock period and ϕ_2 is high for an equal duration in the other half of the sampling clock period. There exists a definite but small time duration when both the clocks are low [16]. These clocks control the sampling, integration and multiply-by-two operations. The comparators work after signal settling occurs in the first half of each of the phases. The modulator comparator works for later half of ϕ_2 and is controlled by signal FB_SWH . For proper operation of the circuit, signals FB_SWH should go low with ϕ_2 . The odd units of the pipelined multibit converter, controlled by PI_COPH1 , compare in the later half of ϕ_1 and hold the result in ϕ_2 . The even units of pipelined multibit converter, controlled by

Figure 4.7. Two-Phase Non-overlapping Clock Generator following the divide-by-two Counter

PI_COPH2, compare in the later half of ϕ_2 and hold the result in ϕ_1 . The timing of these important signals are illustrated in Figure 4.6.

Since a measure of half the phases is required, the chip takes as input a clock signal I that is twice the sampling clock frequency at 50 % duty cycle. A positive edge triggered D-flipflop connected as a ripple counter divides the frequency by 2, generating a 50 % duty cycle clock at the sampling frequency (signal C in Figure 4.7). A standard circuit used to generate the two phase clock outputs the phases ϕ_1 and ϕ_2 at the sampling frequency. The delay introduced by the diodes in the feedback path determine the duration of the dead time between the clock phases. Pass transistor logic is used to generate the signals PI_COPH1 and PI_COPH2 using delayed versions of the clock signals I and C as shown in Figure 4.8. Signal FB_SWH is obtained by 'AND'ing a delayed version of $\bar{I}$ and ϕ_2 . Delaying is critical as otherwise PI_COPH1 and PI_COPH2 may have glitches that would enable a comparison at the wrong instant. The number of pairs of inverters required to implement these and other delays, such as those that determine the dead zone, have been determined by simulation of the circuit extracted from the layout.

These clocks need to drive clock lines that span the entire chip. These lines could have a possible capacitance of 5 pF as determined from layout extraction. For operation in the MHz range, this line capacitance should be charged, say in 2 nsecs. The clocks should thus be buffered with transistors with large enough W/L to drive enough current to achieve the required rise time. The required W/L for the n and p transistors have been

Figure 4.8. Pass Transistor logic for generation of PI_COPH1 and PI_COPH2.

determined [18] to be 40 and 100, respectively. Every timing signal is buffered before it is connected to the lines distributing the signal all over the chip.

The partial layout of the timing circuits is illustrated in Figure 4.9. The section shown includes the D-flipflop, the two-phase clock generators, delay elements, pass-transistor logic and one buffer, in that order. The rest of the circuit is a repetition of the buffers for every signal and its compliment. Some of the building blocks like the D-flipflop, AND gates, NOR gates and the inverters have been modified from the cells available in the digital library of Tanner Tools layout editor LEdit.

4.5 Core Circuits

4.5.1 Operational Amplifier

The operational amplifier (opamp) is used to implement the integrator in the

Figure 4.9. Partial Layout of the Timing Generation Circuit.

sigma-delta modulator and the multiply-by-two and subtract unit in each stage of the pipelined ADC. The requirements on the opamp for both applications are similar. The specifications for the opamp can be derived for the opamp in the integrator, as discussed in the following paragraphs.

The input to the integrator is the difference of the input signal and the feedback digital-to-analog converter output. For the single-bit feedback system implemented, the feedback signal can change from negative reference to positive reference, i.e., the ADC step size (Δ). When integrated, it could possibly change the integrator output by Δ . For sinusoidal signal inputs, it can be shown by simulation that the output of the integrator is limited to values between $+\Delta$ and $-\Delta$, a total swing of 2Δ . This typically is the maximum voltage swing in the system and determines Δ and consequently the maximum signal input $x(t)$ to the system. (The input signal swing can at best be Δ). For a 5 V supply and fully-differential configuration, the maximum possible output swing is ± 5 V. For a practical circuit, the maximum gain region is typically limited to ± 3 V, limiting Δ and maximum signal input swing to 3 V. Maximum input dynamic range can be achieved by optimizing the opamp to handle rail-to-rail output swing.

$\Delta = 3$
 $\pm \frac{\Delta}{2} = \pm 1.5$

Every cycle, the integrator output can possibly change by Δ . The output of the opamp must be able to make this transition within a quarter of the clock period, as integrator output is expected to be valid at the later part of the integration clock phase, which is one-half of the clock period. The settling behavior of the integrator is determined by opamp slew rate (SR) and its unity gain bandwidth (UGB). Large signal settling is determined by both factors, while small signal settling is determined by the latter factor alone. Since the integrator handles large signal changes, both the SR and UGB specifications are important [19].

For large signal changes, most of the swing occurs while limited by slew-rate. The final settling time to the required accuracy is determined by the UGB and the phase margin. For sampling rate of 1 MHz, and a Δ of 3 V, the required slew-rate is 12 V/ μ -sec, which is reasonable. However, for a sampling rate (clock frequency) of 50 MHz, this increases to 600 V/ μ -sec, which is a difficult specification to meet with CMOS single-

stage opamps. The use of a second-stage in the opamp, biased to produce higher output current drive and consequently higher SR, introduces a second pole in the opamp, limiting its UGB. Circuit techniques to improve SR under large signal inputs have also been explored [16]. The use of bipolar or BiCMOS technology enables higher output currents at the cost of extra-power dissipation or more expensive process.

Since the opamp small signal settling should occur within one-fourth the clock period, the UGB should be at least an order larger than 4 MHz for a 1 MHz clock and 200 MHz for a 50 MHz clock. Minimum settling time is assured only if the opamp has a phase margin of 60° to 70° . As an example, for a 0.1 % settling with a 60° phase margin, settling time is around $5/UGB$ [19], which implies that UGB is greater than 20 times the sampling frequency. For the $2\ \mu$ CMOS process, UGBs of few hundred MHz are only possible, limiting the clock to few MHz.

In traditional single-loop single-bit sigma-delta modulators, the gain of the opamp is rarely a concern. In fact, published results [20] indicate that as long as the gain is greater than the oversampling ratio, the modulator will work. This is because the integrator is followed by the quantizer. The single-bit quantizer, in the extreme case, recognizes only the sign of the integrator output. After the opamp settles, the accuracy to which it is near the ideal is determined by the gain of the opamp, which is immaterial if only the sign is to be recognized. However, for the system under consideration, the integrator output needs to be accurate as it is further quantized with the residue being the input to the next stage. Furthermore, the gain of the opamp determines the pole accuracy. This pole error can limit the signal-to-noise ratio that can be achieved by the system, as discussed elsewhere. Thus a gain of 80 dB is desired for the opamp.

A given process, with a specified minimum line width, has a limit on the maximum gain and UGB that can be achieved [21]. The specification of 80 dB gain and few 100 MHz UGB is difficult to achieve in a $2\ \mu$ process. A target of 60 dB gain and 100 MHz is more realistic for the given process.

The use of fully-differential circuitry serves to mitigate the effects of common-mode signals. In fact, common-mode voltages at input and output need to be fixed by

circuitry external to the opamp itself. The effects of clock-feedthrough, signal dependent charge injection, noise coupling from substrate due to parasitic capacitance, etc., are also reduced due to the fully-differential configuration.

The opamp configuration that is best suited for such application is the folded-cascode configuration [22, 23, 24]. High gain can be achieved by the use of cascoded output transistors. In this single stage design, the primary pole is determined by the load capacitance and the second pole is determined by parasitic capacitance [25]. This parasitic pole is well separated from the main pole, allowing for a high UGB. Output common-mode voltage can be set by switched-capacitor techniques, transistors operating in linear region, or by separate common-mode amplifier [16]. Because of its suitability, the folded cascode configuration is used with a separate common-mode amplifier to set the output common-mode voltage. In what follows, the detailed design considerations are given.

The opamp that has been implemented is shown in Figure 4.10. The folded-cascode differential amplifier that forms the core of the opamp requires four bias voltages, three of which are generated by the bias circuitry. The fourth one is controlled by the common-mode feedback amplifier to maintain the output common-mode voltage.

The differential inputs are fed to the input differential pair M1 and M1_A at their

Figure 4.10. Fully-Differential Folded-Cascode Amplifier.

gates + IN and - IN, respectively. The differential output is available at nodes + OUT and - OUT whose quiescent (or DC) output is maintained at the value set externally at the common-mode reference (CM_REF) input of the common-mode amplifier. The external bias reference (BIAS_REF) sets up the current in MBREF that determines the current in the entire circuit. Since the transistor sizes associated with the bias circuitry is small compared to the rest of the transistors in the amplifier, each amplifier has its own bias circuitry rather than one bias generator supplying all the amplifiers in the chip. This reduces noise from digital circuits coupling through bias lines which is possible in all mixed-signal circuits. Further, routing problems are also mitigated. The analog supplies VDD_ANA and VSS_ANA correspond to 5 V and 0 V, respectively.

The operation of the common-mode amplifier is as follows. In the absence of common-mode feedback, since the output is taken between two (ideally) equal and opposite current sources, the quiescent (or DC) output voltages will approach either of rails, since ideal matching between the current sources cannot occur. The desired DC voltage required at the outputs is the value set at the external common-mode reference (CM_REF) which is 2.5 V. Under this condition, MC1_B,C,D and E carry identical currents. In presence of differential input, the output nodes are expected to swing equally in opposite directions such that the average of the voltages in the two nodes is 2.5 V. If this average voltage is different from 2.5 V, the two output nodes have some voltage component that rise (or fall) together. This results in the decrease (for a rise in the output common-mode voltage) of currents in MC1_B and E and corresponding increase of currents in MC1_C and D and consequently in MC3, which increases $V_{GS\ MC3}$, $V_{GS\ M3}$ and $V_{GS\ M3\_A}$. As the currents in M6 and M6_A are fixed by external bias, currents in M3 and M3_A cannot increase, so $V_{DS\ M3}$ and $V_{DS\ M3\_A}$ decrease to compensate an increase in $V_{GS\ M3}$ and $V_{DS\ M3\_A}$. This negates the initial rise in the common-mode output voltage. Equal and opposite differential output voltage swings cause an equal increase in one of MC1_B and E and decrease in the other, causing the sum currents in MC3 and MC3_A to remain unchanged. Thus a feedback signal is not created for differential inputs.

The relation between the drain current I_{DS} and gate voltage V_{GS} in a MOS transistor is given by

$$I_{DS} = \frac{1}{2} K' \frac{W}{L} (V_{GS} - V_T)^2 \quad (4.2)$$

where V_T , the threshold voltage of the device and K' , the transconductance parameter, are process related constants and W and L , the width and length of the device are determined by the designer. The process constants vary between different fabrication runs and are estimated only after the fabrication is complete. Thus, the design procedure used to determine the device sizing must be robust to ensure that the circuit is functional for the given possible process parameter variations, which could be as much as 30%.

Small signal analysis of the folded cascode configuration yields relations between the expected opamp performance and the device sizes [15]. Design equations have been published [25]. However, in view of the robustness required for the design, a simple design procedure that will ensure functionality has been realized. This procedure involves the concurrent design of both the amplifier and the associated bias circuitry. While many special bias circuits have been used [22], the bias circuit that has been used here provides for a systematic design of the amplifier.

The maximum current in the circuit is carried by M3, and the minimum current by MB3, the biasing transistor. The bias current is chosen to be I while the current through M3 is chosen to be $20I$. M1 supplies $8I$ and M4, $12I$ to make $20I$ through M3. M2 supplies $16I$ and M5 and M6 also carry $12I$. The current in M4 needs to be larger than that in M1. If they are made equal, no current will flow through M4 in the presence of large inputs diverting all the current from M2 to either M1 or M1_A, taking it out of saturation. MC1_B to E are made identical to M1 and carry the same current to assure the same frequency response for the common-mode amplifier as the main amplifier. Thus, MC2_A and B carry $16I$, and so do MC3 and MC3A.

From (4.2), the gate to source voltage of a transistor carrying current I_{DS} is

$$V_{GS} = \sqrt{\frac{2I_{DS}}{\beta}} + V_T \quad (4.3)$$

where β is $K'W/L$. The minimum drain to source voltage V_{DS} required to keep the transistor in saturation is $V_{GS} - V_T$. To achieve maximum signal swing, M3 should be biased such that it is just into saturation. Thus, for MB4, M4 and M3,

$V_{GS\ MB4} = V_{GS\ M4} + V_{DS\ M3}$. The current in MB4 is made $3I$ so that it can generate sufficient voltage to meet this condition while keeping its size small. Thus,

$$\sqrt{\frac{2 \cdot 3I}{\beta_{MB4}}} + V_T = \sqrt{\frac{2 \cdot 12I}{\beta_{M4}}} + V_T + \sqrt{\frac{2 \cdot 20I}{\beta_{M3}}} \quad (4.4)$$

Now a choice is made to size M3 and MB3 such that $\beta_{M3} = 20 \beta_{MB3}$ so that their V_{GS} are the same. This implies

$$\sqrt{\frac{2 \cdot I}{\beta_{MB3}}} + V_T = \sqrt{\frac{2 \cdot 20I}{\beta_{M3}}} + V_T \quad (4.5)$$

Solving for β_{MB4} in terms of β_{MB3} using (4.4) and (4.5), and taking $\beta_{M4} = 12 \beta_{MB3}$ (this step allows the independent device sizing for the cascode transistors) results in the relation $\beta_{MB4} = 3 \beta_{MB3} / 4$. Similar arguments apply for MB5, M5, and M6, resulting in $\beta_{MB5} = 3 \beta_{MB6} / 4$, taking $\beta_{M5} = 12 \beta_{MB6}$. MB3_A mirrors current in MB3 and MB3_B makes it three times. Similarly, MB6_A makes the current in MB6 three times. The choice of sizing for MB3 and MB6 then determine the sizes for MB3_A and B, MB4, MB5, MB6_A, M2, M3, M4, M5, M6, MC2A and B, MC3 and A.

The specification on the slew-rate determines the current in M1 and therefore all the branches in the opamp. The maximum current that can be sourced (or sunk) at the output nodes is the quiescent currents through M1. This current is then given by

$$I_{M1} = SR \cdot C_L, \quad (4.6)$$

where C_L is the load capacitance, and SR is the slew-rate. The opamp has been designed for a slew-rate of $240 \text{ V} / \mu \text{ sec}$. which gives a bias current of $480 \mu \text{A}$ for M1 with a 2 pF load.

The transconductance g_m of the input transistors M1 is determined by the UGB for the amplifier and the load capacitors through the relation

$$g_{mM1} = \omega_0 C_L \quad (4.7)$$

where ω_0 is the UGB and C_L is the load capacitor. The transconductance of the transistor is given by

$$g_m = \sqrt{\frac{K' W I_{DS}}{L}} \quad (4.8)$$

which indicates that the device sizing for M1 (and hence M1_A and MC1_B to E) can be obtained from specifications on the opamp, as the slew-rate determines the current in M1. Here the minimum value for K' from available parameters for different runs can be used to size M1 to assure required specifications. For this implementation, a UGB of 160 MHz is targeted, which results in a 2 mS transconductance and a W/L of 250 for M1 for a 2 pF load.

This design procedure depends very minimally on the process parameters and results in a working first-cut design. Various tradeoffs can then be made to optimize the circuit for some of the specifications.

The tradeoffs in this design include 4I excess current in the cascode transistor legs. This current can be reduced to increase the output resistance and hence the gain of the amplifier. While the current determines the output resistance of the cascode transistors, it is beneficial to make their transconductance large, since it is a factor in the output resistance of a cascode pair. The transconductance can be improved by taking larger W/L (at fixed current) for the cascode transistors at the cost of increased area and parasitic capacitance (which can potentially bring the nondominant pole to play a part in determining the phase margin) at the output node.

The V_T of the cascode transistors increase because of the bulk to source voltage. To accommodate this effect, the sizing on M4 and M5 are heuristically reduced to supply more voltage to the gate of M4 and M5. This will have the effect of increasing the V_{DS} on M3 and M6 assuring their operation in saturation, while sacrificing output swing.

The bias current is determined by the voltage at node BIAS_REF. If biased at 2.5 V, the opamp works in the high slew-rate low gain mode. If biased at any value above that, upto 4 V, the gain increases and slew-rate decreases. While the gain will not vary very much (in the range of 50 to 60 dB) the slew-rate will vary considerably. Such control

is beneficial while testing the chip. At high operating frequencies, the opamp can be in maximum slew mode and for low operating frequencies, it can be in high gain mode. So, this node is connected to one of the pins and the voltage can be set external to the chip.

The common-mode circuit input transistors MC1B to E have been made the same size as the input transistor M1 and biased at the same current to provide the same g_m and hence the same frequency performance as the main amplifier. For high switching speeds, the common-mode amplifier must respond fast enough to keep the output common-mode voltage within the operating limits of the input of the next stage. The trade-off is in the

Table 4.1. Design Considerations and Device Sizing for the Folded-Cascode Amplifier

Device	Design Relation	Size (μm)	I_{DS} (Quiescent)
M1, M1_A	$\frac{W}{L} = \frac{(2\pi \cdot U_{GB} \cdot C_L)^2}{2 \cdot K' \cdot I_{DSM1}}$	500 / 2	$I_{DSM1} = SR C_L$ $= 8I$
M2	$\beta_{M2} = 16 \beta_{MB6}$	400 / 2	16 I
M3, M3A	$\beta_{M3} = 20 \beta_{MB3}$	400 / 2	20 I
M4, M4A	$\beta_{M4} = 12 \beta_{MB3}$	240 / 2	12 I
M5, M5A	$\beta_{M5} = 12 \beta_{MB6}$	300 / 2	12 I
M6, M6A	$\beta_{M6} = 12 \beta_{MB6}$	300 / 2	12 I
MBREF	$\beta_{MBREF} = 2I / (BIAS\_REF - V_T)^2$	6 / 2	I
MB3, MB3A		20 / 2	I
MB3B	$\beta_{MB3B} = 3 \beta_{MB6}$	60 / 2	3 I
MB4	$\beta_{MB4} = 3 \beta_{MB3} / 4$	39 / 8	3 I
MB5	$\beta_{MB5} = 3 \beta_{MB6} / 4$	48 / 8	3 I
MB6		25 / 2	I
MB6A	$\beta_{MB6A} = 3 \beta_{MB6}$	75 / 2	3 I
MC2A, MC2B	$\beta_{MC2A} = \beta_{M2}$	400 / 2	16 I
MC1B, C, D, E	$\beta_{MC1A} = \beta_{M1}$	500 / 2	8 I
MC3, MC3A	$\beta_{MC3} = 16 \beta_{MB3}$	320 / 2	16 I

Figure 4.11. Layout of the Fully-Differential Folded-Cascode Amplifier

chip area and power consumption which are considerably increased. Switched capacitor common-mode feedback circuitry may be utilized to mitigate this condition, but have not been implemented in this realization as chip area and power consumption are not of concern.

The above design considerations are summarized in Table 4.1. The device sizing used for the fabricated opamp is also shown. PSPICE simulation for this design with parameters from run N6AB [26] of 2 micron Orbit process showed a gain of 56 dB, a UGB of 200 MHz and a linear output range of ± 2.3 V (with saturation limits at ± 4 V) for a 50 μ A bias current I . The circuit was also simulated with parameters from other runs of the same process, yielding similar characteristics. The circuit extracted from the layout design included all the parasitic capacitances and showed a 58 dB gain, 200 MHz UGB, and a ± 3.5 V linear output range with a typical parameter set for the 2 micron process. A set of three opamps were fabricated in run N73C and tested.

The layout of the opamp is shown in Figure 4.11. The important feature of this layout is the 'cell' type of layout, enabling the adjacent placement of other cells that continue the horizontal flow of supply and reference voltage lines in the metal 1 layer. The outputs are available along the vertical direction in the metal 2 layer. The layout of the opamp emphasizes matching of transistors by interdigitized layout, in contrast to a symmetric structure that utilizes the inherent symmetry of a fully differential structure. The input transistors M1 and M1A (as also MC1B and C and MC1D and E) have been isolated in their own n-well to suppress noise coupling from the substrate and power lines. The sources of these devices have been tied to the n-well as is indicated in the circuit in Figure 4.10. Large transistors have been laid out in the 'stacked' configuration [22] rather than on single transistor as the parasitic capacitances are considerably reduced because of the reduction in the area of the source and drain diffusions. Guard ring substrate noise protection has been provided to isolate the p and n transistor regions and to reduce chances of latch-up, even though considerable chip area is consumed.

4.5.2 Comparator

The high signal-to-noise ratios obtained from a sigma-delta converter utilizing a coarse quantizer is primarily because of the fact that the quantization noise introduced by the quantizer is noise shaped. Any signal introduced into the sigma-delta loop between the integrator and the quantizer is noise shaped. For this reason, non-idealities in the implementation of the quantizer are noise shaped and their effect on the signal-to-noise ratio is negligible. However, single-bit quantizers are preferred in the sigma-delta loop to prevent the addition of digital-to-analog converter errors that are not noise shaped. A latch type comparator, that has the advantage of high speed, is suitable for this application as a single-bit quantizer. Typically, a resolution and offset in the vicinity of 10 mV, and hysteresis of the order of 5% of the step size [7] are tolerated and response time is in the order of few tens of nanoseconds.

Pipelined converters, on the other hand, rely on the accuracy of the comparison for analog to digital conversion. The accuracy of the latch type comparator is improved by

Figure 4.13. Layout of the Differential Comparator

A standard cross-coupled inverter type comparator, shown in Figure 4.12, has been chosen for implementation. This design, has been used in sigma-delta modulators and tested for operation at 5 MHz [27]. The comparator is inoperative and outputs a low when PHI_COMP is low. As it goes high, input that has a higher voltage will pass more current through that input transistor. This extra current is increased by the positive feedback generated by the cross-coupled inverters MO2A, 4A and 2B, 4B, ultimately driving one output low and the other high. The layout of the comparator is shown in Figure 4.13. The 'cell' type layout once again maintains the supplies laid out horizontally in metal 1 and inputs and outputs laid out vertically in metal 2. The supplies have been made different from the opamp supply so that the sharp transitions in current that occur when switching do not cause noise in the opamp. Double guard-ring latch-up and substrate noise protection is provided as in the case of the opamp. PSPICE simulation of the extracted circuit showed an offset of less than 10 mV and a delay time of less than 5 nsec, which was within expectations.

4.5.3 Capacitors

The accuracy of the integrator and multiply-by-two circuits depend upon the ratio matching of capacitors. The gain of these circuits is directly proportional to capacitor ratio. In the case of the integrator, the capacitor ratio is also a factor in the expression for the pole error. The pole error caused by low opamp gain is the dominant limitation on the signal-to-noise ratio of pipelined sigma-delta modulators, as discussed in Section 5.4.1.

Further, for high-resolution converters, the thermal noise associated with the sampling capacitors can limit the signal-to-noise ratio.

Of the many pairs of layers that can be utilized to implement capacitors, the poly-poly capacitor has the best linearity and highest capacitance per unit area (apart from the gate capacitance). Digital processes usually do not support poly-poly capacitors. However, these capacitors are available in the Orbit 2 μ analog process and are utilized to implement the capacitors. For this process, the capacitance per unit area was around 0.48 fF / μm^2 , giving 0.19 pF for unit capacitors of 20 μm square.

The capacitor ratio matching is degraded due to the undercut that results in a area slightly reduced than that defined in the mask. This effect is mitigated if the area to perimeter ratio of the capacitors are the same [16,21,22]. In implementation, this condition is achieved by implementing the capacitors as a number of unit capacitances in parallel. The area-to-perimeter ratio of each of these units are the same, and the effect of the undercut on the capacitance ratio is diminished. This strategy has been used in this implementation where each capacitor of 1.9 pF is made of 10 unit capacitances of 20 μm square each.

Fabrication process inaccuracies can cause nonuniform insulator thickness across the wafer, which can result in different capacitor ratios than designed for. This is especially true since capacitors consume a lot of area and can be accentuated if all the units of each capacitor are grouped together in one location. The effect of a gradient in the insulator can be nullified by placing the capacitor units in a common centroid geometry. This philosophy has been utilized to layout three capacitors symmetrically, each made of 10 units as shown in Figure 4.14. The 10 units for each capacitor have been distributed as groups of 3, 3, 2 and 2, spread horizontally, with one set of 3 and 2 units in the top row and the other set in the bottom row. These sets have been connected in cyclic order. The bottom plate of the capacitors have been shielded from substrate noise by the use of a n-well under the capacitors, which is connected to a 'quite' positive supply

Figure 4.14. Matched Layout of Three Capacitors of 1.9 pF each.

The maximum possible signal to thermal noise ratio associated with the sampling capacitors has been shown [20] to be

$$\text{SNR}_{\max} = \frac{V_{\text{in}}}{2} \sqrt{\frac{\text{OSR} \cdot C}{kT}} \quad (4.9)$$

where $\text{SNR}_{\max}$ is an amplitude ratio, OSR is the over sampling ratio, C is the sampling capacitor, k is the Boltzmann constant, T is the temperature in Kelvin, and V_{in} is the input signal amplitude. For a low OSR of 8, an input of 1 V amplitude (2 V peak to peak) and a capacitance of 1.9 pF, this translates to about 14 bit resolution, while for an OSR of 64, it increases to about 16 bits. Therefore, the maximum resolution that can be expected from the system is about 16 bits.

4.5.4 Switch

The transmission gate has been used as a switch consistently throughout this design, even though at the opamp virtual ground nodes the use of a single minimum size n-switch is adequate because of low signal swings and preferable because of reduced parasitic capacitances. The requirements on the switches used is that the 'ON' resistance should be such that the capacitors being switched settle to their final voltage, with the required accuracy, in one phase at the maximum clock speed to be used. The n and p-channel transistors that comprise the switch each have a W/L of 20. A rough estimate of the 'ON' resistance for this switch is 1.5 K Ω which gives a time constant of 20 n sec with a 2 pF

capacitor. For adequate settling, assuming a two phase clock and 10 time constants are utilized for settling within one phase, 2.5 MHz is the maximum clock frequency that can be utilized. Increasing the switch size involves a trade off of adding parasitic gate-to-source and gate-to-drain capacitances that contribute to charge injection into the signal path from the clock signal. However, this effect is mitigated by the use of fully-differential circuitry.

In switched capacitor circuits, very often a pair of switches share a common node. The layout of such a pair of switches is shown in Figure 4.15. The use of a 'cell' based layout enables the four clock signals to run horizontally through multiple switches, while the inputs and outputs run vertically.

4.6 System Integration

After the circuit layout is done, the inputs and outputs for the circuit are connected to the pads in the layout. Pads are large metal squares on to which wires will be bonded after chip fabrication. Pads also contain static protection circuitry which are extremely important for the CMOS circuits. The location of pads on a chip is constrained by bonding requirements. Usually, pads form the periphery of the circuit to facilitate easy bonding. The wires bonded to the pads connect to the chip carrier bond pads which are connected

Figure 4.15. Schematic and Layout of a pair of Transmission Gates.

to the pins outside the chip carrier package.

The integrated circuits (or 'chips') have been fabricated using the MOSIS Orbit 2 μ , scaleable, CMOS, n-well, analog (SCNA), low-noise, double-poly, process. Each specific process has its set of design rules. Each layout needs to conform to these design rules. The task of design rule check (DRC) is performed on the layout editor using the DRC file associated with the process. The technology file contains the allowed layers, the allowed connections between layers, inter layer capacitances and other process dependent information necessary for DRC as well as for circuit extraction. The circuit is extracted from the layout and verified using the circuit simulator. The completed layouts are then

Figure 4.16. Layout of Chip N74CFA

a pad frame that has 40 pads, of which 36 can be used for connecting input and output signals. The complete chip layout including the pads is shown in Figure 4.16. The chip to chip-carrier connection diagram is provided by MOSIS and results in the pinout shown in Figure 4.17.

4.6.2 Chip N74LFH

The chip, N74LFH, was designed to implement the proposed sigma-delta modulator system. It consists of three stages, each consisting of a single-bit first-order modulator and a 4-bit pipelined quantizer. The first modulator stage M1 takes its input from external sources, for example, a signal generator. The process of input sampling and integration negates the input signal, i.e., if signal X is connected to the pins of the chip, $-X$ is the actual signal input. It generates the modulator digital output Y_1 . The error output of this modulator is sampled by the following four-bit quantizer that outputs four digital signals, $P1M1$, $P2M1$, $P3M1$ and $P4M1$ and the residue, which is the scaled inverted quantization error introduced by this multibit quantizer. This residue is sampled and inverted by the second stage modulator, which outputs Y_2 . The error output of this modulator is sampled by the following four-bit quantizer that outputs four digital signals, $P1M2$, $P2M2$, $P3M2$ and $P4M2$ and the residue, which is unutilized. The third stage is configured to take external input and output relevant analog nodes as well as the digital signals. Specifically, the differential analog outputs are those that are valid in ϕ_1 : the integrator output ($OUT1 \pm M3$), the residue of the second unit of the pipelined converter ($OUT2 \pm M3$), and the residue of the fourth unit of the pipelined converter ($OUT3 \pm M3$). This allows connection of any of the three outputs to the input of the first stage, allowing for a multitude of modulator configuration to be tested. However, connecting these nodes to the pads (and other external load, if any) adds a large load capacitance to the respective nodes reducing the operating speed for the third stage. The digital outputs of the third stage are Y_3 , $P1M3$, $P2M3$, $P3M3$ and $P4M3$. The reference inputs required by the chip are the bias reference ($BIAS\_REF$), the common-mode reference (CM_REF), the modulator feedback references ($SD \pm REF$) and the multibit pipeline converter references

Figure 4.18. Layout of the Chip N74LFH with the Bonding Diagram.

(PIP±REF). The signal FB_SWH is asserted in the later half of ϕ_2 , when all digital signals are valid, but may require delay in the order of tens of nanoseconds to act as a data-ready signal. The pinout for the chip is shown in Figure 4.17.

A standard 40 pin DIP is used to mount the 6 mm x 4 mm chip. This package causes a rise in temperature of less than 100°C for a 3 W dissipation, and less than 30°C rise for a dissipation less than 1 W [28] with no forced air cooling. For biasing in the high slew mode, that draws the maximum current, each opamp draws close to 5 mA. Since the static dissipation of the rest of the circuit is considerably less, an estimate of the static power dissipation in the chip is close to 0.36 W. Even adding the dynamic power

dissipation of the digital circuits, which is frequency dependent, the thermal requirements on the package are adequate.

Both analog and digital signals are input and output from the chip. This calls for two different types of pads, as the analog pads conduct the signal directly to the pins, while the digital pads have a digital buffer interface. A custom frame that incorporates modified analog and digital, input and output pad cells available from MOSIS [26] cell-libraries has been made. The pad centers, for the particular chip size, conforms to the recommended specification of MOSIS. The layout of the system is fitted into this pad and is shown in Figure 4.18.

The pads are connected to the bond fingers as also shown in Figure 4.18. The bond fingers are connected to the pins that are outside the package. This connection can be modeled as a series combination of a resistor and a inductor between the finger and pin, with a capacitor connected to the ground from the pin [28]. These parasitics are maximum for pins 1, 20, 21 and 40 and decrease progressively from the side centers to the top and bottom centers. Hence it is advantageous to connect the supplies at the side centers and the high frequency signals at the top and bottom centers. Further, it is also advantageous to separately connect the analog and digital supplies. Since the analog supply takes a large current, two pins are allotted for supply and ground each, on the left center. The digital supplies occupy the right center. The substrate effectively connects the analog and digital ground which are connected to it through the substrate guard rings. The supply required for the frame itself, for the pad drivers and static protection circuits, has been connected to the digital supplies.

The digital pad drivers are a potential source of substrate coupling, as they switch the output loads. For this reason the placement of analog pads as far as possible from the digital pads is favorable. Thus the analog signals are concentrated at the left while the digital are concentrated to the right. The input clock, the highest frequency digital signal with the least load, has a grounded pad separating it from an analog output. The differential signals are placed on adjacent pads to reduce any differential noise pick up.

The clock circuits have been placed in the center to reduce the maximum clock delay to the extremities. The cell oriented circuit layout is extremely beneficial at this stage, as all that is required is the placement of individual circuits next to each other. This automatically ensures the transport of signals to every cell. The analog references are distributed to the cells using the vertical metal 2 busses on the left. Similarly the clock and other digital signals are distributed using the vertical metal 2 busses on the right. Inside the circuits, all the analog signals are shielded from the digital signals by running a grounded metal line between the two groups.

The suggested layout [22] for the differential circuits with the analog circuits in the center, followed by the capacitors, and the digital circuits in the periphery is followed within each cell. This layout philosophy could also be applied on a global level, with all analog circuitry in the center and shielded from digital circuits in the periphery. However, the complexity of interconnections is tremendous and location of layout errors, in the event of circuit malfunction, is extremely difficult. On the other hand, the use of tested and verified cells ensures circuit functionality while the double guard-ring shielding is expected to mitigate substrate noise coupling.

In summary, this chapter strives to elucidate the intricacies involved in the design and implementation of the pipelined sigma-delta modulator with interstage scaling. The next chapter describes the testing of the two fabricated chips.

CHAPTER 5

SYSTEM TESTING AND RESULTS

5.1 Overview

This chapter describes the testing procedures and results obtained from testing the two chips, N73CFA, that contains the opamp and the comparator and the chip N74LFH, that contains three stages of the pipelined sigma-delta modulator with interstage scaling. Each of the chips require some external circuitry and programming to do the various tests. These circuits and programs are described. The results obtained are discussed.

5.2 Testing of Chip N73CFA

5.2.1 Testing of the operational amplifiers

Chip N73CFA contains three identical opamps and two identical comparators in a 2 mm x 2 mm TinyChip. MOSIS, the chip fabrication service, provides four pieces of the chip. The opamps require supplies VDD_ANA, VSS_ANA, the common-mode reference voltage CM_REF, the bias reference BIAS_REF, and the inputs IN+ and IN-. With reference to the layout in Figure 4.16, the opamps are named top left (TL), bottom left (BL) and bottom right (BR). The corresponding pinouts are shown in Figure 4.17. The chips are numbered one to four.

The supplies chosen for the entire system is a single 5 V supply. Hence the opamp terminals VDD_ANA and VSS_ANA are connected to 5 V and 0 V, respectively. Setting the bias reference to 2.5 V results in a high slew mode and setting it to 4 V results in a low slew, higher gain mode. The pins IN+ and IN- are connected to the gates of the opamp differential input transistors. The DC bias voltage, or the common-mode input voltage, at these inputs need to be set. When the opamp is used as a part of the entire modulator system, it faces the output common-mode voltage CM_REF of the previous stage. Hence the input common-mode voltage is also chosen to be the same as CM_REF, which is taken to be 2.5 V, the center of the supply range. This setting is done externally by using a potential divider resistance network, shown in Figure 5.1, which also converts the single-

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ended output of the function generator to a differential input for the opamp. This is possible because the outputs of the function generator can be floated, i.e., not referenced to the earth ground inside the function generator. The 100 K resistors bring the input common-mode voltage close to 2.5 V, which is then precisely adjusted to that value using the 10 K potentiometers.

Under these conditions, two types of tests can be performed. The first is the DC sweep test, in which a low-frequency triangle wave is applied to sweep the differential input voltage from - 5 to + 5 V. The differential output must change from + 5 V to - 5 V at 0 V input. Some portion around the center of the output is linear. The slope of the linear transition determines the open loop gain of the opamp. The limits of the linear transition determines the output voltage range of the opamp. The input voltage range in which this linear output voltage change occurs is the opamp open-loop input voltage range, where the signal is amplified by the open-loop gain of the opamp. This input range, and hence the gain, can be directly measured only for opamps with low gain, as is the case of the opamp under test with an expected gain 60 dB, for higher gain (say 80 dB) results in extremely small input range (less than 100 μ V) and impractical measurement. This test resulted in an average gain of 50 dB and linear output range of 4.5 V at a bias voltage of 3.9 V, the average taken over all the 12 opamps.

The second test is the frequency test in which a sinusoid of magnitude less than the open-loop input range is applied, and its frequency is varied to get the frequency response of the opamp. Again, this test is practicable only if the opamp gain is low. The unity gain bandwidth (UGB) is the frequency at which the input and the output have the same magnitude. A test of this type with a 10 mV input signal indicated a UGB of about 3 MHz. The frequency test can also be performed by connecting the opamp in a unity gain configuration, as shown in Figure 5.1, and sweeping the frequency. The UGB is then the frequency at which the output is 3 dB below the expected unity gain output. With a 1 V input and all capacitors as 5 pF this test also yielded a UGF close to 1 MHz.

While these results indicated the functionality of the opamp, they indicated a result inconsistent with that predicted by the Level 2 simulations in PSPICE. Simulation of the

Figure 5.1. Opamp in the Unity Gain Configuration.

extracted circuit with the empirical BSIM 1 model and model parameters obtained from the run N73C on which the chip was made, indicated a better match of the gain to the simulation, at 50 dB with a bias of 3.9 V. However, the model still predicted 80 MHz for the UGB under no load conditions, and 20 MHz with a load of 5 pF which has probably not been observed due to the limitations of the experimental set up.

The next test is to subject the opamp to a step input and confirm the settling time, which will depend on the slew rate achieved. The test circuit is the same as in Figure 5.1, except that both outputs have an additional 5 pF load to the circuit ground. The least settling time observed for varying bias references was about 800 nsecs., which corresponded to a maximum operating speed of close to 500 KHz.

In summary, the opamp loaded with the pads and external circuitry, both at the input as well as the output, showed a gain of 50 dB, output range of 4.5 V, UGB of 3 MHz and a large signal settling limited frequency of operation to be 500 KHz. However, the frequency specifications can possibly be expected to be underestimates for the opamp used as a building block in a larger integrated system.

5.2.2 Testing of the Comparator

Just as for the operational amplifier, the differential input terminals are biased at the common-mode output voltage of the opamp, i.e., 2.5 V, as shown in Figure 5.1. The operation of the comparator is dynamic, i.e., comparison occurs on the positive going edge of the strobe and the output is retained until the strobe is high. When the strobe is

low, output is low, as explained in the section on comparator (4.5.2). To obtain the maximum operating speed of the comparator with pad and external loads, a high differential input is applied and the strobe frequency is swept. It was found that a maximum operating frequency of 1 MHz was possible. This probably is an underestimate with the reduced loads, if the comparator operates as a part of a larger integrated system. To find the comparator offset, a triangle sweep at 25 KHz is applied to the differential inputs, and the comparator is strobed at 1 MHz. The differential input at which the comparator shows a change of state in the output is the offset voltage of the comparator. For the eight comparators tested, offsets measured ranged from -0.4 V to +0.4 V. Further confirmatory test was made on some of the comparators by manually varying the input differential voltage near this measured offset using a DC source and then measuring the DC voltage when the transition occurs. This rather large offset for the comparator occurs probably due to device mismatch in the fabricated circuit.

The measured performance of the building blocks was found to be less than the design targets achieved with the Level 2 model in PSPICE. The results obtained from the overall modulator system could thus be adversely affected by the performance of the building blocks. The consequence of these non-idealities, which will inevitably exist in any practical implementation, is observed in the physical testing of the modulator, as described in the next section.

5.3 Testing of Chip N74LFH

The chip, N74LFH, was designed to implement the proposed sigma-delta modulator system. The layout, pinout and other considerations are discussed in Section 4.6.2. This section describes the testing of the two-stage pipelined sigma-delta modulator with interstage scaling that utilizes single-bit first-order modulator loops and four-bit pipelined quantizers.

The objective of the testing procedure is to obtain the signal-to-noise ratio (SNR) at the output Y of the system shown in Figure 3.1. As described in Section 4.6.2 the analog portion of the modulator has been implemented in the chip. The digital portion of

the scheme in Figure 3.1 is implemented as a computer program. It should be noted that the actual analog-to-digital converter would in fact use a digital signal processing hardware, may be on the same chip, to implement the digital functions as well as low-pass filtering and decimation.

The requirements on a testing system are as follows. The modulator oversamples the input signal and outputs a digital word in every sampling instant. This data must be acquired on to the testing system at the sampling rate. This data acquisition must proceed for sufficiently long time to encompass few cycles of the input signal as well as enough data to make the SNR measurement possible. Usually, the latter constraint is more demanding, as the region of the output spectrum that we wish to calculate the SNR in is actually the baseband $F_s / (2 \cdot \text{OSR})$ where as the number of points available to compute the frequency spectrum in a region F_s is limited to the available number of sample points. As the measurement of SNR is dependent on the identification of signal and harmonic peaks and estimation of signal power, at least 1024 points are needed in the baseband, and at least 32 K sample points for a modest OSR of 16. Further this data transfer is required to be done at the sampling rate, which could be greater than 1 MHz. Once the data is stored, it should be accessible for data analysis. The large amount of data storage and computation is best done on a computer. The high sampling rate is accommodated by using a data acquisition card from National Instruments (PCI-DIO-32HS) capable of direct memory access (DMA) on the high speed PCI bus in a personal computer.

The input common-mode voltage needs to be set externally and is achieved by the resistor divider network described in the previous section. In addition, a passive bandpass filter with pass band 100 Hz to 10 KHz has been utilized at the input to reduce DC, harmonic and high frequency introduction into the system as also for anti-aliasing to a limited extent. The input circuit incorporating the bandpass filter is shown in Figure 5.2.

A delayed version of the FB_SWH signal was expected to provide the 'data ready' information to enable or strobe data collection. However, this pin was found to be non functional in all the 12 chips. Therefore, an external state machine was devised to

generate this information with the output of the modulator and the input clock to the chip being inputs to this state machine.

Data is collected using the data acquisition board driver LabView from National Instruments. The data is collected on to a file in a 16 bit format, 15 bits from the system and the one clock input to the chip. The individual bits that comprise this data word are related to different samples, as the pipelined nature of the system introduces latency. Thus, as the first step, these bits are separated and delayed to form meaningful digital information. The digital signal sequencing for the two-stage modulator under study, for sample 'n', is detailed in Table 5.1. Once separated, all the digital signals are scaled. The actual ADC/DAC combination in the sigma-delta modulator does not operate with 0 and 5 V for a high and low; instead, these levels refer to SD+REF and SD-REF. The multibit pipeline ADCs output is converted to a analog quantized value by assuming ideal thresholds and gains for the ADC. Then these signals are differentiated (noise shaped) and added to the modulator output (which is a permissible operation since all mathematical estimation procedures that are used to analyze the signals are linear). A power spectrum of the result is indicative of the SNR obtained at the modulator output.

Unfortunately, this power spectrum is not suitable for harmonic estimation or for the calculation of signal to total noise ratio. This is because the signal peak is very broad due to the inherent nature of the power spectrum estimation. The use of a windowing function considerably improves the estimation process. Hence, an estimation procedure

Figure 5.2. Input Bandpass Filter and Bias Circuit.

that more closely approximates the analog-to-digital converter has been adopted. The signals are first low-pass filtered to reduce the out of band noise to about -100 dB. Then, the signal is decimated and windowed with a Blackmann-Harris 4-term window. Power spectrum of the output then resulted in a sharp peak. Harmonic estimation gives the total harmonic distortion (THD) as

$$\text{THD}\% = 100 \frac{\sqrt{a_2^2 + a_3^2 + \dots + a_n^2}}{a_1}; \quad \text{THD(dB)} = 20 \log_{10} \left(\frac{\sqrt{a_2^2 + a_3^2 + \dots + a_n^2}}{a_1} \right)$$

with the power of the i th harmonic expressed as a_i and n harmonics are utilized to calculate the THD. If in the above equation instead summing only the harmonic power, all the noise power in the baseband is also included, then the result is the total harmonic distortion plus noise. It can be seen that the signal-to-total-noise ratio is the negative of THD+noise expressed in dB.

Table 5.1. Digital Signal Sequencing. All digital outputs are valid only in the later half of ϕ_2 .

Cycle	ϕ_1 First half	ϕ_1 Second half	ϕ_2 First half	ϕ_2 Second half
1	Sample $x(n)$, negate	Output $e(n-1)$	Integrate $x(n)$	Output $Y_1(n)$
2	Integrate - $Y_1(n)$	Output $e_1(n)$ Sample $e_1(n)$ Output $P1M1(n)$	Cal. residue bit 1 Output $P1M1(n)$	Out residue bit 1 Sample residue 1 Output $P2M1(n)$ Output $P1M1(n)$
3	Cal. residue bit 2 Output $P2M1(n)$	Out residue bit 2 Sample residue 2 Output $P2M1(n)$ Output $P3M1(n)$	Cal. residue bit 3 Output $P3M1(n)$	Out residue bit 3 Sample residue 3 Output $P4M1(n)$ Output $P3M1(n)$
4	Cal. residue bit 4 Sample residue 4, negate Output $P4M1(n)$	Out residue bit 4 Output $P4M1(n)$	Integrate	Output $Y_2(n)$
5	Integrate - $Y_2(n)$	Output $e_2(n)$ Sample $e_2(n)$ Output $P1M2(n)$	Cal. residue bit 1 Output $P1M2(n)$	Out residue bit 1 Sample residue 1 Output $P2M2(n)$ Output $P1M2(n)$
6	Cal. residue bit 2 Output $P2M1(n)$	Out residue bit 2 Sample residue 2 Output $P2M2(n)$ Output $P3M2(n)$	Cal. residue bit 3 Output $P3M2(n)$	Out residue bit 3 Sample residue 3 Output $P4M2(n)$ Output $P3M2(n)$

Figure 5.3. Experimental Results of the THD and THD+noise at the Output of the First-Order Single-Bit Modulator (top graph), First-Stage (middle graph) and Second-Stage (bottom graph).

$\pm 3V$
 $\Delta = 3$
 $\frac{4}{2} = 2$

The two stage pipelined sigma-delta modulator with interstage scaling was tested assuming a 6 V linear output range for the opamp. Thus, the single-bit analog-to-digital converter step size Δ was taken to be half of the linear output range of the opamp, at 3 V. This implies that for a high or low decision of the comparator, 1.5 V was either subtracted or added, respectively, to the integrator. This implied a SD+REF of 3.25 V and SD-REF of 1.75 V. Under these conditions, the maximum error introduced by the single-bit analog-to-digital converter in the modulator is expected to range between +1.5 V and -1.5 V. To derive the maximum benefit out of the pipelined multibit converter, PIP+REF was set to 1.5 V and PIP-REF was set to 0 V, so that the full-scale range was set to ± 1.5 V. The input signal was 2 V peak-to-peak at 1000 Hz, with a band width taken to be 8 KHz.

This signal was oversampled by a factor of 8 at a sampling frequency of 128 KHz. Results are displayed in Figure 5.3 in which the input signal at 1 KHz is clearly visible. The first two numbers on the right of graphs display the THD and THD+noise ratio in % in the top row and in dB in the following row. The top graph displays the spectrum in the baseband at the output of the first-order single-bit modulator Y_1 with a SNR of 50 dB and a STNR of 22.5 dB. The second graph displays the spectrum at the output of the first stage Y_1' and the multibit modulator is seen to reduce the noise floor considerably. The SNR and STNR are seen to be 66.5 and 41 dB, respectively. The second stage reduces the noise still further, giving an SNR and STNR of 74 and 49 dB, respectively. Considering the STNR of 49 dB, it corresponds to 8 bit resolution at an oversampling ratio of 8. This result clearly indicates the feasibility of the proposed pipelined sigma-delta modulator with interstage scaling.

5.4 Implementation Nonidealities in the Proposed System

Though the result presented above validates the proposed system, it does not reflect the full potential of the system. Nonidealities in the implementation of the modulator and the pipelined analog-to-digital converter limit the signal-to-noise measurements obtained from the system. Much better performance can be realized with building blocks that perform better than those that make up this implementation. The requirements on the building blocks to achieve expected performance are investigated in this section.

5.4.1 Integrator Leakage

The opamp used to construct the integrator typically faces the design tradeoff that involves a slew-rate and unity gain bandwidth on one hand and the gain on the other. Usually, the gain of the opamp is sacrificed, as the integrator output need to settle to a value less than the quantization error introduced by the following analog-to-digital converter. While this is acceptable for topologies that are based on a single quantizer Candy structure, it causes the presence of unshaped or lower order shaped quantization noise in the output of Mash, Leslie-Singh and other multistage topologies.

The transfer function of the integrator implemented with a nonideal opamp with gain A in a switched capacitor circuit is given by [29]

$$H(z) = \frac{1}{\frac{C_2}{C_1} \left(1 + \frac{1}{A}\right) (1 - z^{-1}) + \frac{1}{A}} \quad (5.1)$$

where C_1 and C_2 are the sampling and integrating capacitors. With

$$\alpha = \frac{1}{1 + \frac{1}{A} + \frac{C_1}{C_2} \frac{1}{A}} \approx 1 - \frac{2}{A} \quad (5.2)$$

and

$$\beta = \frac{1}{1 + \frac{C_1}{C_2} \left(\frac{1}{A+1}\right)} \approx 1 - \frac{1}{A} \quad (5.3)$$

the transfer function can be written as

$$H(z) = \frac{C_1}{C_2} \frac{\alpha}{1 - \beta z^{-1}} \quad (5.4)$$

where $1-\alpha$ and $1-\beta$ are the gain and pole errors, respectively. Capacitor ratios can be made accurate to 0.1 % [16] and opamp DC gain is typically 1000 or 60 dB. Then, $\alpha = 0.998$ and $\beta = 0.999$, with C_1 / C_2 as 1.001. It should be noted that α and β are, to the first order, dependent on the gain and to a lesser extent dependent on the capacitor matching.

Considering the single-bit two-stage MASH structure shown in Figure 2.4, the dominant terms in the output Y of the modulator incorporating the integrator leakage is given as

$$Y \cong \alpha_1 X z^{-1} + (1 - \beta_1) E_1 z^{-1} + (1 - z^{-1}) \left((1 - \alpha_2) E_1 z^{-1} + (1 - \beta_2) E_2 z^{-1} \right) + E_2 (1 - z^{-1})^2, \quad (5.5)$$

where subscript 1 and 2 refers to quantities in the first and second stages. The digital differentiator transfer function $(1 - z^{-1})$ is taken to be implemented as the difference of two digital words and hence precisely achieved. This equation displays only the dominant few terms of the actual output. Only the first and last terms are actually expected out of the ideal modulator. The second term can potentially limit the signal-to-noise ratio that can be

achieved using this converter, as it is not noise shaped. At high oversampling ratios, the second-order noise shaping function will attenuate the last term to a large extent, the third term is attenuated by the first-order noise shaping function, and so, the unshaped second term will be the primary error component in the output. This term is associated with the pole error of the first integrator. The same arguments can be applied to the cascade of many stages to obtain higher-order noise shaping and the usefulness of the MASH structure is reduced.

A similar analysis shows that the output of the topology of Figure 2.7 is

$$Y \cong \alpha Xz^{-1} + (1 - \beta)E_1z^{-2} + (1 - z^{-1})((1 - \alpha)E_1z^{-1} - E_2) \quad (5.6)$$

where E_1 and E_2 are the single-bit and multibit quantization errors, respectively. It can be seen that the signal-to-noise ratio is once again restricted by the pole error leakage. Further, the number of bits that can be utilized in the multibit quantizer is limited by the gain error leakage.

The linear model for the proposed system 3.1 predicts the following dominant terms in the output

$$\begin{aligned} Y \cong & \alpha_1 Xz^{-1} + E_1(1 - \beta_1)z^{-3} \\ & + (1 - z^{-1})z^{-1} \left[E_1(1 - \alpha_1)z^{-1} - E_2((1 - \alpha_2) + (\alpha_1 - \beta_1)z^{-1}) + \frac{E_3}{K}(1 - \beta_2)z^{-1} \right] \\ & + \frac{(1 - z^{-1})^2}{K} \left[E_3(1 - \alpha_2)z^{-1} - E_4(1 + (\alpha_2 - \beta_2)z^{-1}) \right]. \end{aligned} \quad (5.7)$$

The integrators are modeled with $1 - \alpha$ and $1 - \beta$ as the gain and pole error respectively with the subscripts denoting the stages. A comparison with the ideal expected output in (3.7) shows the presence of unshaped first-stage pole error, first-order shaped errors from the first and second stages and second-order shaped gain error, in addition to the expected second-order shaped and scaled error E_4 . Ideally, the quantities $1 - \alpha_i$, $1 - \beta_i$, and $\alpha_i - \beta_i$ are 0 and roughly A^{-1} , where A is the opamp DC gain.

While the presence of error terms in the output of the proposed modulator pose a possible limitation on the achievable SNR, these errors can be reduced to levels below that required to obtain the SNR in any given design, without precision components. The

simplest approach is to increase the gain of the opamp, for example, by gain-boosting techniques [21] or using a suitable technology that enables high gain, for example, using smaller line widths. The effect of leakage errors can be reduced by either circuit or system level solutions. Circuit techniques involve the use of gain compensated switch-capacitor integrators that make α and β proportional to the inverse of the square of the opamp DC gain A instead of being proportional inversely to A [30,31]. System level techniques like digital error calibration are the topic of current research [32, 33, 34] and can be undertaken as future study with respect to the proposed system.

5.4.2 Pipelined Multibit Converter Nonidealities

The sources of errors in pipelined converters are discussed in section 2.2.2. The ideal threshold of 0 V is replaced by a random voltage whose absolute value is less than the threshold V_T . Each stage has an independent threshold, which has an uniform probability distribution in $\pm V_T$. This threshold is held constant for each simulation, but is generated at the beginning of every simulation. Similarly, the gain error is modeled to be a random variable within 1% of the nominal value of 2. Actually, capacitor ratio error and low opamp gain contribute to the gain error. Capacitor ratios can be obtained to 0.1% accuracy [16]. Opamp gain is usually sufficiently high for the error to be ignored, but considered here to include the possibility of using a conventional low-gain high-slew rate opamp used in sigma-delta modulators. It is estimated that a maximum 1% variation in gain would be inclusive of these and other gain errors. If the outputs of some of the stages are overranged, the opamp saturation will limit these excursions. The saturation limits are taken to be ± 3 V. While this type of model with random values will require statistical techniques to predict the performance within a confidence limit, the approach here has been to use example simulations to estimate the loss in performance from ideal due to the nonidealities.

5 4.3 Effect of Nonidealities

The system is modeled taking into account the non-idealities associated with the integrator and the pipelined multibit analog-to-digital converter. The primary source of error in the integrator is the gain of the opamp which typically will be in the order of 1000 to 10,000 (60 to 80 dB), while in the present implementation, it is expected to be around 300 (50 dB). The primary source of error in the pipeline analog-to-digital converter, in the present implementation, is the comparator thresholds, which is of the order of 0.4 V and could be an order less for more refined implementations. Comparison of the simulation results that incorporate these non-idealities with the experimental results is shown in Table 5.2. The simulated and experimental conditions corresponded to a 1 V peak-to-peak input at 1000 Hz, baseband of 8 KHz, oversampling ratio of 8, opamp saturation at ± 3 V, modulator ADC levels ± 1.5 V, and a pipeline reference of 2.5 V. It can be seen that while non-idealities are the reason for the degraded performance of the modulator, the feasibility of the improved performance of the proposed system is confirmed.

The requirements on the opamp gain and tolerance on the comparator offsets to achieve close to ideal performance can be estimated by simulations. Keeping the comparator thresholds ideally at zero and varying the opamp gain resulted in the graph

Table 5.2. Comparison of Experimental and Non-ideal Simulation results.

System tested	Opamp Gain	Max.ADC Threshold variation (V)	STNR at Y_1 1 st order modulator	STNR at Y_1' 1 st stage	STNR at Y 2 nd stage
Simulation:					
Ideal	250,000	0	28	40	68
Non-ideal opamp	250	0	24	41	58
Non-ideal ADC	250,000	1	28	36	36
Both non-ideal	250	1	24	30	30
Experiment:					
			28	42	49
			29	43	49

Figure 5.4. Variation of System STNR with Opamp Gain. Comparators are assumed to be ideal.

shown in Figure 5.4 for oversampling ratios of 8 and 128. For low oversampling ratios, opamp gain above 60 dB is adequate to achieve close to ideal results. However, gain greater than 80 dB is required if high oversampling ratios are used. Such gain can be achieved in currently available technologies, while meeting the needs of slew-rate and settling.

Similar simulation with opamp gain greater than 100 dB and the comparator offsets randomly selected to be within V_T yields the graph shown in Figure 5.5, for one example run. At low oversampling ratios, the comparator offsets play an important part in determining the total STNR obtained from the system. However, offsets that are in the range of few tens of millivolts are not detrimental to the system performance. Such offsets are typically obtained in current technologies, and no correction algorithm is needed as in the case with pipelined converters. The comparator offsets can be seen to have little effect at high oversampling ratios as was predicted, since the errors that are introduced in the multibit converters are noise-shaped and consequently attenuated.

The choice of specifications for the building blocks is thus dependent on the specific design targets on required signal resolution and bandwidth. In general, if the system is used to convert signals with large bandwidth, then a small oversampling ratio can be used. In such circumstances, the tolerance on comparator offset is more important than the opamp gain, which can be traded to increased slew-rate and consequently a

Figure 5.5. Variation of System STNR with Comparator Offset V_T . Opamp gain greater than 100 dB is assumed.

shorter settling time for the opamp. Achieving the tolerance specification of few tens of millivolts on the comparator offset is not a constraint, which implies that the system can achieve high resolution at low oversampling ratios.

A design typically consists of the identification of the order of the noise-shaping function L , number of bits in the multibit quantizer N and the number of stages M in the system, given the signal bandwidth and required resolution. The required building block specifications then need to be determined from system simulation, for each topological variation will result in a different sensitivity of resolution to nonidealities. For example, a second-order modulator in the first-stage noise shapes the nonidealities of the multibit quantizer in the first stage by second-order and consequently reduces its effect in comparison to a first-order modulator in the first stage. Circuits that meet the specifications are then used to implement the system.

CHAPTER 6

CONCLUSIONS

Pipelined sigma delta modulators with interstage scaling have been proposed to achieve high resolution at high frequencies by reducing the noise power in the entire spectrum and not only in the baseband. The use of multibit quantizers external to the single-bit $\Sigma\Delta$ loop is the key to effectively incorporate interstage scaling in the pipeline of $\Sigma\Delta$ loops. Reduced quantization noise in the baseband allows the use of lower oversampling ratios, for a given resolution, compared to traditional $\Sigma\Delta$ modulator architectures. Stability problems associated with higher-order $\Sigma\Delta$ modulators that achieve high resolution are absent in the proposed architecture. The use of single-bit feedback $\Sigma\Delta$ loops does not require the high precision components used in multibit digital-to-analog converters. Due to the reduction of high-frequency noise, contrary to the traditional $\Sigma\Delta$ modulator architectures where the high-frequency noise is amplified, further reduction in digital circuit complexity and power is possible.

This proposed system has been implemented as an integrated circuit in 2 micron CMOS technology using switched-capacitor circuits. A robust design procedure for fully-differential folded-cascode opamps that does not involve extensive use of process parameters is presented. Two chips have been fabricated, one to test the functionality of the opamps and comparators and the other implements the proposed system. Testing of these chips proved the functionality of the components as well as the entire system. Measurement results confirm the practicability of achieving improved performance from the proposed system, as predicted.

Nonidealities in the implementation limit the performance obtained. Two important sources of errors, the integrator leakage and pipelined converter nonlinearity, which are directly related to the opamp gain and comparator thresholds, have been explored. The requirements on these building blocks to achieve close to ideal system performance is shown to be practically implementable, validating the usefulness of the system.

The implemented system is the simplest topology that implements the concept of interstage scaling in multibit sigma-delta modulators. Future work could apply the same principle to other sigma-delta topologies that make use of multibit modulators. The reduction of the effects of nonidealities mentioned above is a subject of ongoing research. The proposed system will greatly benefit from the results of such research, extending the capabilities of both the sigma-delta as well as the pipelined converters.

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