SMART UTILITY INTERFACE FOR PHOTOVOLTAIC CONVERTERS

by

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TABLE OF CONTENTS

ACKNOWLEDGEMENTS	ii
ABSTRACT	iv
LIST OF FIGURES	v
CHAPTER	
I. INTRODUCTION	1
II. PHOTOVOLTAIC CHARACTERISTICS	10
III. POWER TRACKING BOARD	30
IV. MULTI-LEVEL H-BRIDGE INVERTER	42
V. MICROCONTROLLER: THE HARDWARE INTERFACE	51
VI. UTILITY DETECTION	59
VII. CONCLUSIONS	63
REFERENCES	65
APPENDIX: COMPONENT RATINGS	67

ABSTRACT

The main objective of this project is to develop an intelligent, compact power-conditioning module that can be directly interfaced to PV converters and the utility grid. This inverter will be incorporate smart control electronics that will synchronize to the utility voltage. Additionally, this technology will use power tracking to extract the optimum power from the solar panels. This will involve developing software algorithms to extrapolate the maximum amount of power from the PV arrays under changing solar intensity. Data obtained will show that the DC voltage of an array initially drops only slightly, when loaded but after passing the maximum power point, decreases rapidly.

LIST OF FIGURES

1. Project Diagram.....	2
2. Declination, δ , versus Day of Year.....	3
3. Azimuth as a Function of Hour and Day.....	5
4. Elevation as a Function of Hour and Day.....	6
5. Pictorial Description of Azimuth and Elevation Angle.....	7
6. Time Correction versus Day of Year for Lubbock, New York, and Honolulu	8
7. Approximate Sunset, Sunrise, and Length of Day versus Day of Year.....	9
8. Periodic Table	10
9. Intrinsic Fermi Level of (a) Undoped Material, (b) p-type Material, (c) n-type Material	12
10. P-N Junction	13
11. P-N Junction, Contact Potential, and Energy Levels	13
12. Photoelectric Effect and Graph of Equation 10	15
13. Photovoltaic Effect	16
14. Fill Factor	17
15. Solar Panel, 300 W Light Bulb, Variable Power Supply	18
16. Components and Construction of a Generic Solar Panel ⁶	19
17. Chroma 6310 Programmable DC Electronic Load	21
18. Front Panel of LabVIEW Controller	23
19. First Portion of LabVIEW Diagram	24
20. Second Portion of LabVIEW Diagram	24

21. Current versus Voltage of Solar Panel @ 754 Lux	26
22. Power versus Current of Solar Panel @ 754 Lux	26
23. Current versus Voltage of Solar Panel @ 1798 Lux	27
24. Power versus Current of Solar Panel @ 1798 Lux	27
25. Current versus Voltage of Solar Panel @ 8050 Lux	28
26. Power versus Current of Solar Panel @ 8050 Lux	29
27. The Hall Effect	31
28. Open Loop Current Sensor Used in Project; a) Picture, b) Schematic	32
29. Multiplying Effect of Hall Sensor	33
30. Operational Output of Hall Sensor	34
31. Circuit Schematic of Power Tracking Board	35
32. Theoretical Output Range for Power Tracking Board	36
33. Component Layout of Power Tracking Board	37
34. Constructed Power Tracking Board	38
35. Operational Output of Power Tracking Board	39
36. Voltage Output of Solar Panel at Varying Currents versus Voltage Output of Power Tracking Board, Simulated Data (Blue Lines) and Experimental Data (Multi-colored Lines)	40
37. Performance of Power Tracking Board (Collected on the Roof of the Electrical Engineering Building, TTU)	41
38. Single-Phase Full Bridge Inverter	42
39. Two-Level, 3-Phase Inverter	43
40. Output of Two-Level, 3-Phase Inverter	44
41. Multi-Level Inverter Concept	45

42. Output of Multi-Level Concept	46
43. Full-Bridge Multi-Level Inverter Concept	47
44. Output of Full-Bridge Multi-Level Inverter	48
45. Schematic of PCB Layout for Power Converter	49
46. Layout of Inverter, Microcontroller, and Utility Detection Circuitry	50
47. HC12 Module Used for Processor	51
48. 9S12 Processor Module	52
49. Schematic of an Opto-isolator	53
50. Switching Frequency and Sinusoid Used to Generate PWM	54
51. SPWM ₁ Signal Generated Using Sin(t)	55
52. SPWM ₂ Signal Generated Using -Sin(t)	56
53. Resulting PWM Signal and Desired Sinusoidal Frequency	56
54. Schematic of Utility Amplitude Detection Circuit	60
55. Simulated Output of Utility Amplitude Detection Circuit	60
56. Schematic of Utility Phase Detection Circuit	61
57. Simulated Output of Utility Phase Detection Circuit	62

CHAPTER I

INTRODUCTION

In 1996, worldwide energy consumption reached 375.07 quads annually, with 29% of that energy being used by North America.¹ The USA has the highest per capita energy usage in the world, and as most consumers notice, when energy needs increase so does the cost. Photo-voltaics (PVs) have recently gained a lot of attention as a practical and accessible way to offset increasing energy costs for the consumer public. Whereas solar panels were previously reserved for industrial and academic applications, they are now cheap enough to be utilized in household applications. Under the Public Utilities Regulatory Policies Act of 1978 (PURPA), utility companies are required to buy back power from owners of PV systems.² Powering an entire household solely with PVs, however, would be difficult to implement due to the extensive number of panels required. Additionally, since solar panels are useless without light, the elaborate storage system needed to store power for nighttime use would be expensive and voluminous. However, using PVs to supplement the utility proves to be convenient energy management. This application should be completely automatic and indistinguishable to the consumer.

The purpose of this paper is to discuss the methods and techniques used in creating a compact intelligent power conditioning module that can be used to interface photovoltaic converters to the utility grid. Currently, utility-connected, power tracking inverters exist. This project proposes a novel method of sensing the maximum power point and also includes an inverter design to improve the signal being fed back to the

utility. One of the goals of this project was to develop a compact device that conformed to the IEEE Standard 929 and the *NEC* (National Electric Code). Another goal was to realize a strategy for accomplishing the above while consuming minimal power. Figure 1 below is a diagram of how this interface will work. After power is generated by the solar panels, it is measured by the power-tracking board. The DC power is then converted to AC power by the inverter. The inverter synchronizes its output to the utility. If the two are perfectly in synch no power is exchanged but, real power can be injected to the utility by advancing the phase of the converter's phase in relation to the utility's phase. Likewise, reactive power can be injected into the utility by increasing the magnitude of the converter voltage. Both real and reactive powers are exchanged with large deviations in phase and magnitude and the power components are affected by any changes.³

Figure 1: Project Diagram

Solar Tracking

Being able to calculate the path the sun will take over a solar panel is useful in order to approximate the amount of sunlight that will be reaching the panel. It is also useful in determining the tilt of the panel. This can be crucial if a solar panel is essentially

stationary. Determining the angle is a function of the sun's path and also the consumer's energy needs. The earth revolves around the sun in an elliptical orbit with the sun at one of the foci. However, there is only about a 2% difference between the maximum and minimum distances so the mean distance of $1.5 \cdot 10^{11}$ m is often used in calculations.¹

In order to calculate the sun's approximate path, one must first find the declination, δ . For purposes of this paper, the point of reference will be Lubbock, TX. The declination is the angle of deviation of the sun from directly above the equator. A value for δ is generated by Equation 1, where d is the day of the year from January 1st.

$$\delta(d) := 23.45 \text{ deg} \cdot \sin \left[\left(\frac{360}{365} \right) \cdot (d - 81) \cdot \text{deg} \right] \quad \text{Eq. (1)}$$

Figure 2 below graphs the value of δ versus the day of the year. Positive angles are considered north of the equator and negative angles are considered south of the equator. These results are only approximate, however, since the year is not exactly 365 days long.

Figure 2: Declination, δ , versus Day of Year

The declination is related to the zenith angle by Equation 2, where θ_z is the zenith angle and ϕ is the latitude of the location of interest. The zenith is simply a line that is perpendicular to the earth's surface and the zenith angle represents the angle between the zenith and the sun.¹ The term solar noon refers to the moment when the sun is directly overhead; this can be determined by how the shadow of an object falls on a sunny day. If the shadow lies directly north in the northern hemisphere, or to the south in the southern hemisphere, then that informs the observer that the sun has reached the highest point in the sky.

$$\theta_z = \phi - \delta \quad \text{Eq. (2)}$$

There are several other terms which must be defined before continuing. The azimuth angle, Ψ , is the angle between the south and the projection of the sun-earth line in the horizontal plane.⁴ Figure 3 below depicts the changing azimuth angle of the sun, with respect to Lubbock, each day throughout the year. The z-axis shows the fluctuations of the azimuth and the azimuth is measured in radians in the graph.

Figure 3: Azimuth as a Function of Hour and Day

The altitude angle, also known as the solar altitude or the elevation angle, is the angle between the horizontal plane and the line from the observer to the sun. Figure 4 below graphs the elevation angle of the sun over a twenty-four hour period throughout the year. The elevation is measured on the z-axis. The elevation angle is a function of inverse sine, so modulates between -1 and 1. Neither graphs in Figures 3 or 4 are entirely accurate as a year is not exactly 365 days, and some years are 366 days long!

Figure 4: Elevation as a Function of Hour and Day

Figure 5 below is a pictorial representation of the azimuth and elevation angles. The horizontal plane is denoted by the circle and the blue arrow indicates the north direction. The projection of the sun-earth line in the horizontal plane and the line perpendicular to the horizontal plane to the sun form a right angle. The line from the observer to the sun's position forms the hypotenuse of the triangle. The line pointing opposite the north direction is the line indicates the south and is used to determine the azimuth angle.

Figure 5: Pictorial Description of Azimuth and Elevation Angle

Not only is it important to consider the sun's position but, when engineering a PV system, the designer needs to know sunrise and sunset times as well to approximate the length of days. This is necessary in order to correctly size the system to fit a consumer's needs. As an example, a customer wants to primarily offset the expensive cost of cooling in the summer. A designer must take in to consideration how much offset the customer desires in conjunction with how much the consumer wishes to invest in solar panels. The power generated by the panels throughout a particular day is also necessary for this sizing function. To calculate sunrise and sunset times, the time correction (TC) must first be found. This item is a function of the equation of time (EoT), which is a function of the eccentricity of the earth's orbit and tilt, as well as, the longitude of the location of interest. The equations for TC and EoT are given in Equations 3 and 5, respectively, where $Long_{LBK}$ is the longitude of Lubbock, TX at -101.82 deg and d is the number of the day from January 1st.⁵ Figure 6 is a graph of the TC for Lubbock, TX. Also shown, for

the purposes of comparison, are the time corrections for New York City (TC_{NY}) and Honolulu, Hawaii (TC_{HI}). The longitude for the comparison locations are -74.01170 deg and -157.93 deg, respectively.

$$EoT(d) := 9.87 \sin(2 \cdot \beta(d)) - 7.53 \cos(\beta(d)) - 1.5 \sin(\beta(d)), \quad \text{Eq. (3)}$$

$$\text{where } \beta(d) := \left(\frac{360}{365} \right) \cdot (d - 81) \cdot \text{deg} \quad \text{Eq. (4)}$$

$$TC(d) := \frac{[4(-90 \text{ deg} - \text{Long}_{LBK}) + EoT(d)]}{60} \cdot \text{min} \quad \text{Eq. (5)}$$

Figure 6: Time Correction versus Day of Year for Lubbock, New York, and Honolulu

When the results from Equations 3 and 5 are plugged into Equations 6 and 7, it yields the results which are graphed below in Figure 7. Lat_{LBK} is the Latitude of Lubbock,

TX, which is 33.65 deg. The length of the day is simply graphed as the difference between the sunset and the sunrise.

$$\text{Sunrise}(d) := 12 - \left(\frac{1}{15\text{-deg}} \right) \cdot \text{acos} \left[\frac{(-\sin(\text{Lat}_{\text{LBK}}) \cdot \sin(\delta(d)))}{\cos(\text{Lat}_{\text{LBK}}) \cdot \cos(\delta(d))} \right] - \frac{\text{TC}(d)}{60} \quad \text{Eq. (6)}$$

$$\text{Sunset}(d) := 12 + \left(\frac{1}{15\text{-deg}} \right) \cdot \text{acos} \left[\frac{(-\sin(\text{Lat}_{\text{LBK}}) \cdot \sin(\delta(d)))}{\cos(\text{Lat}_{\text{LBK}}) \cdot \cos(\delta(d))} \right] - \frac{\text{TC}(d)}{60} \quad \text{Eq. (7)}$$

Figure 7: Approximate Sunset, Sunrise, and Length of Day versus Day of Year

solar cells, the properties of Si are modified by doping the material, or adding impurities. Dopants, or added impurities, either create more holes, which is an empty state in the valence band, or electrons, in the silicon.⁷ This results in two kinds of doped semiconductor materials, n-type which is predominantly electrons, and p-type which is mostly holes. Donor atoms are used to create an n-type material. These are atoms which donate electrons to the conduction band of the Si lattice. Conversely, acceptor atoms are used to manufacture p-type semiconductors, and these atoms accept electrons from the valence band, thus creating holes in the valence band.⁷ Elements in column 13 from the Figure 8 above are considered acceptor atoms in germanium (Ge) and Si, and column 15 is considered donor atoms.

Electrons in solid materials follow the Fermi-Dirac distribution function in Equation 8. This equation determines the probability that an electron will occupy an energy state at absolute temperature, T. E_F is the Fermi level of the material and k is Boltzmann's constant.⁷

$$f(E) = \frac{1}{1 + e^{\frac{(E-E_F)}{k \cdot T}}} \quad \text{Eq. (8)}$$

Doping a semiconductor will alter its intrinsic Fermi level (Figure 9a). The addition of an acceptor dopant causes the Fermi level to shift towards the valence band (Figure 9b) whereas; creating an n-type semiconductor shifts the Fermi level towards the conduction band (Figure 9c).

Figure 9: Intrinsic Fermi Level of (a) Undoped Material, (b) p-type Material, (c) n-type Material

Junction Physics

One single solar cell is composed of a p-n junction. Imagine having two separate pieces of semiconductor material, as shown in Figure 10, one piece being n-type the other p-type. Then, combine the two pieces into one. This is a p-n junction; the contact between the two different pieces of semiconductor material completely alters the dynamics and characteristics of the two pieces.

Figure 10: P-N Junction

The joining of the n-type and p-type creates a contact potential, V_o , and a resulting electric field from the n material to the p material. This potential is due to the fact that the two shifted Fermi levels of the n and p materials must connect, as depicted in Figure 11.

Figure 11: P-N Junction, Contact Potential, and Energy Levels

This creates the graded connection with the potential of qV_o , which is the difference in the energy of the p-type and n-type energy bands. The energy grade corresponds to the transition region, also known as the depletion region, specified by the W above. V_o , by definition, is an equilibrium quantity and no resulting net current can be attributed to it. The value of V_o is related to the concentration of dopants on either side and is shown below in Equation 9. It will play a large role in the effectiveness of a PV cell. N_a represents the acceptors/cm³ in the p-type material and N_d is the donors/cm³ in the n-type material, n_i is the intrinsic carrier concentration ($n_i=1.5*10^{10}$), k is Boltzmann's constant ($k=8.62*10^{-5}$ eV/K= $1.38*10^{-23}$ J/K), T is absolute temperature, and q is the charge of one electron ($q=1.6*10^{-19}$ eV).⁷

$$V_o = \left(k \cdot \frac{T}{q} \right) \cdot \ln \left(N_a \cdot \frac{N_d}{n_i^2} \right) \quad \text{Eq. (9)}$$

Photovoltaic Effect

In order to explain the photoelectric effect, several terms must first be explained. First, there exist discrete units of energy called quanta. It was discovered by Planck when he observed that radiation was emitted from heated samples, and the energy levels of these quanta were $h\nu$, where ν is the frequency and h is Planck's constant ($h=6.63*10^{-34}$ Js). If monochromatic light is projected onto a flat metal surface, and some of the electrons receive enough energy from the light to “jump” from the metal surface to the surrounding vacuum, this is known as the photoelectric effect and is described by

Equation 10. The unit of energy, $q\Phi$, is known as the work function, where q is the magnitude of the electronic charge. The term Φ is reported in volts but, it is simply a characteristic of the metal used.

$$E_m = h\nu - q\Phi \quad \text{Eq. (10)}$$

The above equation represents the energy gained from the incident light and the energy lost from its “jump” from the metal to vacuum. A plot of the maximum energy of the electrons leaving the metal surface versus the frequency yields a line with a positive slope h (Figure 12).⁷

Figure 12: Photoelectric Effect and Graph of Equation 10

The photoelectric effect this project is most concerned with is the photovoltaic effect, which is when a forward voltage appears across an illuminated junction. Figure 13 illustrates this phenomenon. This effect causes electron-hole pairs to be generated in the semiconductor p-n junction region. As shown, power is delivered to the external load

because the junction voltage is positive and the current is negative. However, the generation of power by this technique is limited. The junction voltage is limited to values less than the contact potential, V_o , which is also less than the band gap voltage E_g/q . Additionally, the current is dependent on the amount of area illuminated. An area of 1 cm^2 will typically generate currents that are in the range of 10-100 mA.⁷ Though, arrays of these junctions have the capability of powering space satellites, to supplement the utility for residential and commercial buildings, and in some unique cases, entirely power a home.

Figure 13: Photovoltaic Effect

Many compromises are made in the construction of a solar cell. For instance, a large contact potential is attractive for the reasons stated above, but long carrier lifetimes are also desirable. The problem is that a large contact potential is obtained by heavy doping which also diminishes lifetimes.⁷ Like batteries, PVs can be hooked up either to

increase the current of voltage. If two or more panels are connected in series, this will generate a higher output voltage; if they are placed in a parallel connection that will increase the output current.

Solar Panels

Currently, a well-made Si solar panel has about 10% efficiency and can provide about 100 Watts of power per square meter. The PVs used in this project were manufactured by Chronar. These solar panels have a maximum open circuit voltage, V_{oc} , of 22 V and a maximum short circuit current, I_{sc} , of 1.1 A. In order to calculate the fill factor, which is the ratio $I_m V_m / I_{sc} V_{oc}$, V_m and I_m must also be determined. These values are found from the maximum power delivered to a load by a solar cell. The fill factor is a characteristic of a solar array and identifies its quality.¹ An illustrative description of the term is below in Figure 14.

Figure 14: Fill Factor

Figure 15 is a picture of one of the Chronar solar arrays utilized in this project. This picture depicts the experimental set-up when testing the characteristics of the solar panels. The results from these tests will be discussed later in the paper.

Figure 15: Solar Panel, 300 W Light Bulb, Variable Power Supply

Shown in the picture is the 300 W light bulb, which was used to illuminate the solar panel. The intensity of this light bulb was controlled by a variable power supply. This light bulb had a range up to 8050 Lux.

All solar cells contain the same basic components. The most crucial is the semiconductor layer, as described earlier, because this is where the current is generated when exposed to sunlight. This is also where most PV arrays differ; there are many different materials used for this layer. On top of the semiconductor layer is a metallic grid and on the bottom a metal contact; this is where the electrons are collected to power a load connected to the array. Figure 16 is a picture of a generic solar cell. The panels are also covered with a protective transparent material, usually glass, and then coated with an antireflective substance to keep light from reflecting off the panel, thus improving its performance.² This antireflective material acts as an impedance inverter and is often referred to as a quarter-wave impedance transformer. Two dielectric materials, the glass covering and the n-type semiconductor, have intrinsic impedances, η_a and η_c , where η_a and η_c are not equal. A third material must be placed between them in order to prevent reflections at the boundary planes. The intrinsic impedance of this third material, η_b , is found using Equation 11. The required thickness of this material, d , is determined by Equation 12, where λ is the wavelength to be transmitted.⁸

$$\eta_b = \sqrt{(\eta_a \cdot \eta_c)} \quad \text{Eq. (11)}$$

$$d = (2 \cdot n + 1) \cdot \frac{\lambda}{4}, \quad \text{Eq. (12)}$$

where $n = 0, 1, 2, \dots$

Figure 16: Components and Construction of a Generic Solar Panel⁶

The Chronar solar panels are made from cells of amorphous silicon (a-Si) that were invented in the 1970s. Amorphous silicon is further divided into multi-junction and single-junction panels. Single-junction panels usually have about a 2% to 4% efficiency rating, which is what is used in this project, whereas crystalline silicon panels can reach efficiencies of 17%. This means that if there is 1 kW of energy available in 1m² of sunlight, then this a-Si array can only extract 200 W to 400 W of that available power. Also, most a-Si panels lose approximately 25% of their power output during the initial few months of use, after which, the performance stabilizes at a constant level. This final "stabilized" performance is supposed to equal the manufacturer's "rated" performance; so, a 15 W panel should start out at about 20 W new, dropping to 15 W after the first few months of use.⁹

DC Electronic Load

The Chroma 6310 programmable DC electronic load is shown below in Figure 17. The 6310 is actually a mainframe that controls two 63103 and two 63105 modules. These modules contain the electronics, which actually provide the load and also sense the voltage and current measurements. The difference between the two modules is the power, current and voltage ratings. I used the 63105 module because the lower ratings yielded better resolution in my measurements. It is rated for up to 1 amp (A) at 30 watts (W) of power or 10 A at 300 W. It has a voltage range of 2.5 to 500 volts (V). Its resistive range varies from 1.25Ω to $5k\Omega$. When setting a load, voltage or current value, it has an accuracy of 0.1%; also, when measuring a value, it has an accuracy of 0.1%.¹⁰

Figure 17: Chroma 6310 Programmable DC Electronic Load

The solar panel is connected to the load at the module's sensing connections. The rear of the instrument has an RS-232 connector that was used to interface the instrument

to a computer. The load has three modes of operation: constant current, constant resistance, and constant voltage. Within each of those modes are variations of that mode. For instance, if constant current is the desired mode, the user would have to select from static constant current low range, static constant current high range, dynamic constant current low range, or dynamic constant current high range.⁴ The controller for this project used only constant resistance low. This was chosen because a LabVIEW function block was found on the Chroma website which could control the instrument in that mode. This simplified the process of designing the controller significantly.

LabVIEW Controller

The LabVIEW controller was interfaced from the computer to the DC electronic load via an RS-232 serial port. A null modem was required for the computer and instrument to talk. A null modem switches the transmit and receive pins of the RS-232 so that the Transmit Data of the computer is connected to the Receive Data of the instrument and vice versa. If this is not used, then the computer will just be sending commands to itself and no handshaking or communication will take place.

The algorithm for the controller is fairly simple. The user selects which of the computer's communication ports to access, which channel of the load to control, and the slew rate of the current. The user also decides which mode to operate the electronic load and must also determine the name of the file where the data will be sent after it is all collected. Figure 18 is a picture of the front panel where the user inputs their selections.

Figure 18: Front Panel of LabVIEW Controller

Once the program begins, a VISA (Virtual Instrument System Architecture) session is opened and the instrument is initialized. The channel and slew rates are then set and the controller enters a “for-loop.” Figure 19 is a picture of the first portion of the LabVIEW diagram. This “for-loop” increments the resistance of the load from 0Ω to $5k\Omega$ in steps of 25Ω . For each increment a current and voltage measurement is taken and sent to a Build Array block.

Figure 19: First Portion of LabVIEW Diagram

This last part of the LabVIEW code is shown in Figure 20. Once the program exits the loop, the array is sent to a spreadsheet file. The instrument is then put back into local mode and the VISA session is closed.

Figure 20: Second Portion of LabVIEW Diagram

One problem encountered was that the computer could never make a real measurement for the first characteristic measured. For instance, after the resistance was set, if the current was measured first, the computer was not able to make a valid current measurement; the same thing occurred with the voltage. To overcome this in the sequence, several more frames were added. These frames asked the instrument for a voltage measurement; knowing that no real value would be given, that information was sent to a junk buffer, then the valid voltage and current measurements were obtained.

Graphs

This section contains the voltage-current and power-current graphs obtained from the experimental setup. This first graph, Figure 21, was generated at an intensity of 754 Lux. It shows the current versus voltage relationship of the panel at that intensity and also the power and current relationship in Figure 22. Figure 22 shows the maximum power point position circled. The maximum power point position refers to the point on the P-I (power versus current) graph where the power peaks before sharply flagging. This position corresponds to the “knee” in V-I (voltage versus current) graph. Solar panels have a limiting voltage and a limiting current, as depicted in the V-I graphs. The “knee” position is the point between the limiting current and limiting voltage where the panel generates the most power.

Figure 21: Current versus Voltage of Solar Panel @ 754 Lux

Figure 22: Power versus Current of Solar Panel @ 754 Lux

These next two graphs, Figures 23 and 24 are the current-voltage and power-current relationships at 1798 Lux; again the maximum power point is circled on the graph.

Figure 23: Current versus Voltage of Solar Panel @ 1798 Lux

Figure 24: Power versus Current of Solar Panel @ 1798 Lux

The last two graphs included, Figures 25 and 26 are the V-I relationship and the P-I relationship of the solar array at 8050 Lux, respectively. Again, the maximum power point position is circled in Figure 26.

Figure 25: Current versus Voltage of Solar Panel @ 8050 Lux

Figure 26: Power versus Current of Solar Panel @ 8050 Lux

Light Meter

The light meter used to determine the light intensity being exposed to the panels is an Extech model 407026 heavy-duty light meter. It can measure up to 50,000 Lux or 5000 Foot-Candles (Fc) with 4% accuracy. The user can choose what type of light source the meter is exposed to, such as daylight (tungsten), fluorescent, sodium, or mercury. The light meter also has a relative % mode feature. When the % button is pushed, that particular intensity is set as 100% and everything else is measured relative to that. Also, the instrument has an RS-232 serial port so that it can be interfaced and controlled with a computer.

CHAPTER III

POWER TRACKING BOARD

In order to find the maximum operational point of a solar panel, it is necessary to know the power output of the solar panel. To do this, a power tracking board was constructed; this board measures the output of the solar cell using the multiplying effect of the Hall sensor, which generates a Hall voltage directly proportional to the power.

The Hall Effect

The Hall effect was discovered, in 1879, by a scientist named Edwin Hall. He noticed that when a current carrying conductor was placed in a magnetic field, a voltage was generated in a direction that was perpendicular to both fields. Also known as a Hall voltage, this is the result of the deflection of charge carriers due to the magnetic field. This phenomenon can be used to determine whether a material is p-type or n-type and as well as the density of the carriers.¹¹

In Figure 27, the bar is a p-type bar. In this picture the magnetic field is being applied in the z-direction, which deflects the holes. Equation 13 below expresses the total force on a hole due to the magnetic and electric fields, where E is the electric field, v is the velocity of the carriers, B is the magnetic field and q is the carrier charge.

$$F = q(E + v \times B) \quad \text{Eq. (13)}$$

Figure 27: The Hall Effect

In order to maintain the flow of holes down the bar, an electric field E_y must form which is equal to $v_x B_z$. This will make the net force experienced by the holes equal to zero.

So, if in the y-direction $F_y = q(E_y - v_x B_z)$ Eq. (14)

and $E_y = v_x B_z$ Eq. (15)

then, $F_y = 0$ Eq. (16)

This is the Hall effect and the Hall Voltage is determined by the electric field formed and the width of the bar as shown in Equation 17.⁷

$$V_H = E_y w$$
 Eq. (17)

The hall voltage can also be expressed in terms of the Hall coefficient below.

$$R_H = 1/nq$$
 Eq. (18)

In the previous relationship, n is the concentration of carriers and q is the associated charge, + for holes and – for electrons.

$$V_H = IB/R_H t$$

Eq. (19)

Figures 28a and 28b below depict the actual open loop current sensor used in the project, the NA-25. It is manufactured by F.W. Bell and is a low cost, low power consumption model. The open loop current sensor is basically a Hall sensor that is placed in the air gap of a magnetic core. The current carrying conductor that passes through the aperture generates a proportional magnetic field, B , experienced by the Hall sensor. The conductor used in the project but, not shown in Figure 28a is an aluminum wire that is passed through 25 times. This was done to ensure that the entire output range of the sensor was utilized. The sensor can sustain up to 25A of aperture current and the solar panel generates only 1A. V_x is the excitation voltage and V_H is the hall voltage generated.

Figure 18: Open Loop Current Sensor Used in Project; (a) Picture (b) Schematic

In the case of this project, the multiplying effect of a Hall sensor is utilized in order to derive a Hall voltage output proportional to the power generated by the solar panel. The velocity of the holes is proportional to the excitation voltage, and the magnetic field is proportional to the aperture current. This can be seen more clearly in the circuit schematic below in Figure 29. The excitation voltage is derived from a voltage divide to generate a voltage proportional to the load voltage generated by the solar panel.

Figure 29: Multiplying Effect of Hall Sensor

This was necessary in order to adhere to the specifications of the open loop current sensor used in the project. The load current is sent directly through the aperture and looped through twenty-five times. As mentioned, this was done in order to exploit the

entire output range of the open loop current sensor. The wire must be wrapped tightly around the magnetic core because the induced magnetic field is inversely proportional to the distance from the current. If the wire is loose and there is distance between the wire and the core, this will weaken the induced magnetic field. This relationship is shown in Equation 20, where B is the magnetic field. N represents the number of turns of the wire, in this case 25, and I is the current. The term μ_0 is the permeability of free space ($\mu_0 = 4\pi \cdot 10^{-7} \text{ N/A}^2$), and r is the mean radius of the magnetic core.⁸

$$B = \frac{\mu_0 \cdot N \cdot I}{2 \cdot \pi \cdot r} \quad \text{Eq. (20)}$$

Figure 30 below shows the operational output of the Hall sensor. The input power and Hall voltage have a linear relationship with a slight offset from the zero crossing.

Figure 30: Operational Output of Hall Sensor

The Operation of the Board

There is more to the power tracking board than just the Hall sensor. The information from the board will be sent to a microcontroller which will tie the hardware together and control the power converter. The output of the sensor is far below what a microcontroller can detect so an operational amplifier (op-amp) is required to amplify the Hall voltage to 0 volts (V) to 5 V, the voltage range acceptable to the microcontroller. The schematic below illustrates the circuit of the power tracking board, and Figure 31 is the simulated output of the board.

Figure 31: Circuit Schematic of Power Tracking Board

The op-amp used is a low cost and low power device. In our tests we used both the AD620 and the LT1920. Both have identical pin layouts and the only difference between the two is how to arrive at the value for the gain resistor. The inputs are

completely differential, which is necessary to amplify the Hall voltage. This device also has a convenient reference input which is used to compensate for the offset in the output.

There is an offset which results from the residual magnetization of the core of the Hall sensor. This flux increases when the core is energized and it appears as a constant current and it will cause a proportional power offset. However, using the TL082 op-amp to drive the reference of the AD620 essentially eliminates this problem. Figure 32 shows the simulated output for the schematic.

Figure 32: Theoretical Output Range for Power Tracking Board

Another important aspect of the board is the protection circuit implemented at the end. This circuit will protect the microcontroller from any voltages outside of its range. The diodes and resistors are used to create a voltage divider such that the board's output voltage never exceeds 5V or falls below 0V. The constructed board is pictured below (Figure 34).

Figure 34: Constructed Power Tracking Board

The graph of Figure 35 shows the operational output of the power tracking board. This data was collected in the lab using a power supply in place of the solar panel and using the Chroma electronic load to simulate household usage. The data was taken at various voltages over a current range of 0A to 1A. The output voltage is the amplified

Hall voltage. It is apparent that the relationship between the output and instantaneous power is linear, which compares to the simulated results. Additionally, we can note that the protection circuit works.

Figure 35: Operational Output of Power Tracking Board

Figure 36 on the next page is a comparison of the two graphs. They have been placed on top of one another and sized identically, for an accurate analogy. The blue lines are the simulated output from PSpice, and the multi-colored lines are experimental data. Figure 37 is data collected on the roof of the Electrical Engineering building. A solar panel was used as the power supply, an electronic load was used as the load, a power

supply was used to provide the 5V supply to the protection circuitry, and a voltmeter was used to collect the output. The performance of the amplified Hall voltage mimics that of the instantaneous power of the solar panel. The last little hump at the end of the graph is a characteristic of the solar panel which is imitated by the board.

Figure 36: Voltage Output of Solar Panel at Varying Currents versus Voltage Output of Power Tracking Board, Simulated Data (Blue Lines) and Experimental Data (Multi-colored Lines)

Figure 37: Performance of Power Tracking Board (Collected on the Roof of the Electrical Engineering Building, TTU)

CHAPTER IV

MULTI-LEVEL H-BRIDGE INVERTER

A solar cell produces direct current (DC) power. The utility and most household appliances operate on three phase alternating current (AC) power. A power converter is necessary in order to feed the power developed by the solar panel back into the utility. This power converter, called an inverter or a power conditioning unit (PCU), changes DC power into AC power. The design used in this project is a multi-level full-bridge converter. A standard single-phase full-bridge, or H-bridge, is shown in Figure 38. The full bridge design is attractive for this project because it allows for full control over phase, amplitude and frequency of the output. This is essential because in order to feed power back into the utility, the phase of the inverter's output must lead the utility's phase. Additionally, the amplitude must be adjusted to determine the amount of reactive power fed into the utility.

Figure 38: Single-Phase Full Bridge Inverter

Theory Behind Multi-Level Inverters

A normal two-level three phase inverter is shown below (Figure 39). The letters A, B, and C denote each phase of the circuit. The term two-level is used because its line to line voltage output has two levels, high and low, as in the top graph of Figure 40.

Figure 39: Two-Level, 3-Phase Inverter

The bottom graph shows the resulting sinusoidal AC currents of the three different phases. Each phase is separated by 120 degrees. The benefit of this is that the total sum of the power of the three legs equals zero, so no return line is necessary.

Figure 40: Output of Two-Level, 3-Phase Inverter

The purpose of using a multi-level inverter is to produce a better output of the inverter while reducing necessary filtering hardware. This technique produces the resulting sinusoidal wave in smaller steps. The advantage of this design is an AC wave of a higher power quality while maintaining low switching losses within the circuit. Figure 41 on the next page demonstrates a schematic of the multi-level concept and Figure 42 is the output of such a circuit. There are not just two levels of line-to line voltages anymore, now there are three, hence this is referred to as a three-level inverter. The top graph is the unfiltered output voltage of such a circuit. Compared to the top graph of Figure 40, the difference is very noticeable. The output of the three-level inverter has a much smoother sinusoidal shape, and no additional filtering was needed to accomplish this.

Full-Bridge Multi-Level Converter Concept with Uni-Polar Switching:

Figure 41: Multi-Level Inverter Concept

Figure 42: Output of Multi-Level Concept

It is possible to use more than three levels however; there is point of diminishing returns if additional hardware is taken into account.

Three-Phase, Three-Level Full Bridge Inverter

Below is a schematic (Figure 43) of the three-phase, three-level full bridge inverter. The design is uses the LMD18200 H-bridge chips. The graphs in Figure 44 show that the goal of a smoother output is accomplished.

Full-Bridge Multi-Level Converter Concept with Uni-Polar Switching:

Figure 43: Full-Bridge Multi-Level Inverter Concept

The top graph is the output current and the bottom graph is the output voltage.

Figure 44: Output of Full-Bridge Multi-Level Inverter

Each level is fed by an isolated DC-DC converter. The final output of the circuit is a series combination of the two full-bridges. The H-bridges used are the LMD18200 integrated H-bridge devices manufactured by National Semiconductor.

The LMD18200 is an H-bridge that can deliver up to 3A of continuous current and will operate at voltages of up to 55V. The DC-DC converters that supply the H-bridges will output a constant voltage on the DC bus. This simplifies the power tracking algorithm; the inverters will feed power back to the utility and meanwhile, the DC-DC converters will adjust to the varying voltage supplied by the solar panel operating at its optimum point. The PCB (printed circuit board) layout is shown in Figure 45, illustrating

the placement of the H-bridge chips. An interesting characteristic of the LMD18200 H-bridges is that they contain their own internal logic to generate a PWM signal. The transistors in the bridges are not accessible by the user. Figure 43 shows that two signals are sent to the chip, a PWM signal generated by the absolute value of a sine wave and a direction signal. The direction signal is simply a rectangular signal that modulates from 0 to 1. This signal is the red trace on the bottom graph of Figure 44. Also shown in this picture are the HCPL-2232 opto-isolators which provide electrical isolation between the microcontroller and the H-bridges. The layout of the board is shown in Figure 46. This picture shows the layout of the inverter located on the top part of the board, and also the placement of the microcontroller and utility detection circuitry, which will be discussed later in the paper, on the lower portion of the board.

Figure 45: Schematic of PCB Layout for Power Converter

Figure 46: Layout of Inverter, Microcontroller, and Utility Detection Circuitry

CHAPTER V

MICROCONTROLLER: THE HARDWARE INTERFACE

Motorola HC12 Microprocessor

A microcontroller module from the HC12 family will be used to tie the hardware together and accomplish the overall control. A microcontroller unit (MCU) is a computer containing a central processor unit (CPU), memory, and Input/Output (IO) capabilities on one chip. Since the utility voltage will already be present in order for synchronization, it will be used as the power supply for the MCU. The utility will be fed into an integrated AC-DC converter which will power the board with the necessary 5V. The processor which is manufactured by Axiom Manufacturing, is shown below in Figure 47.

Figure 47: HC12 Module Used for Processor

The processor is called the 9S12 personality module and has 256 kilobytes of Flash electrically erasable programmable read-only memory (EEPROM). EEPROM is useful because the memory can be reprogrammed. When initially ordered, each bit is preset, either all 1's or all 0's. The programmer then stores a fixed pattern of bit strings, called words, into the memory. This can be erased using an electric signal and reprogrammed as necessary. Additionally, this MCU possesses an abundance of IO (input/output) ports, analog-digital (AD) converters, several serial ports, and eight channels for producing pulse width modulation (PWM). The chip also sports a clock generator, hardware for a phase locked loop (PLL) clock multiplier, and reset hardware. The clock frequency can be set up to 24 MHz by the software using the PLL function.

The module is mounted with two sixty pin connectors. An interesting feature of this device is its portability and versatility. It is possible to unplug the module from the two mounts and connect it into a processor module shown in Figure 48, for debugging and code modifications. This allows for the board to be programmed externally.

Figure 48: 9S12 Processor Module

The code for this device is written in assembly language.

The processor's power supply is electrically isolated from all other components in the circuit using opto-isolators. Opto-isolators, also called optocouplers, are basic components used specifically to provide electrical isolation in a circuit. As shown in Figure 49, an opto-coupler consists of a light emitting diode (LED), on the left, and an output photo-transistor, on the right, in one package. An electric high signal causes the LED to emit light which is focused on the optically sensitive base of the photo-transistor.

Figure 49: Schematic of an Opto-isolator

This generates electron-hole pairs at the base of that transistor, thus turning it on. This provides complete electrical isolation, and reduces any electrical interference, between the input of the opto-isolator and its output.¹² The H-bridges for the DC-AC converter are driven by opto-isolators, in addition to the phase reference signals and over-temperature signals from the LMD18200 H-bridge devices are routed to the MCU via opto-isolators.

Pulse Width Modulation (PWM) With Uni-Polar Switching

In order to operate the transistors in the H-bridges to output a sinusoidal wave, a PWM signal must be generated by the MCU and sent to the hardware. This particular technique is referred to as sinusoidal PWM (SPWM). Figure 50 illustrates the concept behind an inverter generating a sinusoidal output with a controllable frequency and magnitude.

Figure 50: Switching Frequency and Sinusoid Used to Generate PWM

$\text{Sin}(t)$ and $-\text{Sin}(t)$ represents the control signal at the desired frequency and $\text{Triangle}(t)$ is the switching frequency of the inverter. $\text{Sin}(t)$ and $-\text{Sin}(t)$ are the separate control signals for two different legs of the inverter. Figure 51 shows $\text{Sin}(t)$, $\text{Triangle}(t)$, and the resulting SPWM signal in red, called SPWM_1 . When the magnitude of $\text{Sin}(t)$ is

greater than the magnitude of $\text{Triangle}(t)$, the SPWM_1 signal goes high, in this case 1. Vice versa, when the magnitude of $\text{Sin}(t)$ is less than the magnitude of $\text{Triangle}(t)$, then the SPWM_1 signal goes low to 0.¹³

Figure 51: SPWM_1 Signal Generated Using $\text{Sin}(t)$

Figure 52 shows the same thing being done for SPWM_2 , the resulting SPWM signal generated from the control signal $-\text{Sin}(t)$ and switching waveform $\text{Triangle}(t)$. If $-\text{Sin}(t)$ is greater than $\text{Triangle}(t)$, SPWM_2 goes high, else SPWM_2 goes low. In order to achieve the final signal, SPWM_2 is subtracted from SPWM_1 , the result is shown in Figure 53. Also, shown is the desired sinusoidal frequency. The benefits of bipolar over unipolar switching are that it doubles the switching frequency and also reduces the voltage jumps in the output voltage by half.

Figure 52: SPWM₂ Signal Generated Using $-\sin(t)$

Figure 53: Resulting PWM Signal and Desired Sinusoidal Frequency

It is advantageous to double the switching frequency because of the effects on the harmonic spectrum. The two control signals are out of phase by 180, which means that their harmonic components at the switching frequency in the output voltage have the same phase and thus cancel each other out. The sidebands of the switching frequency harmonics will disappear, as well as, the dominant harmonic at twice the switching frequency, though its sidebands will not.¹³ It is useful to reduce the harmonics in the voltage output because of their consumptive effects. Power is only transferred by the fundamental frequency of current and power. Harmonics can load a translation system, causing an increase in the apparent power. The apparent power is the sum of the real and reactive power, as shown in Equation 21 below, where P is the real power in Watts and Q is the reactive power, often expressed in volt-amperes reactive or var.

$$S = P + jQ \quad \text{Eq. (21)}$$

The j represents the imaginary element mathematically associated with the reactive power. It is common to refer to S in voltamperes (VA) and can also be written as in Equation 22, where $(\delta - \beta)$ represents the angle between the voltage and current, respectively.

$$S = VI \cos(\delta - \beta) + jVI \sin(\delta - \beta) \quad \text{Eq. (22)}$$

This phase angle is called the power factor angle, and the term $\cos(\delta - \beta)$ is called the power factor. If the current lags the voltage, so β is less than δ , then the power factor is lagging; if the current lead the voltage, so β is more than δ , then the power factor is leading.¹⁴ For a grid-connected PV system, the IEEE Standard 929 states that if it is

exceeding its rated output by 10%, then it must operate at a power factor greater than 0.85, leading or lagging.¹ This reactive power due to the harmonics will reduce the power factor of the signal being fed into the utility.

CHAPTER VI

UTILITY DETECTION

In order to be able to synchronize the power converter's output to the utility signal, it is necessary to be able to detect the amplitude and phase of the utility signal in order to match up the signals. This is also imperative if power is to be fed back to the utility. This is accomplished by having the phase of the PCU's output lead that of the utility.

Utility Amplitude Detection

The schematics shown in Figure 54 is the circuit used in conjunction with software, to detect the amplitude of the utility. This is necessary in order to synchronize the output of the inverter to the utility voltage. An optically isolated analog link feeds the positive half of the sinusoidal waveform from the utility voltage to the AD input port of the MCU. Here, the signal is converted to a digital signal and implemented into the control algorithm. The electrical isolation is provided by the HCNR-200 analog optoisolator, which has one LED but, two identical photo detectors. The input photodiode is used to monitor and stabilize the output of the LED. This allows for the chip to eradicate virtually all nonlinearity and drift characteristics. The output photodiode produces a current proportional to the illumination received from the LED. This signal is then amplified and then buffered before being sent to an AD port of the microcontroller.

Figure 55 shows the simulated output of the circuit. The signal was taken across diode D3. The opto-coupler removes any voltages less than 0V before the signal is fed into the microcontroller, slightly changing the shape of the resultant waveform.

Figure 54: Schematic of Utility Amplitude Detection Circuit

Figure 55: Simulated Output of Utility Amplitude Detection Circuit

Utility Phase Detection

The circuit in Figure 56 is used for phase detection. It will output a logic high signal to the processor when the utility is in the positive half cycle, and a logic low when the utility is in the negative half-cycle. Diodes D1 and D2 generate an oscillating negative and positive as the negative and positive parts of the utility signal pass. That voltage is sent to the comparator. If the voltage is positive the comparator outputs a logic high, otherwise it outputs a logic low. The comparator's output is then sent to the HCPL-2211 opto-isolator before being fed into the Synch port of the microcontroller.

Figure 56: Schematic of Utility Phase Detection Circuit

Figure 57 shows the simulated output of the utility phase detection circuit. The top graph shows the power being dissipated across the resistor, R_{zc} , used as the voltage divider, which takes a proportionate amount of the utility's voltage to use in the circuit. The second graph shows the current flowing through that resistor. The third graph shows the signal sent to the synch port in green and the utility voltage in blue. The zero

crossings and switch-over points are correlated exactly. The bottom two graphs show the signal at earlier points in the circuit. The forth graph shows the output from the comparator before it is sent through the opto-coupler and the last graph shows the fluctuating voltage across diodes, D1 and D2, in green. The utility voltage is also shown in blue. The zero-crossings are lined up precisely here, as well.

Figure 57: Simulated Output of Utility Phase Detection Circuit

CHAPTER VII

CONCLUSIONS

The smart utility interface designed includes a number of innovative features. Among them is the use of the multiplying effect of the Hall sensor. This phenomenon generates a Hall voltage proportional to the instantaneous power developed by the PVs. Tracking the power output of the panels is necessary and this feature of Hall sensors allows the tracing to be accomplished in a simple manner and with low power consumption. The use of a multi-level inverter is also helpful in that it drastically improves the sinusoidal output of the inverter while eliminating the need for filtering hardware. This is important in consumer applications, as it will reduce the size and weight of such a product. Power-tracking inverters that are currently on the market weigh anywhere from 75 to 125 pounds and occupy 1.8 to 2.9 cubic feet. Using the techniques described in this paper will reduce the weight and size such a device.

The hardware is tied together using the 9S12 personality module, a member of the Motorola HC12 family. All code for the control software was written in assembly language. In addition to controlling the inverter and synchronizing its output to the utility, this algorithm also tracks the power from the PVs and adjusts the real and reactive power in order to operate at the panel's optimum point. It operates the inverter with PWM using uni-polar switching. This effectively doubles the switching frequency, helping to reduce the harmonics in the output signal. It is necessary to eliminate as many harmonics as possible as they reduce the power factor of the voltage output which will have destructive

effects on the utility. This helps to ensure that the device will adhere to the IEEE Standard 929 and the *NEC*.

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APPENDIX A: COMPONENT RATINGS

This appendix contains partial data sheets for components used in this project.

NA-25 Open-Loop Current Sensor¹⁵

Measuring Circuit	<u>Units</u>	
Full Scale (FS) DC or AC peak (1)	+ A	25
Full Scale output (2)	+ mV	22.5 to 62.5
Excitation Circuit		
Nominal excitation current (I _c)	mA	7
Maximum excitation current (I _c)	mA	10
Input resistance	ohms	450 to 900
Output		
Sensitivity (2)	mV/A	0.9 to 2.5
Linearity	%FS	1
Maximum zero offset	+ mV	25
Maximum hysteresis of offset (3)	+ mV	0.15
Minimum load resistance.....	k ohms	10
Output resistance	ohms	<3200
Influences On Accuracy		
Maximum offset drift with temperature	+ $\mu\text{V}/\mu\text{oC}$	4 0
Excitation change of +1% Max. sensitivity change.....	+ %	1
Maximum sensitivity drift with temperature	+%/oC	- 0.07
Withstand Capabilities		
Dielectric test (4)	kV	0.5
Output short or open	NoDamage	
General Information		
Operating temperature range.....	oC	-40 to +85
Storage temperature range.....	oC	-40 to +100
Aperture opening	in (mm)	0.2 (5.1)
Current carrying conductor diameter (12 AWG).....	in (mm)	0.087 (2.21)
Weight	grams	3.4
Output short or open circuit	NoDamage	
Output reference	Conventional current flowing in direction of dot or arrow results in a positive difference in V _H .	
Frequency Response	kHz	1

LMD18200¹⁶

Absolute Maximum Ratings

Total Supply Voltage :	60V
Voltage at Pins 3, 4, 5, 8 and 9:	12V
Voltage at Bootstrap Pins (Pins 1 and 11):	V _{OUT} +16V
Peak Output Current (200 ms):	6A
Continuous Output Current:	3A

Power Dissipation:	25W
Lead Temperature (Soldering, 10 sec.):	300°C
Junction Temperature, T _J (max):	150°C
Electro-Static Discharge (ESD) Susceptibility:	1500V
Storage Temperature, T _{STG} :	-40°C to +150°C
Operating Ratings	
Junction Temperature, T _J :	-40°C to +125°C
V _S , Supply Voltage:	+12V to +55V

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