FAST TRANSIENT BEHAVIOR OF
THYRISTOR SWITCHES

by

JERRY LYNN HUDGINS, B.S.E.E., M.S.E.E.

A DISSERTATION

IN

ELECTRICAL ENGINEERING

Submitted to the Graduate Faculty
of Texas Tech University in
Partial Fulfillment of
the Requirements for
the Degree of

DOCTOR OF PHILOSOPHY

IN

ELECTRICAL ENGINEERING

Approved

Accepted

December, 1985

U1
T3
1985
No. 89
Copy 2

ACKNOWLEDGMENTS

I wish to thank Dr. William Portnoy and the members of the Solid State Electronics Lab. I am also grateful to engineers at Westinghouse Corporation and International Rectifier Incorporated.

TABLE OF CONTENTS

	Page
ACKNOWLEDGMENTS	ii
ABSTRACT	v
LIST OF TABLES	vi
LIST OF FIGURES	vii
I. INTRODUCTION	1
II. CHARACTERIZATION PARAMETERS AND TEST CIRCUITS ...	3
Blocking Voltage	3
Gate-Cathode Diode Characteristics	9
Gate Trigger Characteristics	17
Anode Holding Current	17
Anode Forward Current-Voltage Characteristics	20
III. TEST CIRCUITS	22
Pulse Forming Networks	22
Gate Drive Circuit	49
Resonant Charging Supply	61
IV. MEASUREMENT PROCEDURES	67
Test Devices	67
Measurement Protocol	69
Device Fixture	70
Instrumentation	72

V.	RESULTS AND DISCUSSION	73
	Initial Characterizations	73
	Single-Shot Stress	93
	Repetitive Stress	135
	Failure Analysis	154
VI.	CONCLUSIONS	155

ABSTRACT

The fast pulse switching behavior of center-fired and interdigitated thyristors was studied by switching 10 μ s, 1000 A (at 800 V) pulses. Single-shot switching was performed up to 10,000 A/ μ s, and repetitive switching at 500 Hz and 800 Hz up to 10,000 A/ μ s for various lengths of time. No damage to the devices resulted from the switching stresses.

LIST OF TABLES

Table	Page
1. Device DC Parameters	75
2. Piecewise Linearized Equivalent Circuit Parameters for the Gate-Cathode Diode Characteristic Curves for the T72H-45 Thyristor	87
3. Piecewise Linearized Equivalent Circuit Parameters for the Gate-Cathode Diode Characteristic Curves for the T7S7 Thyristor	88

LIST OF FIGURES

Figure		Page
1.	Circuit schematic for the blocking voltage tester	4
2.	Phase relationships between the voltage at the secondary of the input transformer, the amplifier output square wave and the Schmitt NAND output	6
3.	Open circuit output voltages	10
4.	Gate-cathode diode test circuit	13
5.	Timing diagram for the timer outputs	14
6.	Stairstep output of the digital-to-analog converter	16
7.	Circuit for the gate trigger measurements	18
8.	Anode holding current measurement circuit	19
9.	Measurement circuit for the forward voltage drop	21
10.	Lumped equivalent of a transmission line	23
11.	Simulated output of the 100 μ s PFN	25
12.	Simulated output of the 10 μ s PFN	26
13.	Effect of series inductance on the 10 μ s PFN output pulse	27
14.	Photographs of the PFNs	29
15.	Photograph of the 8 μ s PFN	31
16.	Output pulse of charged coaxial line	33
17.	Output pulse of the 100 μ s PFN	35
18.	Output pulse of the 10 μ s PFN	37

19.	Output pulse of the modified 10 μ s PFN	41
20.	Output pulse of the 8 μ s PFN	43
21.	Output pulse of the modified 8 μ s PFN with the hammer switch and aluminum slug	45
22.	Output pulse of the modified 8 μ s PFN with the hammer switch and T720 package	47
23.	Gate trigger circuit	51
24.	Typical 100 μ s gate trigger pulse	53
25.	Typical 10 μ s gate trigger pulse	55
26.	Gate current flow due to negative anode current	58
27.	Typical 8 μ s gate pulse	59
28.	Typical short gate trigger pulse	62
29.	Resonant charging circuit for repetitive discharge of the 10 μ s PFN	64
30.	Resonant charging circuit for repetitive discharge of the 8 μ s PFN	65
31.	Gate structures for the test thyristors	68
32.	Low inductance device mounting fixture	71
33.	Anode forward current-voltage characteristic curve	74
34.	Forward blocking voltage waveforms	77
35.	Single-pulse blocking voltage waveforms	79
36.	Typical low current gate-cathode diode characteristic curves	82
37.	Model for the piecewise linearization of the gate-cathode diode characteristic curve	84
38.	Pulse high current gate-cathode diode characteristics	85

39.	Typical switching waveforms for the 100 μ s PFN ...	90
40.	Current rise and voltage fall times on expanded time scales for the switching waveforms for the 100 μ s PFN	91
41.	Anode current and voltage waveforms for the T72H-45 at 1000 A/ μ s	94
42.	Leading edges of the current and voltage waveforms on expanded time scales for the T72H-45 at 1000 A/ μ s	96
43.	Representative current and voltage waveforms for the T7S7 at 1000 A/ μ s	99
44.	Leading edges of the current and voltage waveforms on expanded time scales for the T7S7 at 1000 A/ μ s	100
45.	Leading edges of the current waveforms on expanded time scales for the T72H and the T7S7 at 2000 A/ μ s	102
46.	Typical voltage fall on an expanded time scale for the T72H-45 and the T7S7 at 2000 A/ μ s	104
47.	Typical anode current pulse for the T72H-45 and the T7S7 at 5000 A/ μ s	106
48.	Leading edges of the current waveforms on expanded time scales for the T72H-45 and the T7S7 at 5000 A/ μ s	107
49.	Typical voltage falls on expanded time scales for the T72H-45 and the T7S7 at 5000 A/ μ s	109
50.	I_R and V_{AK} for device T720-35-27 to measure time delays	113
51.	Gate trigger pulse for device T720-35-29	115
52.	V_{AK} fall and I_A pulse for device T720-35-29	117
53.	Reduced gate trigger pulse	120
54.	Minimum gate trigger pulse	122

55.	V_{AK} and I_A leading edges corresponding to minimum gate trigger pulse width	123
56.	Delay of I_A rise with respect to I_{GK} for device T720-35-29	124
57.	Typical I_A and V_{AK} waveforms for T72H-40 devices	126
58.	Gate trigger pulses for 650PBQ-1 device	129
59.	Leading edge of I_A and V_{AK} for device 650PBQ-1	131
60.	Narrow gate trigger pulse for device 650PBQ-X-2	132
61.	Leading edge of I_A and V_{AK} for device 650PBQ-X-2	134
62.	Photograph of the load and mounting structure	137
63.	Anode voltage charging waveform (T7S7-6)	138
64.	Single anode current pulse at 2500 A/ μ s and 500 Hz (T7S7-6)	139
65.	Single anode current pulse at 2000 A/ μ s and 500 Hz (T7S7-3)	141
66.	Leading edges of the current and voltage single pulse waveforms on expanded time scales for T7S7-3 at 2000 A/ μ s and 500 Hz	142
67.	Single anode current pulse at 2000 A/ μ s and 500 Hz (T72H-45-8)	145
68.	Leading edges of the current and voltage single pulse waveforms on expanded time scales for T72H-45-8 at 2000 A/ μ s and 500 Hz	146
69.	Single pulse voltage fall on an expanded time scale for T72H-45-18 at 1600 A/ μ s and 1 KHz	149
70.	Repetitive V_{AK} waveforms for device T72H-40-19	151

CHAPTER I

INTRODUCTION

Although the development of pulsed power technology depends on the availability of high energy density storage devices and suitable pulse forming networks, the principal limitation is probably the switch. No switch at this time meets simultaneously the many specifications of a satisfactory closing device, and opening switches are still primitive. Hard glass tubes, such as thyratrons and spark gaps, are commonly used as closing switches; however, their lifetime and reliability are severely affected by electrode erosion, surface flashover, reaction products, and similar poorly understood effects. On the other hand, semiconductor switches have demonstrated long life and reliability under a variety of conditions which imply similar dependability under the stress of fast, high-power pulses, and the use of semiconductor thyristor closing switches deserves serious consideration.

Thyristors are used at present for many switching applications, and their static characteristics and behavior after turn-on have been extensively studied. However, transient turn-on, probably the most important constraint on fast thyristor switching, has scarcely been addressed. Although thyristor switches have been characterized for

low frequency and long pulse operation, there is essentially no information respecting fast pulse switching by such devices. Models for turn-on of semiconductor thyristor switches have been proposed, but none have been applied to thyristor operation in the very fast, high current, short pulse regime; no significant data respecting such operation are available, and it is not possible to describe theoretical or actual performance limits. User results, generally undocumented, indicate that thyristors will occasionally exceed their ratings by factors which cannot be explained on the basis of present models or manufacturing technology. The purpose of this work was to establish more realistic performance characteristics of semiconductor switching devices by a careful series of pulsed measurements.

CHAPTER II

CHARACTERIZATION PARAMETERS AND TEST CIRCUITS

Although not all the test circuits were used in the characterization procedures which were finally selected, a number of preliminary characterizations were performed. These involved forward and reverse blocking voltage, pulsed gate-cathode diode forward current-voltage behavior, gate trigger voltage and current, anode holding currents, and DC forward voltage drop.

Blocking Voltage

Forward and reverse blocking characteristics are probably the most important parameters for establishing degradation. Although maximum leakage current is specified at rated blocking voltage, this current is a 125 °C value; at room temperature, no significant leakage current flows in a good device. It was not practical to establish a percentage change in room temperature leakage current as a criterion for degradation; serious degradation was assumed to have occurred if the room temperature current at 800 V exceeded its 125 °C value, 30 mA for the T7S7 and 35 mA for the T72H-45. The blocking voltage test circuit, shown in Figure 1, provides a continuous or single pulse half-

rectified 60 Hz sinusoidal voltage of appropriate polarity to the anode of the test device. The peak voltage amplitude can be varied between almost zero (100 mV) and 1000 V.

In the pulse mode, a 5 V signal, transformed down from the line voltage, is fed to a two-stage amplifier. The amplifier has an overall gain of 1000 and saturates rapidly, so that its output is a 10 V square wave with very fast leading and trailing edges. The square wave is fed to a Schmitt NAND gate which clips the negative-going pulse and increases the rise time of the positive-going pulse. Figure 2a shows the output from the secondary of the input transformer relative to the output from the amplifier. In Figure 2b, the transformer voltage is shown relative to the Schmitt NAND output. It can be seen that the output of the NAND gate is a positive 5 V, 60 Hz pulse synchronized with the line voltage such that the trailing edge of the pulse is at the positive-going zero-crossing of the line voltage.

The output from the Schmitt trigger is fed to one input of an AND gate. The other input is usually at 5 V (BCD 1) so that the Schmitt pulse feeds directly to the clock of the 4-bit binary counter. One reset of the counter, RS2, is tied directly to 5 V. The other reset, RS1, is connected to a single-pole double-throw switch. In normal counting mode, RS1 is grounded. The clock pulses cause the counter to count from BCD 0 to BCD 15. (A is the least significant bit and D, the most significant bit.)

a.

b.

Figure 2. Phase relationships between the voltage at the secondary of the input transformer and a) the amplifier output square wave; b) the Schmitt NAND output.

The counter outputs (A, B, C and D) are connected to a 4-input AND gate whose output goes high at BCD 15. This signal is inverted and fed into the AND gate with the Schmitt signal. As the counter changes from BCD 14 to BCD 15, the clock signal goes to 0. In this way, the counter counts from 0 to 15 at 60 Hz and then stops until the counter outputs are manually reset by switching RS1 to 5 V.

The outputs of the counter are also tied to a second 4-input AND gate (with A inverted), so that a 5 V pulse appears at BCD 14 at the output of the second AND. This pulse is used as a leading edge trigger for a monostable multivibrator which has a 5 V, 500 μ S output pulse. The pulse is fed to a transistor, buffered by a unity gain op amp; the transistor drives a transformer which gates an SCR switch.

The line voltage is fed through a DPDT switch, set to continuous mode (connecting the mechanical timer), or to single pulse mode (short), to the primary of a variable transformer. The secondary is connected to another DPDT switch, set to continuous mode (short) or pulse mode (tying in the SCR). In the pulse mode, the SCR is in series with the primary of a power transformer. The gate pulse turns on the SCR just as a positive half-wave rectified current appears at the anode, allowing current flow through the primary of the transformer. The SCR self-commutates on the

The counter outputs (A, B, C and D) are connected to a 4-input AND gate whose output goes high at BCD 15. This signal is inverted and fed into the AND gate with the Schmitt signal. As the counter changes from BCD 14 to BCD 15, the clock signal goes to 0. In this way, the counter counts from 0 to 15 at 60 Hz and then stops until the counter outputs are manually reset by switching RS1 to 5 V.

The outputs of the counter are also tied to a second 4-input AND gate (with A inverted), so that a 5 V pulse appears at BCD 14 at the output of the second AND. This pulse is used as a leading edge trigger for a monostable multivibrator which has a 5 V, 500 μ S output pulse. The pulse is fed to a transistor, buffered by a unity gain op amp; the transistor drives a transformer which gates an SCR switch.

The line voltage is fed through a DPDT switch, set to continuous mode (connecting the mechanical timer), or to single pulse mode (short), to the primary of a variable transformer. The secondary is connected to another DPDT switch, set to continuous mode (short) or pulse mode (tying in the SCR). In the pulse mode, the SCR is in series with the primary of a power transformer. The gate pulse turns on the SCR just as a positive half-wave rectified current appears at the anode, allowing current flow through the primary of the transformer. The SCR self-commutates on the

negative half-cycle so that only one pulse appears at the secondary.

At the secondary, the positive half-wave rectified current flows through three diodes in series to the device under test (DUT). The anode voltage at the test device is measured directly, and the anode leakage current is measured with a sampling resistance. The blocking voltage amplitude is controlled by the variable transformer in the primary circuit.

In the continuous mode, the switch on the primary of the variable transformer is set so that the mechanical timer is in the circuit. The mechanical timer is adjustable for a continuous wave train, 1 to 10 seconds in duration. The switch in the power transformer primary must also be in the continuous mode to allow primary current flow. With the switch in this position, the SCR is completely disconnected from the primary circuit. The diodes in the secondary half-wave rectify the signal so that a train of positive sinusoidal pulses appear at the DUT during the timed interval.

Thyristor blocking voltage is measured with the gate open-circuited. All switches are set in the single-pulse mode with the voltage set to 0 V. The toggle switch connected to RS1 of the counter is switched to 5 V to reset the outputs; the switch is then toggled to ground to permit one pulse to appear across the DUT. The counter is again

reset and triggered with the output of the variable transformer increased to some voltage greater than zero. The process is continued until the rated blocking voltage is reached; anode leakage current is measured at this value. The reverse leakage current is measured with the anode and cathode polarities reversed from their forward leakage configuration. Leakage current measurements for a train of continuous pulses are made the same way, except that all switches are placed in continuous mode, placing the mechanical timer in the circuit and short-circuiting the SCR. Typical open circuit single pulse and repetitive pulse voltages are shown in Figure 3.

Gate-Cathode Diode Characteristics

The limiting rate at which a thyristor turns on depends on the amount of power which can safely be dissipated in the region where switching is initiated. A current flows between the gate and the cathode in the p-base when a trigger pulse is applied to the gate; the accompanying lateral voltage drop establishes a greater forward bias at the emitter edge nearest the gate than at the rest of the emitter, and only a small part of the device directly adjacent to the gate turns on. Once forward conduction begins, the gate loses control, and gating current can be supplied to the remaining off portions of the thyristor only by carrier diffusion from

a.

b.

Figure 3. Open circuit output voltages
for a) a single pulse;
b) repetitive pulses.

the adjacent on-region. A considerable time may elapse before the entire cathode area turns on, and during this time the entire anode current flows only through the small part of the total device area which has been turned on. At high values of dI/dt , high localized power dissipation and heating may damage the device. However, if the gate drive is increased, it is possible to increase the turned on region, and higher dI/dt may be obtained. In this work, the effects of very high values were to be examined, so that correspondingly hard gate drives were desired. The gate drive itself, however, is limited by the maximum power which can be dissipated at the gate-cathode junction. No such values could be obtained from the manufacturer's literature, so that a measurement of the maximum current which could safely flow through the gate was required. Inasmuch as only a pulsed current would flow during the actual stress, a pulsed measurement was designed, in which a sequence of widely separated pulses, whose widths were the same as the gating pulse to be used during the measurement, and the amplitudes of which increased linearly during the sequence, could be delivered to the gate. The maximum gate current would then be that value just before gate burnout. This measurement could also be used to determine if any changes in the gate-cathode forward characteristics at high gate currents occurred after dI/dt stress. (Changes at lower currents could be safely observed using a

curve tracer.)

The circuit shown in Figure 4 has a family of sixteen current pulses as its output. The first pulse has the lowest amplitude, each succeeding pulse increasing in amplitude. The pulses are 100 μ s long; there is 1.5 ms between pulses, so that the pulse period is 1.6 ms. The duration of the pulse train is 25.6 ms. The long interval between pulses permits the gate-cathode diode to recover from any transient effects of one pulse before the next pulse appears. The interval between pulse trains may be increased up to 1.8 s even more to reduce heating. The maximum current pulse amplitude can be varied between 100 μ A and 12 A.

The pulses are controlled by two timers. One timer is biased for an output pulse exactly 100 μ s wide; the other is biased such that its output, by way of a toggle switch, can reset the counters after one pulse train, then enable another train after some time interval (up to 1.8 s). The potentiometer (R3) on the first timer sets the current pulse width (the clock period) to 100 μ s. The potentiometer (R5) on the second timer sets the duty cycle such that exactly one sequence is enabled; following the first sequence, the counters are disabled for a time determined by the potentiometer R4. A timing diagram is shown in Figure 5. The switch sets either timed or free running operation (by setting RS1 to 0 and removing the second

Figure 4. Gate-cathode diode test circuit. Resistors: R1, 5.6 K Ω ; R2, 4.7 K Ω ; R3, 15 K Ω ; R4, 250 K Ω ; R5, 5 K Ω ; R6, 3.3 K Ω ; R7, 1 K Ω ; R8, 2.2 K Ω ; R9, 10 K Ω ; R10, 56 Ω ; R11, 1 Ω . Capacitors: C1, 0.01 μ F; C2, 5.6 nF; C3, 10 μ F; C4, 15 pF. Transistors: Q1, 2N5002; Q2, 2N5003. Integrated circuits: I1, NE555 timer; I2, SN7493 counter; I3, SN72741 operational amplifier; D/A, MCL408L8 digital-to-analog converter.

Figure 5. Timing diagram for the timer outputs.

timer from the circuit).

The output of the first timer is connected to the clock input of the first 4-bit counter. This counter has the four least significant bits, starting with A. The 4 bits are logically ANDed with the clock pulse to provide a clock pulse for the second counter, which generates the four most significant bits, every 1.6 ms. Outputs B, C and D are inverted and tied to a 4-input AND gate. The output of this gate, Q_A , is high at BCD 1, and low for BCD 0 and BCD 2 through 15. This output then has a period of 1.6 ms. Counter outputs E through H are individually ANDed with Q_A . Each AND gate output is tied directly to its appropriate input on the digital-to-analog converter, D/A. Outputs Q_B , Q_C and Q_D are tied to 0 V. Q_A , Q_E , Q_F , Q_G and Q_H are forced to 0 V during the 1.5 ms when B, C or D is at a logic high, and then allowed to take on their corresponding high or low, for 100 μ s, from the counter outputs. In this way, the D/A receives a non-zero input for BCD 1, 17, 33, 49, 65, 81, 97, 113, 129, 145, 161, 177, 193, 209, 225 and 241. The remainder of the D/A biasing circuit outputs the proper voltage to the amplifier. The output of the D/A is a staircase voltage waveform; there are 16 steps, each 100 μ s long, with 1.5 ms between pulses. The step levels increase in 0.31 V increments to 5 V at the sixteenth pulse. This waveform (Figure 6) is fed to the amplifier for voltage gain and isolation from the D/A converter. The amplifier

Figure 6. Stairstep output of the digital-to-analog converter.

output drives the base of an n-p-n transistor, whose output drives a p-n-p transistor which acts as a current source. Gate current is measured across the sampling resistor, R_{11} . The pulsed gate current vs. gate-cathode voltage characteristic curve is displayed in the x-y mode on an oscilloscope.

Gate Trigger Characteristics

The gate trigger current and voltage are measured with the circuit of Figure 7. The anode-cathode voltage is set to 12 V, and the gate-cathode voltage is slowly increased until the device switches on. The values of gate current and voltage at this point are the trigger values.

Anode Holding Current

The circuit for measuring the anode holding current is shown in Figure 8. The gate supply voltage, V_{GK} , is initially set to zero, as is the anode series resistance, R . V_{GK} is slowly increased until the anode-cathode voltage, V_{AK} , drops from 12 V to 1 or 2 V, that is, until the thyristor turns on. The gate is then open-circuited, and remains open-circuited during the measurement. R is then slowly increased until V_{AK} again increases to 12 V, that is, until the device turns off. The anode current measured just before the transistor turns off is the holding current.

Figure 7. Circuit for the gate trigger measurements. R_1 and R_2 are $10\ \Omega$, 5 W and $7\ \Omega$, 24 W resistors, respectively; M_1 is the gate trigger current ammeter; M_2 is the gate trigger voltage voltmeter; and M_3 is the anode current ammeter.

Figure 8. Anode holding current measurement circuit.

Anode Forward Current-Voltage Characteristics

The thyristor is triggered on, after which the gate supply is disconnected. The anode forward current-voltage characteristics are then obtained by varying the anode current and measuring the anode-cathode voltage at a specified current (Figure 9). The anode source in these measurements was an HP 6464C high current (500 A) supply.

Figure 9. Measurement circuit for the forward voltage drop.

CHAPTER III

TEST CIRCUITS

Pulse Forming Networks

Transmission lines cannot be used for generating pulses even of moderate width unless impractically long lines are used; practical circuits are lumped equivalent networks of transmission lines (Figure 10). However, high dI/dt pulses are difficult to obtain from pulse forming networks unless the pulses are narrow. In order to obtain the high dI/dt values required as stresses in this work, it was decided to use a pulse around 10 μs wide for the stress pulse. Inasmuch as transient turn-on in the test device was to be examined at this time, a short pulse was considered to be adequate. However, it was desirable to obtain the forward voltage drop at full turn-on, so a longer pulse, around 100 μs wide, was required as well; the rise time of this pulse would be much slower. In both cases, the peak current was chosen to be at least 1000 A, approximately twice the rated average current of the test devices. For an 800 V PFN, in which one-half the voltage is dropped across the internal impedance, this required a matched load of 0.4 Ω .

Two pulse forming networks were designed, employing a design program at the Los Alamos National Laboratory. The

Figure 10. Lumped equivalent of a transmission line
(Type E PFN).

first was a 12 section, equal inductance, equal capacitance, type E PFN, whose output was a 100 μ s pulse with a rise time of around 0.5 μ s. Physically, the network was designed to consist of 12 sections, each 4 cm long, each consisting of a 1.5 cm radius, 9 turn coil (1.34 μ H inductance) and a 10 μ F capacitor. Figure 11 shows the simulated output of the PFN obtained with the LANL Net-2 circuit analysis program. The second PFN was a 125 section equal inductance, equal capacitance, type E network; each section was 1.5 cm long, consisting of an 0.75 cm radius, 1 turn coil (10.2 nH) and an 0.1 μ F capacitor. This PFN, charged to 800 V, delivers a 1000 A, 10 μ s pulse, with a 100 ns rise time, to a matched load. Figure 12 shows the rise time associated with the first 10 sections (0.8 μ s pulse width: the width is increased by adding series sections). The rise time can be varied with an appropriate series inductance; Figure 13 is a plot of the output pulse with series inductances of 100, 200 and 500 nH. This network is sensitive to stray inductance (although a capacitor series inductance up to around 10 nH does not affect the network seriously) so that the device fixture inductance is important.

For the 100 μ s PFN, a continuous inductor, around 19 inches long, was helically wound on a cylindrical Teflon core, using 8 gauge annealed copper wire. (This has a room temperature resistance of 20.6 $\mu\Omega$ /cm, corresponding to a

Figure 11. Simulated output of the 100 μ s PFN.

Figure 12. Simulated output of the 10 μ s PFN (10 sections).

Figure 13. Effect of series inductance on the 10 μ s PFN output pulse.

total resistance of $0.012\ \Omega$ [5% of the load] for the 100 μs PFN, and of $0.012\ \Omega$ [3% of the load] for the 10 μs PFN.) The L-C sections were obtained by introducing short capacitors to a ground plane at appropriate locations along the inductance. GE 26F6626, 10 μF , 680 VAC capacitors were used in the 100 μs PFN. (These operate safely at 1000 VDC.) The load for this PFN was formed from a parallel array of eight 3.2 ohm, 2 watt carbon composition resistors. The inductor for the 10 μs PFN was similarly wound on a Lucite core; in this case, the total length of the coil, around 74 inches, was not convenient, so the PFN was folded into two sections, each some 37 inches long. This PFN incorporated Sprague 10PS-P10, 0.1 μF , 1000 VDC capacitors. The load here was a T and M Research Products Series A, Model BNC-5-4, $0.4\ \Omega$ ($0.3972\ \Omega$), low inductance current viewing resistor. Figures 14a and 14b, respectively, are photographs of the 100 μs and 10 μs PFNs.

A third PFN was built to increase the current pulse rise time and to operate at higher frequencies for repetitive testing. This PFN provided a pulse with about an 8 μs width and a peak current of 1200 A to 1600 A (depending on the device being tested) into a $0.37\ \Omega$, 4.4 kW resistive load. The network consisted of 10 short linear sections of type E PFNs connected in parallel so that the currents from each section added. The sections were arranged radially, similar to the spokes of a wheel, with the test SCR at the

a.

b.

Figure 14. Photographs of the PFNs:
a) 100 μ s; b) 10 μ s.

hub. A photograph of the PFN is shown in Figure 15. The inductors of each section were made by wrapping insulated solid conductor 12 gauge copper wire around a 3/4" O.D. phenolec core; the turns were in contact with each other; that is, there was no separation between them. Each core was 16 inches long. A capacitor was placed every 11 turns along the coil; each section contained eleven capacitors which were the same type as used in the 10 μ s PFN. The calculated total coil inductance was 18 μ H and the total capacitance was 1.1 μ F for each section (the impedance of each section was around 4 Ω). Each coil and its accompanying capacitors were placed on a copper ground plane and separated from it by a sheet of 0.005 inch mylar. The mylar was used because the wire insulation was rated for only 600 V. The load for each section consisted of 209 resistors in parallel, each 820 Ω and 2 W. (The total number of resistors in the load was then 2190.) These resistors were arranged in lines on each side of the inductor coil with one end pushed through to the PFN groundplane from underneath and soldered to it. The spacing between resistors was about 0.5 inch. The other ends of these resistors were soldered to a common copper plane. Each section was turned on its side and the outputs tied together with braided copper straps.

The PFNs were energized by charging them to 800 V through a 1 M Ω series resistance. Their pulse characteris-

Figure 15. Photograph of the 8 μ s PFN.

tics were determined by discharging them through their loads and measuring the load voltages. In order to avoid introducing switching artifacts, the PFNs were discharged using a fast discharge switch. This switch consists of two brass electrodes separated by a Mylar layer and a lead sheet. The switch is closed by driving a nail through the top brass electrode and the Mylar layer into the sheet of lead, which rests on the bottom brass electrode, and which prevents bounce. The nail, driven by a hammer, closes the switch in times much shorter than the rise time of the output pulse. A picture of the switch discharging a piece of coaxial line charged to 800 V is shown in Figure 16a. The leading edge of the pulse (Figure 16b) shows the 10% to 90% rise time is less than 1 ns.

Typical output pulses are illustrated in Figure 17 (100 μ s PFN) and 18 (10 μ s PFN). The measured output of the 100 μ s PFN (Figure 17a) has very similar characteristics to those predicted by the pulse simulations (Figure 11). The predicted width is around 90 μ s; the observed width is around 100 μ s. The rise time of the simulated pulse (to 800 A) is around 2.4 μ s (330 A/ μ s); that of the actual pulse (shown on an expanded time scale in Figure 17b) is around 2.2 μ s (360 A/ μ s) to 800 A. The observed current at the flat portion of the pulse is 900 A; the predicted current is around 960 A.

Figure 16. Output pulse of charged coaxial line:
a) entire pulse; b) pulse leading
edge. The horizontal scale for the
upper photograph is 5 ns per large
division, and for the lower photo-
graph, 1 ns per large division. The
vertical scale for both photographs
is 100 V per large division.

a.

b.

Figure 17. Output pulse of the 100 μ s PFN: a) entire pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 20 μ s per large division, and for the lower photograph, 1 μ s per large division. The vertical scale for both photographs is 250 A per large division.

0 a.

0 b.

Figure 18. Output pulse of the 10 μ s PFN. a) entire pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 2 μ s per large division, and for the lower photograph, 200 ns per large division. The vertical scale for both photographs is 250 A per large division.

0

a.

0

b.

Agreement between the simulated and observed output pulses for the 10 μ s PFN is not so good. Predicted values (Figure 12) of rise time (to 800 A) and peak current are around 60 ns (13300 A/ μ s) and 1000 A, respectively (10 sections only: pulse width is scaled); the observed pulse (Figure 18) has a peak current of 850 A and a rise time to 800 A of 340 ns (2350 A/ μ s).

The output pulses were obtained by measuring the voltages across the PFN loads. In both measurements, a Tektronix P6057, 100X, 1.4 GHz probe was used, with a Tektronix 7A19, 600 MHz plug-in amplifier in a 7834, 400 MHz mainframe, so that the measurement was not band-limited by the measuring instruments. The increased rise time and reduced peak current for the 10 μ s PFN output pulse is very probably the result of series inductance (see Figure 13). Although the load, the current viewing resistor, should be a low inductance configuration, the high dI/dt associated with the 10 μ s output pulse could affect the observed rise time even in a low inductance load, so a comparison measurement was made using a Pearson 411 current transformer, with a rise time of 20 ns. The shapes of the pulses obtained with the load voltage measurement and the current transformer were the same, as were the rise times, so that the parasitic series inductance is in the PFN itself. In order to reduce the leading edge rise time, 30 turns of the inductor were shorted and an additional

10 μF of shunt capacitance was added at the PFN output. Figures 19a and 19b show the respective output pulse and leading edge; the pulse shape is degraded, but the leading edge dI/dt has been increased to around 8000 A/ μs .

A typical output pulse from the 8 μs PFN is illustrated in Figure 20. The leading edge is shown in Figure 20b, and has a 10% to 90% rise time of 280 ns (2750 A/ μs). To test for effects of the device package on the current rate of rise, a dummy package, consisting of a cylindrical aluminum slug, having approximately the same dimensions as a T720 package, was placed in the device fixture; the hammer switch was then placed in series with the fixture and used as the system switch. (The last eleven turns of each PFN section were shorted to obtain the minimum rise time.) A typical current pulse and LE are shown in Figure 21. The 10% to 90% rise time corresponds to $dI/dt = 7100$ A/ μs , with a peak current of 1240 A and a level value of around 930 A. The measurement was improved by using an actual T720 package with the device chip replaced by a wafer of copper having the same dimensions (33 mm diameter by 0.25 mm thick). The resulting output waveforms are shown in Figure 22. The peak current is 1200 A and the 10% to 90% rise time corresponds to 6200 A/ μs (about 1000 A/ μs slower than the rise time of Figure 21); the peak current is lower with the device package in the mount, compared to the slug in the mounting

 

Figure 19. Output pulse of the modified 10 μ s PFN: a) complete pulase; b) pulse leading edge. The horizontal scale for the upper photograph is 2 μ s per large division, and for the lower photograph, 200 ns per large division. The vertical scale for both photographs is 250 A per large division.

a.

b.

1. The first part of the document is a letter from the author to the reader, explaining the purpose of the study and the methods used. The letter is dated 1st January 1998 and is addressed to the reader.

2. The second part of the document is a list of references, which includes books, articles, and other sources used in the study. The references are listed in alphabetical order.

3. The third part of the document is a list of figures, which includes tables, graphs, and other visual aids used in the study. The figures are listed in alphabetical order.

4. The fourth part of the document is a list of tables, which includes tables of data, tables of results, and other tables used in the study. The tables are listed in alphabetical order.

5. The fifth part of the document is a list of appendices, which includes appendices of data, appendices of results, and other appendices used in the study. The appendices are listed in alphabetical order.

Figure 20. Output pulse of the 8 μ s PFN: a) entire pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 2 μ s per large division, and for the lower photograph, 100 ns per large division. The vertical scale for both photographs is 200 A per large division.

a.

b.

Figure 21. Output pulse of the modified 8 μ s PFN with the hammer switch and aluminum slug: a) entire pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 2 μ s per large division, and for the lower photograph, 100 ns per large division. The vertical scale for both photographs is 200 A per large division.

a.

b.

Figure 22. **Output** pulse of the modified 8 μ s PFN with the hammer switch and T720 package: a) entire pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 2 μ s per large division, and for the lower photograph, 100 ns per large division. The vertical scale for both photographs is 200 A per large division.

a.

b.

structure. The package inductance is clearly significant in determining device performance at these values of dI/dt .

Gate Drive Circuit

A pulse commonly used when relatively high dI/dt is desired has a fast leading edge, with a current peaking at around three to five times the minimum trigger current, and decaying to a steady value, usually the minimum trigger current; the overall decay time to the steady value is approximately 20% of the pulse width, which is around 100 μs , at the end of which time the thyristor is completely turned on. This pulse shape was chosen for the gate drive in this work, but because very fast pulses were to be switched by the test thyristor, a very high peak current, 10 A or more, was selected, with a final steady value of around 5 A. This shape was to be used for the 100 μs characterization pulse, the 10 μs stress pulse and the 8 μs stress pulse except that, in the latter cases, the overall gate pulse width was reduced to the stress pulse width, with a proportionally reduced decay time. However, the actual gate drive in this work differed from conventional gate drives in another significant respect. The gate drive circuit is commonly isolated from the switched circuit by a pulse transformer; wave shaping is performed on the primary side of the transformer, with some peaking occasionally done on the secondary side. The gate is then

driven by a voltage pulse, and the gate current pulse may have a distorted shape. In order to assure that the gate current pulse had the desired shape, the gate was driven from a pulsed current source (Figure 23).

In order to obtain a constant current, the source output resistance must be high relative to the load resistance; in this case, the gate-cathode diode. In that case, in order to obtain a high peak current, the source voltage must also be high; a high voltage switch is then required to discharge the pulse shaping circuit. An IRF610 power MOSFET was selected as the switch because of its high breakdown voltage, relatively low input capacitance, and fast switching rise time. Because the input capacitance of the IRF610 required very fast charging during the 8 μ s stress tests, a 30,000 μ F capacitor was placed across the output of the full wave rectified circuit (180 V power supply) so that current would flow from a capacitive source. A fast switching diode, the 1N5804, is placed antiparallel across the gate-cathode diode to clamp any reverse voltage when the thyristor switches on. The gate of the FET was driven by both Systron Donner 101D and HP 214A pulse generators; both deliver a 15 V pulse with rise times of around 10 ns. Because the cathode of the test device was tied to the system common during stress, the entire gate trigger circuit was floated with respect to system common.

Figure 23. Gate trigger circuit. Q: IRF610;
 D: 1N5804; R₁: 33 Ω ; R₂: 15 Ω ;
 C: 0.47 μ F (100 μ F pulse), 0.056 μ F
 (10 μ s pulse).

The oscilloscope used in the measurements was also floated by way of an isolation transformer so that no equipment was tied directly to ground. If the cathode of the SCR being tested was tied to earth ground, then the low potential side of the pulse generator, which floated from 25 V to 100 V peak with respect to earth ground, caused the internal diode of the IRF610 to conduct. The cathode of the test device was therefore floated by tying it to the oscilloscope common.

A typical 100 μ s gate trigger pulse is shown in Figure 24a. The load is the gate-cathode diode of a test thyristor with an anode-cathode short. Gate current is measured on the cathode lead of the DUT with a Pearson Model 2878 current transformer, which has a rise time of 5 ns. The gate current pulse is 100 μ s wide, with a peak current of 13 A and a steady value of 5.5 A; the decay time is around 20 μ s to 30 μ s. The leading edge of the pulse is shown in Figure 24b; the current rises to 10 A in around 40 ns and to 13 A in 70 ns. The 10 μ s trigger pulse and pulse leading edge are shown in Figures 25a and 25b, respectively. The pulse width here is 10 μ s, the peak current is around 14 A, the steady current value is 5 A, and the decay time, 2 μ s to 3 μ s. The current rise time is 40 ns to 10 A and 70 ns to 13 A. Current is measured with the Pearson Model 2878 current transformer on the cathode lead; the slight ringing which is observed may be the

Figure 24. Typical 100 μ s gate trigger pulse:
a) entire pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 20 μ s per large division, and for the lower photograph, 50 ns per large division. The vertical scale for both photographs is 5 A per large division.

a.

b.

Figure 25. Typical 10 μ s gate trigger pulse: a) entire pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 2 μ s per large division, and for the lower photograph, 50 ns per large division. The vertical scale for both photographs is 4 A per large division.

a.

b.

result of switching by the test thyristor, which here switches 800 V. The small current glitch about 16 μ s after the initial current spike is caused by negative current flow through the SCR. When negative cathode current begins to flow as a result of mismatch in the PFN circuit, the shunt diode, D, in the gate drive circuit becomes forward biased and allows part of the cathode current to flow into the gate of the SCR. Since this current flow through the Pearson coil is in the same direction as the initial gate current, it shows up as a positive current spike. This effect is shown in Figure 26. The top curve is the anode current flow in a test device in the 8 μ s PFN. The lower curve is the gate current pulse (a 250 ns pulse used here to trigger the SCR). The gate current spikes after 8 μ s correspond exactly to the negative anode current flow.

In the stress tests using the 8 μ s PFN, comparisons were made on the dI/dt values of anode current using the full 8 μ s gate pulse and a shorter (250 ns) gate pulse. No effects on dI/dt were seen by using the shorter gate pulse. Below about 250 ns (current zero to current zero), the dI/dt value decreased. A typical 8 μ s gate current pulse is shown in Figure 27a. The gate pulse peaks at 12 A, and then decays to about 5 A in 1 μ s. The leading edge is shown in Figure 27b. The current rises to 8 A in 20 ns and 12 A in about 42 ns. A typical short gate pulse is shown

Figure 26. Gate current flow due to negative anode current:
 The upper trace is the anode current with a vertical scale of 316.2 A per large division. The lower trace is the corresponding gate current with a vertical scale of 4 A per large division. The horizontal scale for both traces is 2 μ s per large division.

Figure 27. Typical 8 μ s gate pulse: a) entire pulse; b) pulse leading edge. The horizontal scale for the upper photograph is 1 μ s per large division, and for the lower photograph, 20 ns per large division. The vertical scale for both photographs is 4 A per large division.

a.

b.

in Figure 28; the peak current and rise time are similar to those in Figure 27b.

Resonant Charging Supply

Power requirements for repetitive stress increased significantly over those for single-shot discharges. For example, at 500 Hz, the PFN load must dissipate at least 2 KW, and at 1 KHz at least 4 kw, and the resistance limiting the steady current (Figure 23, R1: 33 Ω) in the gate trigger circuit must dissipate around 2.5 W. R1 was therefore replaced by a parallel array of three 100 Ω , 2 W resistors, and the PFN load for the 10 μ s PFN was reconfigured. An array of four Stackpole 4 Ω (nominal) carborundum disc resistors was assembled; these discs are 1 inch thick by 4.5 inches in diameter, and have low parasitic series inductance. The array consisted of a paralleled pair of two discs in series, connected to each other and to parallel aluminum end plates by way of compliant copper foil. The end plates were bolted together for mechanical support and also served as heat sinks. The entire assembly was force air cooled. The load for the 8 μ s PFN consisted of 2190 paralleled and air cooled resistors which could dissipate around 4.4 kw.

The PFN could no longer be trickle charged because the capacitors could not be charged sufficiently fast between repetitive discharges. Because of the restrictive simul-

Figure 28. Typical short gate trigger pulse. The horizontal scale is 50 ns per large division. The vertical scale is 4 A per large division.

taneous high voltages and high output currents required in a DC charging power supply, it was decided to charge the PFNs resonantly. The resonant charging circuit for the 10 μ s PFN is shown in Figure 29. The line voltage is isolated and stepped-up to a peak voltage of 424 V; this voltage is fed to a bridge rectifier whose output is filtered by three paralleled 240 μ F, 450 V electrolytic capacitors. The PFN is command charged through the inductor by a control thyristor. Originally, a diode was used instead of the SCR, but recharging of the PFN began before the test thyristor had fully turned off, so that it latched on and was destroyed. The diode was replaced by the thyristor to introduce a charging delay. The command trigger pulse is derived from the test thyristor trigger pulse, and delayed by 650 μ s, so that the charging cycle begins some 650 μ s after the PFN has discharged. The delayed pulse is isolated from the charging circuit by a pulse transformer. A resonant supply for the 8 μ s PFN was slightly different; the circuit diagram is shown in Figure 30. Because of the fast discharge of the PFN ($< 1 \mu$ s), the command SCR will self-trigger because its dV/dt rating of 200 V/ μ s is exceeded by the fast discharge of the PFN, so a snubber circuit is added in parallel across the command SCR to suppress triggering. Also, when operating repetitively, the gate drive circuit produces RF noise which is coupled to all unshielded wires in the

Figure 29. Resonant charging circuit for repetitive discharge of the 10 μ s PFN. D: SK3500; SCR: SK6632; C: 720 μ F; L: 19.8 mH.

Figure 30. Resonant charging circuit for repetitive discharge of the $8 \mu\text{s}$ PFN. T: Westinghouse variable static induction; D: SK3500; SCR: SK6632; C: $1020 \mu\text{F}$; L: 2.3 mH .

system and also to the command SCR, such that 1.2 V develops across the gate-cathode diode. The frequency of the noise is high enough to fire the command SCR randomly. Random triggering was inhibited by mounting the command SCR on a heat sink and shielding it by way of a metal box which was sealed with aluminum foil.

CHAPTER IV

MEASUREMENT PROCEDURES

Test Devices

Five types of thyristors in compression packages were tested: T72H084534DN (T72H-45), T72H084064DN (T72H-40), T720083504DN (T720-35), T7S7086034DN (T7S7), and 650PBQ120 (650PBQ). All are fast switching devices, differing principally in their gate-cathode geometries. The T7 devices are Westinghouse products. All are fast switching devices, differing principally in their gate-cathode geometries. All have rated repetitive peak blocking voltages of 800 V; the average forward currents for the T72H, T7S7 and T720 are 450 A, 600 A, and 350 A, respectively. All are 33 mm diameter chips with amplifying gates; however, the T7S7 and T720 are center fired, whereas the T72H is slightly interdigitated (Figure 31). The 650PBQ devices are made by International Rectifier. These are rated at 1200 V and 700 A, and are made from 38 mm diameter chips. They all contain the amplifying gate structures but in two devices, the amplifying gate was bypassed and the gate lead was tied directly to the main gate (650PBQ-X). The 650PBQ devices are also interdigitated, with more gate-cathode periphery than the Westinghouse T72H-40 or T72H-45.

a.

b.

Figure 31. Gate structures for the test thyristors: a) interdigitated, with amplifying gate; b) center-fired, with amplifying gate.

Measurement Protocol

All devices were electrically characterized initially and recharacterized after stress with respect to blocking voltage and gate-cathode diode characteristics. A chromel-alumel thermocouple was attached to the exterior cathode surface of the package for the devices which were stressed in the 8 μ s PFN, to monitor temperature changes during repetitive testing. Failure analysis consisted of the determination of gross fault modes by opening the packages and examining the device chips.

T7 Devices

Five each of types T72H-45 and T7S7 switched the 10 μ s PFN single-shot at stepwise increasing values of dI/dt until the maximum available value was reached. The remaining five T72H-45 and T7S7 devices were repetitively pulsed at a high value of dI/dt and recharacterized at logarithmic time materials. Five T720 thyristors were first single-shot, then repetitively stressed at the highest dI/dt available in the 8 μ s PFN. Two T72H-40 devices were stressed single-shot at the highest dI/dt delivered by the 8 μ s PFN; they were then stressed again at increasing values of dI/dt at one hour intervals.

650PBQ Devices

Two each of the 650PBQ and one of the 650PBQ-X devices were stressed single-shot in the 8 μ s PFN at the highest

value of dI/dt , then repetitively stressed, with a second 650PBQ-X, at the same dI/dt value.

Device Fixture

Commercial fixtures for compression packages have too high an inductance for these measurements, so a low inductance coaxial fixture was designed. The fixture was machined from aluminum, with the interior surfaces micro-machined to obtain flat and parallel, good electrical and thermal contact. The two parts of the structure enclose the device, and are clamped together under 2000 pounds of force for the T7 and 3000 pounds of force for the 650PBQ devices; Figure 32 shows the two segments of the fixture. The bottom, or cathode section, is tied to system common. The top, or anode section, is connected to the PFN by way of braided copper straps. An extra cathode lead and the gate lead are connected to the gate drive circuit through vertical slits in the fixture. In the 8 μ s PFN, a copper foil cylinder with attached vertical foil fins was clamped to the exterior surface of the fixture by two hose clamps; the fins made electrical connection to five pairs of the PFN sections. Dow-Corning 340 heat sink compound was lightly applied to the anode and cathode surfaces of the device package before it was clamped.

Figure 32. Low inductance device mounting fixture. The top section (anode) of the fixture is at the left, and the bottom section (cathode), at the right of the photograph.

Instrumentation

Waveforms were displayed on a Tektronix Model 7834 400 MHz storage oscilloscope, using a 7A19 600 MHz plug-in amplifier for very fast pulse, low impedance measurements, a 7A16A 225 MHz amplifier for fast pulse, high impedance measurements, and a 7A22 1 MHz differential amplifier for low frequency differential measurements. Chopped measurements were performed at the 1 MHz 7834 mainframe chopping rate. A 7B80 time base was used in all the measurements. Low current gate-cathode diode characterizations were performed on a 7633 mainframe, using a 7CT1N plug-in curve tracer.

Fast low voltage pulse measurements were made with the Tektronix P6057 1.4 GHz, 100X, low impedance probe; this probe was used principally to measure the voltage across the load in the single-shot stresses in the 100 μ s and 10 μ s PFNs. High voltage (anode and blocking voltage) measurements were made with the P6009 100 MHz, 100X, high impedance probe. Anode currents in all the 8 μ s PFN tests and in the repetitive stresses in the 10 μ s PFN were measured with the Pearson 110 current transformer, which has a 20 ns rise time; this is a larger version of the Pearson 411 current transformer.

CHAPTER V

RESULTS AND DISCUSSION

Initial Characterization

Anode Forward Current-Voltage Characteristics

Figure 33 is a graph of the anode forward current-voltage behavior for a T7S7 thyristor after turn-on. The curve is similar to that shown in the manufacturer's handbook (although the dip at low currents in this measurement is puzzling). The measurement was more troublesome to perform than anticipated, and the results were not as useful as those obtained from a pulsed measurement, so this characterization was not continued.

Device DC Parameters

The gate trigger current, I_{GT} , trigger voltage, V_{GT} , and anode holding current, I_H , (all with 12 V at the anode) for the T72H-45 and T7S7 devices are contained in Table 1. The average values for the T7S7 thyristors are 51 mA for I_{GT} , 1.28 V for V_{GT} , and 41 mA for I_H , and for the T72H-45 devices, 52 mA for I_{GT} , 0.89 V for V_{GT} , and 46 mA for I_H . The values for I_{GT} and V_{GT} are considerably lower than the specified values, which are 150 mA for I_{GT} and 3 V for V_{GT} for both types. No values are specified by the manufac-

Figure 33. Anode forward current-voltage characteristic curve.

Table 1
Device DC Parameters

T7S7

Device Number	I_{GT} (mA)	V_{GT} (V)	I_H (mA)
2	71	1.25	73
3	50	1.30	37
4	67	1.34	33
6	49	1.41	37
10	38	1.23	45
11	41	1.25	33
13	38	1.23	43
16	44	1.19	38
18	43	1.25	41
20	67	1.36	31

T72H

Device Number	I_{GT} (mA)	V_{GT} (V)	I_H (mA)
1	46	0.94	43
2	45	0.89	49
6	44	0.76	47
8	42	0.77	40
10	71	0.83	66
12	40	0.91	28
18	66	0.91	63
21	60	0.99	43
23	53	0.97	45
26	54	0.94	38

turer for I_H . These measurements are not difficult to perform, but they are time consuming, and the values were not considered to be as sensitive to degradation as the other parameters, so they were not continued.

Blocking Voltage

Figure 34 illustrates representative waveforms for forward single pulse (Figure 34a) and repetitive (Figure 34b) blocking. The current waveforms contain capacitive artifacts which are associated with the open circuit behavior of the blocking voltage test system, and which have no measurement significance. These appear in the reverse blocking waveforms also (not shown), which are very similar. The long tails on the voltage waveforms are the result of capacitive loading of the test circuit by the turned off thyristor. No significant room temperature leakage current ($\leq 500 \mu A$) during forward or reverse blocking was observed in seventeen of the first twenty T7 devices tested; the other three, T72H-45-6, T72H-45-12 and T72H-45-23, exhibited asymmetric high leakage; that is, T72H-45-6 and T72H-45-12 blocked in the reverse direction, but not in the forward, and T72H-45-23 blocked in the forward, but not in the reverse, direction. Figure 35 shows the single-pulse forward and reverse blocking waveforms for T72H-45-12 and T72H-45-23, respectively. Repetitive blocking waveforms are similar, and similar

Figure 34. Forward blocking voltage waveforms:
a) single-pulse; b) repetitive. The upper curves in both photographs are current waveforms (2 mA per large division), and the lower curves, voltage waveforms (500 V per large division). The horizontal scales for both are 5 ms per large division.

a.

b.

1. The first of these is the fact that the
 2. of the system is not a simple one.
 3. It is a complex one, and it is one
 4. which is not easily understood.
 5. It is a system which is not easily understood.
 6. It is a system which is not easily understood.
 7. It is a system which is not easily understood.
 8. It is a system which is not easily understood.
 9. It is a system which is not easily understood.
 10. It is a system which is not easily understood.

Figure 35 Single-pulse blocking voltage waveforms: a) forward blocking in T72H-12; b) reverse blocking in T72H-23. The lower curves in both photographs are current waveforms (5 mA per large division) and the upper curves, voltage waveforms (500 V per large division). The horizontal scales for both are 5 ms per large division.

a.

b.

results are obtained for forward blocking in the T72H-45-6. Five T720-35 devices (numbers 20 through 25) were initially leaky (similar to the currents of Figure 35); device 650PBQ-X4 also had a high initial leakage current.

Gate-Cathode Diode Characterization

Typical low current (≤ 160 mA) gate-cathode diode characteristic curves are shown for the T72H-45 and T7S7 devices, respectively, in Figures 36a and 36b. These curves can be piecewise linearized into several regions (two in Figure 36a and three in Figure 36b), permitting characterization of the gate-cathode diode in terms of the resistance and voltage parameters identified in the model of Figure 37. (Three breakpoints are shown in this model, but it can easily be modified to include only two.) The ideal Zener diode voltages correspond to the breakpoints in the linearization, and the resistances, to the slopes of the straight lines. Pulsed high current measurements were performed to 800 mA and to 12 A; these are illustrated in Figure 38. The equivalent circuit parameters for the T72H-45 and T7S7 devices are listed in Tables 2 and 3, respectively; in general, two breakpoints were obtained, except for the low current curves for the T72H-45 devices, which contained only one. Only the 12 A pulsed measurements were performed in later recharacterizations of these devices. The pulsed gate-cathode measurements were also

Figure 36. Typical low current gate-cathode diode characteristic curves: a) T72H; b) T7S7. The vertical scales in both photographs are 20 mA per large division; the horizontal scales are 0.5 V per large division.

a.

b.

a.

b.

Figure 37. Model for the piecewise linearization of the gate-cathode diode characteristic curve: a) three breakpoint linearization; b) equivalent circuit.

1. The first step in the process of creating a new product is to identify a market need. This involves conducting market research to understand the preferences and behaviors of potential customers. Once a need is identified, the next step is to develop a concept that addresses this need. This concept should be unique and offer a clear value proposition to the target market.

2. After developing a concept, the next step is to create a prototype. This allows the company to test the feasibility of the product and gather feedback from potential users. The prototype should be functional enough to demonstrate the core features of the product, but it does not need to be a fully finished version. This stage is crucial for identifying any design flaws or usability issues before moving forward with production.

3. Once a prototype is developed, the company must conduct a thorough testing phase. This involves evaluating the product's performance, reliability, and user experience. Testing can be done internally or through focus groups with potential customers. The goal is to ensure that the product meets the required quality standards and addresses the identified market need effectively. Based on the feedback received, the company may need to make adjustments to the design or functionality.

4. After successful testing, the next step is to develop a detailed business plan. This plan should outline the production process, distribution channels, marketing strategy, and financial projections. It is essential to have a clear understanding of the costs involved in manufacturing and distributing the product, as well as the potential revenue and profit margins. The business plan will serve as a roadmap for the company's operations and help secure funding if needed.

5. The final step in the process is to launch the product into the market. This involves implementing the marketing strategy outlined in the business plan to create awareness and drive sales. The company should monitor the product's performance closely after launch, gathering customer feedback and making any necessary adjustments to improve the product and its market reception. Continuous innovation and adaptation are key to long-term success in a competitive market.

Figure 38. Pulsed high current gate-cathode diode characteristics: a) to 800 mA; b) to 12 A. The vertical and horizontal scales in the upper photograph are 100 mA per large division and 0.5 V per large division, respectively; in the lower photograph, 2 A per large division and 1 V per large division, respectively.

a.

b.

Table 2
 Piecewise Linearized Equivalent Circuit
 Parameters for the Gate-Cathode Diode
 Characteristic Curves for the
 T72H-45 Thyristor

Low Current
 (≤ 160 mA)

Device Number	1	2	6	8	10	12	18	21	23	26
R_O (Ω)	20.0	19.0	15.0	17.0	11.0	25.0	12.0	19.0	20.0	22.0
R_1 (Ω)	3.0	3.0	1.5	2.2	1.6	2.8	3.4	3.2	3.0	2.7
V_1 (V)	0.88	0.86	0.81	0.80	0.79	0.89	0.85	0.90	0.88	0.91

Pulsed High Current
 (≤ 12 A)

Device Number	1	2	6	8	10	12	18	21	23	26
R_O (Ω)	3.3	2.8	2.5	2.2	1.7	3.3	2.5	2.5	2.5	3.3
R_1 (Ω)	0.69	0.89	0.57	1.1	0.65	1.1	1.4	1.2	1.1	1.1
R_2 (Ω)	1.2	0.31	0.71	0.28	0.98	0.80	0.74	0.73	0.66	1.3
V_1 (V)	2.4	2.0	1.6	1.6	1.2	2.2	1.8	2.0	2.1	2.1
V_2 (V)	3.9	3.9	2.8	3.1	3.0	3.8	4.4	4.1	4.1	4.4

Table 3

Piecewise Linearized Equivalent Circuit
Parameters for the Gate-Cathode Diode
Characteristic Curves for the
T7S7 Thyristor

Low Current
(≤ 160 mA)

Device Number	2	3	4	6	10	11	13	16	18	20
R_0 (Ω)	15.5	2.9	23.0	25.0	19.2	32.5	22.0	22.5	19.2	23.8
R_1 (Ω)	9.1	16.7	16.9	16.7	5.7	17.0	8.7	9.0	7.7	13.1
R_2 (Ω)		2.5	2.8	2.6		2.0	2.0	3.0	3.5	4.8
V_1 (V)	1.0	0.80	0.85	1.1	1.0	0.90	1.1	1.1	1.0	0.90
V_2 (V)		1.4	1.5	1.7		1.5	1.6	1.5	1.5	1.5

Only two breakpoints were obtained for Devices 2 and 10.

Pulsed High Current
(≤ 12 A)

Device Number	2	3	4	6	10	11	13	16	18	20
R_0 (Ω)	2.8	2.8	3.1	3.9	2.8	3.1	3.1	2.6	2.8	3.0
R_1 (Ω)	0.49	0.53	0.69	0.82	0.35	0.52	0.55	0.53	0.42	0.61
R_2 (Ω)	0.85	0.95	0.90	1.1	0.70	0.77	0.67	0.44	0.72	0.75
V_1 (V)	2.2	2.2	2.2	2.4	2.0	2.0	2.0	2.0	2.0	2.2
V_2 (V)	3.8	4.2	4.2	4.8	2.9	3.3	3.6	3.3	3.4	4.0

performed on the five T720-35 devices exhibiting no initial leakage current, on two T72H-40 devices, and all four 650PBQ devices.

Pulsed Characterization

Eighteen of the T7 devices were pulse characterized by switching the 100 μ s PFN. (T72H-45-6 and T72H-45-12, which did not block in the forward direction, were not used.) Representative current and voltage switching waveforms are shown in Figure 39; the current waveform was obtained by measuring the voltage across the load, and the voltage waveform was obtained at the anode, relative to the cathode, which was tied to common. The current rise and voltage fall times are shown on expanded time scales in Figure 40. The current rises to 750 A in 1.4 μ s (540 A/ μ s) and to its peak value of 1000 A in 4 μ s. The voltage falls in several stages: there is a relatively fast drop from 800 V to 600 V in around 100 ns, followed by a very rapid drop to around 160 V in 50 ns, an increase of some 20 V over another 50 ns, and then a slow decay lasting around 1 μ s, to the on value of several volts. The forward drop is at its final value after 2 μ s. The initial voltage drops are probably associated with the collapse of the electric field, and the rise and slower decay, with the spread of the plasma. After pulse characterization, the gate-cathode diode and blocking characteristics of these devices were

Figure 39. Typical switching waveforms for the 100 μ s PFN. The upper curve is the current pulse (250 A per large division); the flat line at zero is the voltage waveform, which falls very rapidly from 800 V. The horizontal scale is 20 μ s per large division.

1. The first part of the paper is devoted to the study of the properties of the function $f(x)$ defined by the equation $f(x) = \int_0^x f(t) dt$. It is shown that $f(x)$ is a constant function.

2. In the second part, we consider the function $g(x)$ defined by the equation $g(x) = \int_0^x g(t) dt$. It is shown that $g(x)$ is a constant function.

3. The third part of the paper is devoted to the study of the properties of the function $h(x)$ defined by the equation $h(x) = \int_0^x h(t) dt$. It is shown that $h(x)$ is a constant function.

4. In the fourth part, we consider the function $k(x)$ defined by the equation $k(x) = \int_0^x k(t) dt$. It is shown that $k(x)$ is a constant function.

5. The fifth part of the paper is devoted to the study of the properties of the function $l(x)$ defined by the equation $l(x) = \int_0^x l(t) dt$. It is shown that $l(x)$ is a constant function.

6. In the sixth part, we consider the function $m(x)$ defined by the equation $m(x) = \int_0^x m(t) dt$. It is shown that $m(x)$ is a constant function.

7. The seventh part of the paper is devoted to the study of the properties of the function $n(x)$ defined by the equation $n(x) = \int_0^x n(t) dt$. It is shown that $n(x)$ is a constant function.

8. In the eighth part, we consider the function $o(x)$ defined by the equation $o(x) = \int_0^x o(t) dt$. It is shown that $o(x)$ is a constant function.

9. The ninth part of the paper is devoted to the study of the properties of the function $p(x)$ defined by the equation $p(x) = \int_0^x p(t) dt$. It is shown that $p(x)$ is a constant function.

10. In the tenth part, we consider the function $q(x)$ defined by the equation $q(x) = \int_0^x q(t) dt$. It is shown that $q(x)$ is a constant function.

Figure 40. Current rise (a) and voltage fall (b) times on expanded time scales for the switching waveforms for the 100 μ s PFN. The upper photograph shows the current rise (upper curve, 250 A per large division) and the voltage fall from 800 V (lower curve). (The dashed appearance of the curves is the result of chopping.) The horizontal time scale is 2 μ s per large division. The lower photograph contains the voltage fall waveform; the vertical scale is 200 V per large division, and the horizontal scale, 200 ns per large division.

a.

b.

compared with the initial measurements to see if any deterioration resulting from pulsed operation had occurred; no changes were observed. It was found during the fast pulse stress that reproducibility of the results was a better criterion for degradation than a slow pulse recharacterization, so that this latter measurement was ultimately discontinued.

Single-Shot Stress

Devices T7S7-3, -4, -11, -13 and -20, and T72H-45-1, -2, -8, -10 and -18 were selected for single-shot stress at high dI/dt , in the 10 μs PFN. The first stress level was 1000 A/ μs (measured to 800 A); four turns were added to the 10 μs PFN inductor to slow the rise time. Figure 41a illustrates the chopped anode current, obtained by measuring the voltage across the load, and anode voltage waveforms for a T72H-45 device. (All single-shot current waveforms were obtained by measuring the load voltage.) The voltage is seen to go negative, to around -200 V; this is an artifact of the measurement, probably the result of ground currents, and was eliminated by wrapping the voltage probe lead around a balun coil (Figure 41b) six times. The waveforms in Figure 41b are typical for all the T72H-45 thyristors stressed; peak current was around 900 A. The leading edges of the waveforms are shown on expanded time scales in Figure 42. The dI/dt for the T72H-45 devices was

Figure 41. Anode current and voltage waveforms for the T72H at 1000 μ s: a) without balun; b) with balun. The upper traces in both photographs are the current waveforms (250 A per large division); the lower traces are the voltage waveforms, falling from 800 V. The horizontal scale in both photographs is 2 μ s per large division.

a.

b.

Figure 44. Leading edges of the current (a) and voltage (b) waveforms on expanded time scales for the T7S7 at 1000 A/ μ s (nominal). The vertical and horizontal scales for the upper photograph are 250 A and 200 ns per large division, respectively; for the lower photograph, 200 V and 50 ns per large division, respectively.

a.

1000 A/ μ s (Figure 42a), except for device T72H-45-8, for which dI/dt was 1060 A/ μ s. Voltage fall (Figure 42b) is very rapid, dropping from 800 V to 300 V in 50 ns, and decaying to the static forward drop (zero on this scale) in another 400 ns.

Representative current and voltage waveforms for the T7S7 devices at 1000 A/ μ s are shown in Figure 43. The voltage fall is slower here than for the T72H-45 (compare with Figure 41b), as can be seen in Figure 44b; in 50 ns, the anode voltage drops to 400 V, and has decayed only to 80 V after an additional 400 ns. The dI/dt in these measurements (obtained from the leading edge of the current waveform in Figure 44a) was only 800 A/ μ s, except for T7S7-13, for which dI/dt was 850 A/ μ s.

The dI/dt of the 10 μ s PFN was increased to 2000 A/ μ s by adding a shunt capacitance of 0.3 μ F at its output. Overall current and voltage pulse shapes were similar to those in Figures 41 (T72H-45) and 43 (T7S7). The leading edges of the current waveforms on expanded time scales are shown in Figure 45a (T72H-45) and 45b (T7S7). The corresponding values of dI/dt are 2285 A/ μ s (T72H-45) and 2000 A/ μ s (T7S7). The voltage fall for both types was similar, and is illustrated in Figure 46. It is to be noted that the voltage fall time for the T72H-45 has increased, the voltage after 50 ns being around 400 V and, after another 400 ns, around 30 V. The fall time for the

Figure 43. Representative current (upper curve) and voltage (lower curve) waveforms for the T7S7 at 1000 A/μs (nominal). The vertical current scale is 250 A per large division. The horizontal scale for both is 2 μs per large division.

[illegible]

Figure 44. Leading edges of the current (a) and voltage (b) waveforms on expanded time scales for the T7S7 at 1000 A/ μ s (nominal). The vertical and horizontal scales for the upper photograph are 250 A and 200 ns per large division, respectively; for the lower photograph, 200 V and 50 ns per large division, respectively.

a.

b.

Figure 45. Leading edges of the current waveform on expanded time scales for the T72H (a) and the T7S7 (b) at 2000 A/ μ s (nominal). The vertical and horizontal scales in both photographs are 250 A and 100 ns per large division, respectively.

a.

b.

Figure 46. Typical voltage fall on an expanded time scale for the T72H and the T7S7 at 2000 A/ μ s (nominal). The vertical scale is 200 V per large division, and the horizontal scale is 50 ns per large division.

T7S7 has decreased somewhat, the voltage decay being faster.

Thirty turns of the 10 μ s PFN inductor were shorted to obtain a dI/dt of 5000 A/ μ s. There was some distortion in the anode current pulse, as shown in Figure 47, which is typical of the anode current in all ten devices. This is probably the result of impedance mismatch. The leading edges of the current waveforms for the two devices are shown on expanded time scales in Figure 48. The values of dI/dt (to 800 A) are 3640 A/ μ s for four of the five T7S7 devices, the fifth, T7S7-17, having a dI/dt of 3480 A/ μ s. There was considerable variation in the values of measured dI/dt for the T72H-45 devices: 4200 A/ μ s (T72H-1), 4700 A/ μ s (T72H-2), 5300 A/ μ s (T72H-8), 5000 A/ μ s (T72H-10), and 4000 A/ μ s (T72H-18). Voltage falls on expanded time scales are shown in Figure 49. The shapes of the voltage fall curves have changed from those in Figures 42b, 44b and 46, and now appear similar to that of Figure 40b, the voltage fall obtained with the 100 μ s pulse at a low dI/dt (around 350 A/ μ s). The total decay times to the static forward values are more-or-less comparable, but the time delay, around 100 ns to 200 ns, occurs only at the lowest and highest dI/dt . It could be argued that the change in the voltage fall waveform is the result of damage occurring at the high dI/dt values used here. Blocking voltage, remeasured after stress, was not affected;

Figure 47. Typical anode current pulse for the T72H and the T7S7 at 5000 A/ μ s (nominal).

422 229

100

100

100

1. *Chlorophyll a* (Chl *a*)

Figure 48. Leading edges of the current waveforms on expanded time scales for the T72H (a) and the T7S7 (b) at 5000 A/ μ s (nominal). The vertical and horizontal scales in both photographs are 250 A and 100 ns per large division, respectively.

a.

b.

Figure 49. Typical voltage falls on expanded time scales for the T72H (a) and the T7S7 (b) at 5000 A/ μ s (nominal). The vertical and horizontal scales for the upper photograph are 200 V and 50 ns per large division, respectively; and for the lower photograph, 200 V and 100 ns per large division, respectively.

a.

b.

however, several of the devices (T7S7-3, T72H-45-8, T72H-45-18) used in the single stress measurements were used again in the repetitive stress experiments at around 2000 A/ μ s and the voltage fall results (Figures 45b, 47b, and 48) were similar to those observed at 5000 A/ μ s single-shot, so that the earlier results at 2000 A/ μ s were not reproduced.

It is also to be noted that, at comparable PFN drives, higher values of dI/dt are obtained for the T72H-45 than for the T7S7. It is possible that the difference is the result of package inductance (the T72H-45 has a somewhat larger diameter package), but is more likely the result of the interdigitation, and increased gate-cathode periphery, in the T72H-45.

The PFN leading edge dI/dt was increased by adding a 10 μ F shunt capacitance at its output, but the increased dI/dt of the anode current pulse (device T72H-45-18) did not change from its previous value, suggesting that the device dI/dt is either self-limited, or limited by parasitic series inductance in the package, fixture, and anode leads. The braided straps were replaced by an 0.4 Ω parallel-plate transmission line, but no change in the anode current dI/dt was observed. Inasmuch as no higher values of anode current dI/dt than 5000 A/ μ s could be obtained in the single-shot measurements in the 10 μ s PFN, they were discontinued and repetitive stress was begun.

Four T720-35 devices were tested single-shot in the 8 μ s PFN. Anode and trigger current turn-on times (measured at the cathode and gate, respectively) for two (35-27 and 35-29) were measured with respect to leading edge of the output pulse of the pulse generator. The timing between the anode voltage fall and anode current rise was also measured by examining the waveforms on the same time scale (triggering was obtained from the leading edge of the gate current pulse). V_{AK} and I_A for device 35-27 are seen to begin changing at nearly the same time (within 50 ns) in Figure 50a. A similar timing relationship is observed in Figure 50b, in which the anode current pulse was the common trigger. Here the delay between voltage fall and current rise is within 2 ns. This device was stressed for tens of single shots at a dI/dt of around 2300 A/ μ s and a peak current of around 860 A. (The dI/dt value given for stresses in the 8 μ s PFN are obtained by dividing the 10% to 90% current difference by the rise between the 10% and 90% values. In some cases the JEDEC standard value for dI/dt will be given parenthetically next to the 10% to 90% value.)

Device T720-35-29 was single-shot stressed with $dI/dt = 5700$ A/ μ s and I_A peak = 1320 A, using the gate current pulse shown in Figure 51a; the leading edge of the gate pulse is shown in Figure 51b. The corresponding anode voltage and current behavior are shown in Figure 52a, and

Figure 50. I_R and V_{AK} for device T720-35-27 to measure time delays: a) trace triggered by gate current; b) trace triggered by I_A . Horizontal scale for the upper photograph is 50 ns per large division, and for the lower photograph, 20 ns per large division. The vertical scale for both photographs is 200 V per large division (V_{AK} and 200 A per large division (I_A)).

a.

b.

1. The first part of the document is a list of names and addresses, which appears to be a directory or a list of contacts. The names are written in a cursive script, and the addresses are listed below them. The list includes names such as "Mr. J. H. Smith", "Mr. W. B. Jones", and "Mr. C. D. Brown".

Figure 51. Gate trigger pulse for device T720-35-29:
a) entire pulse; b) leading edge of pulse. The horizontal scale for the upper photograph is 2 μ s per large division, and for the lower photograph, 20 ns per large division. The vertical scale for both photographs is 4 A per large division.

a.

b.

Figure 52. V_{AK} fall and I_A pulse for device T720-35-29: a) entire pulse; b) leading edge of pulse. The horizontal scale for the upper photograph is 2 μ s per large division, and for the lower photograph is 100 ns per large division. The vertical scales are the same in both photographs; 200 A per large division (I_A) and 200 V per large division (V_{AK}).

a.

b.

the pulse leading edges in Figure 52b. When the gate pulse was reduced to 1 μ s in width (Figure 53a), no change in dI/dt value for the anode current was observed for the same PFN conditions. The gate current pulse width was next reduced to 350 ns (zero current to zero current), then to 250 ns (Figure 53b); no change in dI/dt was observed. If the pulse width is decreased to below around 200 ns, the value of dI/dt is reduced. The minimum gate pulse which could be applied to the device and still obtain turn-on triggering was around 80 ns (Figure 54). The peak gate current decreases to 9.2 A for this pulse width. The anode current pulse is similar to that illustrated in Figure 52a. The leading edges of the anode current rise and voltage fall for the minimum gate drive are shown in Figure 55; the dI/dt value here has decreased to less than 4800 A/ μ s. The voltage fall is also slower.

Current pulse delay times were measured with respect to the leading edge of the voltage pulse from the pulse generator. A 50 ns delay is caused by the switching time of IRF610 and length of coaxial lines used to the gate current (which becomes greater than zero at $t \sim 50$ ns). There is also a 2 to 3 ns delay between the time gate current begins to flow and current appears at the cathode. Current flows into the anode about 36 ns after gate current begins flowing out of the cathode, as seen in Figure 56. The leading edge of the gate current pulse is shown

 

Figure 53. Reduced gate trigger pulses: a) 1 μ s pulse; b) 250 ns pulse. The horizontal scale for the upper photograph is 200 ns per large division, and for the lower photograph, 100 ns per large division. The vertical scale for both photographs is 4 A per large division.

a.

b.

Figure 54. Minimum gate trigger pulse. Horizontal scale is 20 ns per large division. Vertical scale is 4 A per large division.

Figure 55. V_{AK} and I_A leading edges corresponding to minimum gate trigger pulse width. Horizontal scale is 100 ns per large division. Vertical scales are 200 A (I_A) and 200 V (V_{AK}) per large division.

Figure 56. Delay of I_A rise with respect to I_{GK} for device T720-35-29. Horizontal scale is 20 ns per large division. Vertical scale is 0.5 A (I_A) and 4 A (I_{GK}) per large division.

relative to the leading edge of the anode current pulse.

Single-shot stress of devices T720-35-22 and 35-26 were performed using anode current pulses 8 μ s wide and gate pulses 250 ns wide; these were similar to the pulses of Figures 51 and 53b, respectively. Stresses of 3900 A/ μ s and 1280 A were used for 35-22, and 5100 A/ μ s and 1300 A, for 35-26.

Two T72H-40 devices were single-shot stressed in the 8 μ s PFN with two gate pulse widths, 8 μ s and 250 ns. T72H-40-19 was tested after the capacitor fifth from the output of each PFN section was disconnected. This raised the PFN impedance slightly above the load impedance so that a slight undershoot (negative current) occurred in the anode current pulse (Figure 57a). The notch in the center of the pulse is the result of removing the capacitors. Peak current is about 1600 A. The leading edge of the current pulse is shown in Figure 57b; the rise time corresponds to 10,300 A/ μ s (15,400 A/ μ s). The voltage fall is also shown. V_{AK} drops to 600 V in about 20 ns, then decays to its "on" value of around 60 V during the pulse discharge. The decay time, which is not shown in the photograph, is around 450 ns. Gate pulse width around 450 ns did not appear to affect the current and voltage behavior.

Device T72H-40-16 was stressed in the 8 μ s PFN with results similar to those obtained in Figure 57. The stress

 

Figure 57. Typical I_A and V_{AK} waveforms for T72H-40 devices: a) entire I_A pulse; b) leading edge of I_A and V_{AK} pulse. Horizontal scales are 5 μ s per large division for the upper photograph and 50 ns per large division for the lower photograph. The vertical scales are 316.2 A per large division (I_A) and 200 V per large division (V_{AK}) for both photographs.

a.

b.

levels here were 9100 A/ μ s (13,400 A/ μ s) and 1610 A. Gate pulse width did not affect the results. This device was also stressed repetitively for 1 hour, then single-shot tested again; no change in dI/dt was observed.

The 650PBQ devices were tested single-shot in the 8 μ s PFN. Device 650PBQ-1 was triggered with the two gate drives shown in Figure 58; peak gate current was about 10.8 A. The anode current pulse was similar to that of Figure 57a except, for this device, the first negative current spike is larger. The leading edge of the anode current pulse is shown in Figure 59. There are two distinct regions of current rise, and two corresponding regions of voltage fall; these are probably the effect of the amplifying gate. The dI/dt level was 6500 A/ μ s (7100 A/ μ s), with a peak current of 1610 A.

The 650PBQ-X-2 device was single-shot stressed with an 8 μ s wide and 350 ns wide gate pulses. The narrow gate pulse, which has a peak current of 12.4 A, is shown in Figure 60. The narrow pulse has the minimum pulse width which would result in the same dI/dt level which was obtained with the 8 μ s gate pulse. Note that a harder gate drive (Figure 60) (width and peak current) was required for the main gate fired device, 650PBQ-X-2, than for the amplifying gate device, 650PBQ-1 (Figure 58a), for similar anode current pulses; that is, more triggering charge was required. The current rise and voltage fall are illus-

.

• • • • •

Figure 58. Gate trigger pulses for 650PBQ-1 device: a) narrow pulse; b) full 8 μ s pulse. The horizontal scale for the upper photograph is 50 ns per large division, and for the lower photograph, 1 μ s per large division. The vertical scale for both photographs is 4 A per large division.

a.

b.

Figure 59. Leading edge of I_A and V_{AK} for device 650PBQ-1. Horizontal scale is 100 ns per large division. Vertical scales are 316.2 A (I_A) and 200 V (V_{AK}) per large division.

Figure 60. Narrow gate trigger pulse for device 650PBQ-X-2. Horizontal scale is 50 ns per large division. Vertical scale is 4 A per large division.

trated in Figure 61. The curves do not show the structure of Figure 59; the voltage falls smoothly to around 80 V in about 500 ns, then decays slowly to around 15 V in 1 μ s. The anode current dI/dt is 10,100 A/ μ s (13,200 A/ μ s), with a peak current of 1580 A.

The second amplifying gate device (650PBQ-3) was tested single-shot in the 8 μ s PFN at a dI/dt level of 6400 A/ μ s (7500 A/ μ s) and a peak current of 1550 A; voltage and current behavior were similar to those of Figure 59. Two gate drives were used to obtain the same dI/dt level, an 8 μ s pulse and a 125 ns gate pulse; the peak current for both was around 10 A.

The delay time associated with 650PBQ-3 and 650PBQ-X-2 were also measured single-shot. Around 50 ns after gate current began to flow, anode current in the 650PBQ-X-2 device began flowing. (The minimum current which could be measured here was 0.1 A.) The anode voltage did not begin to fall until anode current had been flowing for 170 to 200 ns (voltage measurement sensitivity was 60 V). Anode current began to flow around 30 ns after gate current flow started in the 650PBQ-3 (current sensitivity was the same). The anode voltage began falling about 60 ns after anode current began flowing in this device. The device with the amplifying gate structure begins to turn on faster than the main gate device, but the amplifying gate apparently inhibits the rate of anode current rise.

Figure 61. Leading edge of I_A and V_{AK} for device 650PBQ-X-2. Horizontal scale is 100 ns per large division. Vertical scales are 316.2 A (I_A) and 200 V (V_{AK}) per large division.

The last device tested was the 650PBQ-X-4. Its electrical characteristics were initially good (no leakage current) but the forward blocking voltage dropped to about 580 V after it was inserted into the 8 μ s PFN. There was also a change in the gate-cathode diode characteristics: the low current part became more resistive, whereas the high current portion became somewhat less resistive. This device was therefore not stressed.

Repetitive Stress

Several measurements were made (on T7S7-2 and T72H-45-21) before the diode was replaced by the command SCR. Load mismatch (an increase in the load resistance caused by heating) increased the width of the anode current pulse; the increased pulse length, and undelayed charging, resulted in destructive latching in the two devices. Neither device blocked in either the forward or reverse direction after latching. The gate-cathode diode showed no deterioration in the failed devices; this structure is clearly not as sensitive to degradation as anticipated. (It is also worthwhile to note that the gate-cathode diode [T7S7-2] could be pulsed repetitively for one hour at 500 Hz, with the anode open, with no change in characteristics.) At this time, the diode was replaced by the command switch.

Devices T7S7-3, T7S7-6, T7S7-16 and T7S7-18, and

T72H-45-1, -2, -8, -10 and -18, were all stressed at 500 Hz. Devices T7S7-18, T72H-45-1 and T72H-45-2 were destroyed because of shorts in the load mount before any data were obtained; T7S7-16 and T72H-45-8 were also eventually destroyed because of load mount shorts. The load was finally rearranged into a transmission line configuration (Figure 62). To assure that enough devices were stressed to provide a sufficient sample size, thyristors which had been used in the single-shot stresses were reused in the repetitive stress measurements to replace new devices which had been lost through non-stress related events. The pulse shape of the gate trigger for the test thyristors changed somewhat from its shape in the single-shot measurements, but its peak current, leading edge rise time, and steady value remained essentially the same.

Device T7S7-6 was stressed at 500 Hz at a dI/dt (to 800 A) of around 2500 A/ μ s. (The dI/dt changed somewhat during the measurement because of load heating.) The anode voltage charging waveform is shown in Figure 63; the anode voltage increases as cosine t to its peak value (around 700 V in the 500 Hz measurements because of charging power supply limitations), switches rapidly to zero, and begins to increase again. A single anode current pulse is shown in Figure 64. The pulse distortion is caused by load mismatch and load inductance; this pulse was obtained by

Figure 62. Photograph of the load and mounting structure.

Figure 63. Anode voltage charging waveform (T7S7-6). The vertical scale is 200 v per large division, and the horizontal scale is 1 ms per large division.

Figure 64. Single anode current pulse at 2500 A/ μ s and 500 Hz (T7S7-6). The vertical scale is 250 A per large division, and the horizontal scale is 5 μ s per large division.

measuring the voltage across the load. The device was stressed a total of ten hours, with interruptions after one hour, two hours, and five hours of stress for blocking voltage and gate-cathode diode recharacterizations; final recharacterization was performed at ten hours, after end of stress. (This recharacterization protocol was used in all the 500 Hz repetitive stress measurements.) No changes in either characteristic were observed.

Device T7S7-16 was stressed for five hours at a dI/dt of around 1800 A/ μ s. The PFN was switched from 700 V; the peak anode current was around 1000 A. No changes in blocking voltage or gate-cathode diode behavior were observed in any of the recharacterizations.

Device T7S7-3 was stressed for ten hours at a dI/dt (to 800 A) of 2000 A/ μ s. No changes in characteristics were seen at any time. Figure 65 shows a single anode current pulse, and Figures 66a and 66b, the leading edges, on an expanded time scale, of the current and voltage fall pulses. (The anode currents in this and all the following measurements were obtained with the Pearson 411 current transformer.) The voltage fall here is similar to that of the 5000 A/ μ s T7S7 single-shot stress (Figure 49), and may be the result of damage during that stress.

One device, T7S7-10, failed (would not block) after 45 minutes of stress at 2600 A/ μ s, but this was probably the result of a load resistance change and subsequent

Figure 65. Single anode current pulse at 2000 A/ μ s and 500 Hz (T7S7-3). The vertical scale is 316 A per large division, and the horizontal scale is 2 μ s per large division.

The following table shows the results of the
 test of the null hypothesis that the
 population mean is equal to zero. The
 test statistic is calculated as follows:

$$T = \frac{\bar{X} - \mu_0}{\frac{s}{\sqrt{n}}}$$
 where $\bar{X}$ is the sample mean, μ_0 is the
 hypothesized population mean, s is the
 sample standard deviation, and n is the
 sample size. The test statistic is compared
 to the critical value from the t-distribution
 with $n-1$ degrees of freedom. If the test
 statistic is greater than the critical value,
 the null hypothesis is rejected.

Figure 66. Leading edges of the (a) current and (b) voltage single pulse waveforms on expanded time scales for T7S7-3 at 2000 A/ μ s and 500 Hz. The vertical and horizontal scales for the upper photograph are 316 A and 200 ns per large division, respectively; for the lower photograph, 200 V and 200 ns per large division, respectively.

a.

b.

device latch-on. A second device, T72H-45-10, failed during reverse blocking recharacterization after two hours of stress at 2000 A/ μ s. No leakage current was observed until the reverse anode voltage was at 50 V, when the thyristor failed catastrophically, no longer blocking in either direction. The device did not fail during dI/dt stress; otherwise it would not have blocked at all, or would have been leaky, but it may have been sufficiently damaged during that stress so that the additional stress during blocking voltage characterization would cause it to fail completely.

The remaining two T72H-45 devices, T72H-45-8 and T72H-45-18, were stressed at 2000 A/ μ s and 2600 A/ μ s, respectively, for ten hours in increments of one, one, three and five hours. No changes in blocking voltage or gate-diode characteristics were observed. The single pulse anode current waveform and the current rise and voltage fall, on expanded time scales, for T72H-45-8, are illustrated in Figures 67 and 68, respectively. The PFN is switched from 700 V and the peak anode current is 875 A. The voltage fall characteristics under these conditions are similar to those of the 5000 A/ μ s voltage fall (Figure 49).

After ten hours of stress at 500 Hz, T72H-45-18 was stressed for an additional 24 hours at 1 KHz. The PFN could be charged only to 500 V, and dI/dt was reduced to 1600 A/ μ s, because the charging power supply was limited at

Figure 67. Single anode current pulse at 2000 A/ μ s and 500 Hz (T72H-8). The vertical scale is 200 A per large division, and the horizontal scale is 2 μ s per large division.

Figure 68. Leading edges of the (a) current and (b) voltage single pulse waveforms on expanded time scales for T72H-8 at 2000 A/ μ s and 500 Hz. The vertical and horizontal scales for the upper photograph are 200 A and 200 ns per large division, respectively; for the lower photograph, 200 V and 500 ns per large division, respectively.

a.

b.

this frequency. The single pulse voltage fall is shown in Figure 69; its behavior is similar to that of the voltage fall in the 5000 A/ μ s single-pulse stress. The dip at the end of the trace is probably the result of load mismatch and device fixture inductance. The blocking voltage and gate-cathode diode characteristics were remeasured after 24 hours of stress and found unchanged from their original values. Stress had been reapplied for another 45 minutes when the load mount shorted and the device was destroyed, failing to block in either direction (but the gate-cathode diode characteristics were unaffected).

The T720-35 devices which were stressed single-shot were each subjected to repetition stress at about 4500 A/ μ s using the short gate pulse in the 8 μ s PFN at 150 Hz. Every device failed (forward leakage current) after two to three minutes of stress. T720-35-27 blocked only 560 V in the forward direction and its gate-cathode diode became slightly less resistive at low currents (< 1 A), and slightly more resistive at high current values (> 1 A). Catastrophic failure of the blocking voltage (forward and reverse) occurred for T720-35-29 after short repetitive stress. The high current gate-cathode diode was slightly more resistive after the failure. Device T720-35-26 ran at an anode voltage of 760 V for less than one minute before forward blocking failure (reduced to 480 V), whereas its reverse blocking was unchanged. The gate-cathode diode was

Figure 69. Single pulse voltage fall on an expanded time scale for T72H-18 at 1600 A/μs and 1 KHz. The vertical scale is 100 V per large division, and the horizontal scale is 2 μs per large division.

unchanged. The forward blocking voltage of T720-35-72 was also reduced to 750 V after a short stress at 150 Hz; reverse blocking was unchanged. The high current gate-cathode diode curve was slightly more resistive.

The final T720-35 device, -16, was stressed at 600 V before catastrophic failure (no forward or reverse blocking). The low current gate-cathode diode curve was slightly less resistive, and the high current G-K diode was unchanged.

T72H-40-19 was stressed for 1 hour at 770 Hz (period of 1.3 ms) with the anode voltage at about 780 V, as seen in the charging waveform of Figure 70a. The PFN charges up in about 600 μ s. In Figure 70b, the voltage fall following one discharge is illustrated. V_{AK} decays in about 700 ns to its "on" value of 60 V. The current waveform is similar to that shown in Figure 57, except that the peak is around 1400 A. The dI/dt was 3200 A/ μ s (4100 A/ μ s). The gate pulse was similar to that shown in Figure 53b. This device was then stressed for 1 hour at 800 Hz at 4800 A/ μ s (6200 A/ μ s) with a peak current of 1450 A; measured cathode temperature rose from 19 °C to 36 °C. The voltage fall was similar to that illustrated in Figure 70b. During the third hour of testing, the dI/dt was increased to 6300 A/ μ s (10,100 A/ μ s), with a peak current of 1520 A; the cathode temperature increased from 26 °C to 47 °C. All the voltage fall waveforms looked essentially the same, except that V_{AK}

Figure 70. Repetitive V_{AK} waveforms for device T72H-40-19: a) charging of PFN; b) discharge of PFN. The horizontal scale for the upper photograph is 500 μ s per large division, and for the lower photograph, 100 ns per large division. The vertical scale for both photographs is 200 V per large division.

a.

b.

but the device would not operate repetitively. The cathode temperature increased from 21 °C to 24 °C during this stress.

The last device tested was 650PBQ-X-2. It was stressed at 800 Hz for 25 minutes at a dI/dt of about 4600 A/ μ s (6300 A/ μ s); peak current was 1390 A. V_{AK} dropped to about 90 V in 600 ns. The current pulse is similar to that of Figure 57a. The dI/dt level was increased to 7500 A/ μ s (9600 A/ μ s) with a peak current of 1500 A. This was maintained at 800 Hz for 1 hour. The temperature rose from 18.8 °C to 58 °C. The voltage fell smoothly to a value of 80 V in about 500 ns. Finally, dI/dt was increased to its maximum value of 10,000 A/ μ s (15,600 A/ μ s) at 800 Hz for 1 hour. The peak current was 1560 A, and the final cathode temperature was 57 °C. The anode voltage, 780 V, fell to about 80 V in 480 ns. After the repetitive stress, the forward and reverse blocking voltages were found to be unchanged. The low current gate-cathode diode curve was slightly less resistive; the high current diode was unchanged.

Failure Analysis

The failure analysis performed here did not indicate any obvious failure mode for the failed (non-blocking) T72H-45, T7S7, T720, or 650PBQ devices when the packages were opened. No physical damage was seen.

CHAPTER VI

CONCLUSIONS

The difference in behavior between the center-fired and interdigitated structures indicates that the effect of the interdigitation is to keep the local heating at the junction between the p- and n-bases low enough to permit operation in a fast pulsed mode. The T720-35 devices that failed to operate repetitively probably failed because of local heating because no temperature increase was observed at the case. The interdigitated devices operated at peak currents up to 1600 A with average currents up to 96 A during the repetitive tests. Therefore, if the gate-cathode periphery is designed so that the initial local heating can be tolerated, then the thyristor structure should be able to handle high current, high di/dt switching.

One T72H-40 device was used in the measurement of delay times between current flows in the gate and anode, and the anode-cathode voltage fall. This measurement was also performed with two 650PBQ devices. The devices which had their amplifying gate structures connected apparently began turning on faster with respect to the gate pulse or sooner after gate current than the main gate device. However, the main gate device operated at the highest

repetitive dI/dt of any device type. Also, the device operated at a significantly higher level than the amplifying gate version. The involvement of the amplifying gate appears to reduce the initial delay time between anode current rise and anode voltage fall; however, it inhibits high rates of current rise which limit the device performance. The data indicate that a thyristor with only the main gate is required for high dI/dt switching.

The devices stressed in the 8 μs PFN were triggered with the full pulse width (8 μs) gate drive and a reduced gate width (250 ns nominal). In general, the two types of gate pulses had the same leading edges and maximum currents. If the width of the short pulse was reduced below around 250 ns, dI/dt at turn-on was reduced. There was a minimum gate pulse width, around 80 ns, below which the thyristor would not turn on, indicating that there is at least a minimum time during which gate charge must be injected if the device is to turn on, even at large gate currents. It is not certain that the current and pulse width are the critical parameters in themselves or whether the product of the two is the fundamental controlling parameter. The integral of the product, of course, is the total charge injected into the gate. By varying the gate current at several pulse widths, it should be possible to determine if the important parameter is current or charge.

Finally, all devices that failed catastrophically during testing were examined by opening the packages. No device that was examined showed any evidence of surface related failure nodes, supporting the argument that failure is caused by localized phenomenon, most likely thermal.

It is clear from the results that specified values of single-shot dI/dt are much too conservative, as are repetitive values, at least with respect to tens of hours of operation, if blocking voltage is considered to be the most sensitive criterion for damage. Under appropriate gating conditions, 1600 A has been repetitively switched at around 1 KHz at over 6000 A/ μ s. This high value of dI/dt can be attributed to the interdigitated gate-cathode structures found in inverter type thyristors (which have not been used at their actual safe operating limits). More highly interdigitated structures provided repetitive values of dI/dt up to 10,000 A/ μ s, a limit probably imposed by the test circuit itself. These results, conservatively extrapolated, indicate that repetitive peak currents up to around 10,000 A and dI/dt values in excess of 40,000 A/ μ s may be obtained with existing technology. Although no single thyristor as yet will block more than several kilovolts, still, a small series array of some six devices can be used to switch up to 10 KV. These values for dI/dt , current and voltage are comparable to those specified for some thyratrons, and, unlike thyratrons, semiconductor

switches have very long useful lifetimes, even under the high stress conditions described here.

However, several questions respecting these devices must still be addressed. First, the real current and rise time operating limits of highly interdigitated structures must be established and the role of the plasma spreading velocity must be determined. Next, design optimization must be considered; for example, recent results indicate that the amplifying gate structure found in inverter thyristors actually inhibit fast turn-on. Another very important issue is the gating arrangement required for the synchronized firing of a series array. This work has already shown that very narrow gate pulses can be used to trigger fast turn-on under certain conditions. These and similar issues require additional attention.