Plasma etching of AlN/AlGaInN superlattices for device fabrication

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We report a study of plasma etching of GaN, AlN, and AlN/AlGaInN superlattices for the processing of deep ultraviolet light emitting diodes. Etching was carried out using inductively coupled plasma of chlorine diluted with argon under reactive ion etching conditions. Using parameters selected for etch rate, anisotropy, and surface smoothness, we study etching of *n*- and *p*-type superlattices. The former etches at a rate of 250 nm/min, which is intermediate to that of AlN and GaN, while the latter exhibits a slower etch rate of 60 nm/min. Based on these studies, we prepare low-leakage *p*-*n* junctions and mesa light emitting diodes with peak emission at 280 nm. © 2002 American Institute of Physics. [DOI: 10.1063/1.1527986]

There has been considerable recent activity in preparing ultraviolet light emitting diodes (LEDs) and detectors, based on AlGaInN,¹ operating at wavelengths below 300 nm. Short period superlattices (SLs) based on AlGaInN/GaN and AlGaInN/AlGaInN^{2,3} have been used to overcome some of the difficulties of growing high quality *p*-type Al-rich layers. Our recent work has shown that diodes based on SLs of AlN/AlGaInN can be used to produce LEDs with light emission below 300 nm.⁴ This is accomplished using SLs of AlN and AlGaInN with well and barrier thicknesses of 1.25 and 0.5 nm, respectively. The average AlN mole fraction is very high in these structures, over 0.6, providing the necessary large optical gap, and the wells are heavily doped to produce a high average carrier concentration. An essential step in the fabrication of these devices is mesa etching. Etching by chlorine has become the most popular method for processing GaN-based devices.⁵ However, little work has focused on plasma etching for processing Al-rich device structures or superlattices.

We describe Cl₂-based plasma etching experiments for preparing wide band-gap devices from Al-rich AlGaInN. The GaN, AlN, and AlN/AlGaInN SLs studied were grown on silicon and sapphire substrates by gas-source molecular-beam epitaxy with ammonia as the nitrogen source. An AlN buffer layer (~40 nm thick) was first grown at 830–860 °C. A second buffer layer of GaN was then grown, with thickness of 1.35 μm. This layer is known to reduce the density of threading dislocations, which originate at the substrate-nitride interface.^{6,7} The *n*- and *p*-type SLs were grown next, with the wafer held at temperatures from 760 to 800 °C. Silicon and magnesium were used for *n*- and *p*-type doping, respectively. Details of the growth can be found elsewhere.^{8,9}

A commercial system was used for plasma etching with Cl₂/Ar gas mixture. Samples are mounted on 200 mm silicon wafers coated on the processing side by SiO₂. The baseline pressure of the etching system is 2×10^{-6} Torr. The gases are injected through a showerhead located ~100 mm above the sample. A high-density inductively coupled plasma

(ICP) discharge is generated by applying 13.56 MHz rf power to the water cooled inductive coil. The wafer electrode is powered separately by a 600 W generator (13.56 MHz) for reactive ion etching (RIE). As the ion energy and plasma density are effectively decoupled for the ICP-RIE system, uniform density, and energy distributions are transferred to the sample while keeping the ion and electron energies low.⁵ The substrate was cooled by He gas flowing from the electrostatic chuck, with no temperature control. We estimate the wafer temperature to remain below ~100 °C during our experiments. Etch depths were determined using a stylus profilometer. Scanning electron microscopy (SEM) and atomic force microscope (AFM) were used to determine etch anisotropy and surface properties.

To establish baseline etching parameters for the SLs, we etched test layers of GaN and AlN. Figure 1 shows etch rates versus plasma parameters of ICP power, RIE power, and pressure. The Cl₂ to Ar flow ratios were kept constant at 20–5 sccm in all cases. The etch rate of AlN is consistently lower than that of GaN. Etching is faster with higher ICP and RIE powers. The former is primarily due to increased chlorine radical concentration in the plasma, while the latter stems from enhancing the volatility of etch byproducts at the target surface. We use ICP power of 300 W and RIE power of 150 W for etching the SLs, because these parameters give us a high etch rate while producing anisotropic features and smooth etched surfaces. Figure 1(c) shows that the etch rate decreases with increased chamber pressure, particularly for GaN. This is plausibly due to reduced mean-free paths of the etching species. Consequently, a lower pressure is preferred; we use 8 mTorr for the SL etching experiments. The etch rate results in Fig. 1 are in good agreement with what has been previously reported.^{10,11} A typical SEM micrograph is shown in Fig. 2, verifying the desired anisotropic etching. Our AFM studies of etching induced roughness also show that these parameters lead to smooth postetch surfaces. For example, the rms roughness over the 10 μm×10 μm scan area is found to be ~4.2 nm for the *p*-type SL (to be discussed) following a 165 nm deep etch.

Using the above parameters, and prior to etching of LED

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FIG. 1. Etch rates measured for “bulk” GaN and AlN epilayers on silicon vs (a) ICP, (b) RIE power, and (c) chamber pressure. Fixed parameters are noted on each inset. The lines are to guide the eye.

structures, we measured the etching properties of *p*- and *n*-type superlattices. Hall measurements showed free carrier concentrations of $(0.7\text{--}1.1)\times 10^{18}\text{ cm}^{-3}$ and mobilities of $3\text{--}4\text{ cm}^2/\text{Vs}$ for the *p*-type SLs, and corresponding values of $3\times 10^{19}\text{ cm}^{-3}$ and $10\text{--}20\text{ cm}^2/\text{Vs}$ for the *n*-type SL samples. We found that the etch duration had an effect on the etch rate. AlN etched 58 nm for a 1-min-etch period, and 270 nm following a 2 min process. Similarly, *p*-type SLs etched 60 nm for the first 1 min of etching, and etched 330 nm for a 2 min etch. Buttari *et al.* report an etch duration dependence to the etch rate of AlGaIn and attribute it to the formation of a protective oxide at the surface.¹² To check this, we etched AlN for different times up to 3 min. We find that the AlN does not etch for the first ~ 45 s, after which a constant

FIG. 2. SEM image of the etched surface under our typical conditions of 300 W ICP power, 150 W rf RIE power, 20/5 sccm Cl₂/Ar flow ratio, and 8 mTorr pressure.

etch rate of 200 nm/min is established. We attribute the delay to aluminum oxide formed on the surface following growth. GaN showed no significant delay as the gallium oxides are more chemically reactive. The wafer temperature may also rise during the etching process due to free carrier eddy currents driven by the rf field,¹³ together with the effects of ion bombardment. Elevated temperatures accelerate etching through the kinetics of the chemical reactions and byproduct volatility. The *n*-type SLs etched 250 nm in a 1-min-etch period. This is intermediate to what we find for AlN and GaN layers, but approximately four times faster than what we have in *p*-type SLs.

The effect of doping type on plasma etching rates has been extensively studied in silicon.^{13–16} Two explanations for higher etching rates of *n*-type Si have been advanced. In the space-charge model of Lee *et al.*, the difference in etching rates is attributed to the presence of dopant ions in the near-surface depletion region.^{13,15} These dopant ions serve to attract Cl[−] ions present in the plasma to the surface via Coulomb interaction. *n*-type dopant ions clearly would function in this manner to enhance the Cl[−] adsorption. Mogab and Levinstein interpreted higher etching rates of *n*-type Si as originating from higher free electron concentrations in the material.¹⁴ As neutral Cl atoms reach the surface, they interact with the Si due to the high electron affinity of chlorine. Since electrons are more readily available in *n*-type material, this reaction rate will be enhanced over undoped or *p*-type layers. Since the neutral Cl and positively ionized Cl⁺ are in greater abundance than the Cl[−] ions in the plasma,^{11,17,18} we believe the latter model to be more plausible. The factor of ~ 4 selectivity of *n*-type etching over the *p*-type SL produces practical difficulties when etching a diode with the top *p*-type layer. This factor, and the temperature-induced etch period effect, amplify the risk of rapidly consuming much of the underlying *n*-type SL after completing the *p*-type layer etch in our devices.

The device structure used for our experiments is shown schematically in Fig. 3, with the typical SL properties also depicted. The *n*- and *p*-type SL is composed of alternating layers of AlN and Al_{0.08}Ga_{0.92}N with less than 0.01% of indium. A 10-nm thick SL active region (undoped), was sand-

FIG. 3. Schematic of the device stack and mesa architecture used for making the ultraviolet LED discussed here.

wiched between the *n*- and *p*-type SLs. For preparing the mesa LEDs, we used liftoff photolithography processing. 100-nm-thick Ni masks were deposited using *e*-beam evaporation. Ni is highly resistive to chlorine etching and permits preliminary electrical characterization measurements to be carried out without further processing. For device fabrication, the Ni is stripped off using a solution of HCl (37%) at 50–60 °C or HNO₃ and HF (10:1) at room temperature. *p*- and *n*-type contacts were made separately using *e*-beam evaporation and liftoff. Contacts to *p*-type SLs were made using 50 nm of Ni followed by 70 nm of Au. For electrical contact to *n*-type material, we used Ti/Al/Ti/Au stacks with total thickness 200 nm. High *p*- and *n*-type concentrations in as-grown layers make it possible to prepare Ni/Au and Ti/Al/Ti/Au ohmic contacts without high temperature activation anneals.

Typical electroluminescence and *I*–*V* curves from LEDs fabricated using these methods are shown in Fig. 4. Mesa diameters range from 120 to 400 μm. Turn-on voltages range between 3.5 and 4.0 V, and series resistances are ~90 Ω. The zero forward bias current is ~20 pA and leakage currents of 20–30 μA are found under reverse voltages of 15 V. The low leakage currents are consistent with high quality of etched mesa sidewalls. The devices were able to withstand dc current densities of 500 A/cm² at room temperature. Figure 4(a) shows the electroluminescence spectrum for this device, which exhibits the shortest emission wavelength that we are aware of (280 nm).

In conclusion, we have studied the etching parameters needed to fabricate mesa LEDs based on SLs of AlN/AlGaInN. The etching rates of AlN are ~1/3 those of GaN under identical conditions. This slower etch rate is found to dominate the etching of AlN/AlGaInN SLs, of both *n* and *p* type. Postetch sidewalls are vertical, and the etched surfaces are suitably smooth for contact formation. These methods allow us to make LEDs with extremely low emission wavelengths.

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FIG. 4. (a) Electroluminescence spectrum at dc current of 10 mA; (b) room-temperature current–voltage characteristics of a mesa LED.

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