INVESTIGATION OF ULTRA-HIGH SWITCHING FREQUENCY
TO REDUCE SIZE IN RAPID CAPACITOR CHARGING

by

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TABLE OF CONTENTS

ACKNOWLEDGEMENTS	ii
TABLE OF CONTENTS.....	iii
ABSTRACT.....	v
LIST OF FIGURES	vi
1. INTRODUCTION	1
2. THEORY AND DESIGN	3
2.1 Voltage Multiplier Cascade	3
2.1.1 40kV Charger Multiplier.....	5
2.1.2 50kV Charger Multiplier.....	5
2.2 Gate Driver and H-Bridge.....	6
2.2.1 40kV Charger H-Bridge.....	8
2.2.2 50kV Charger H-Bridge.....	10
2.3 Transformer.....	11
2.3.1 40kV Charger Transformer.....	12
2.3.2 50kV Charger Transformer.....	13
2.4 Optical Isolation.....	14
2.4.1 40kV Charger Optical Isolation	14
2.4.2 50kV Charger Optical Isolation	15
2.5 Power Supply	15
2.5.1 40kV Charger Power Supply	16
2.5.2 50kV Charger Power Supply	16
3. COMPUTER SIMULATIONS.....	18
3.1 Transformer Simulation	18
3.2 40kV Charger Simulation	19
3.3 50kV Charger Simulation	24
4. IMPLEMENTATION.....	27
4.1 Transformer Wrapping.....	27
4.2 Board Layout	28
4.2.1 40kV Charger Layout	28
4.2.2 50kV Charger Layout	33

4.3 40kV Charger Assembly	37
4.4 50kV Charger Assembly	39
5. RESULTS	41
5.1 40kV Charger Results	41
5.2 Transformer Results.....	52
5.3 Battery Supply	54
5.4 50kV Charger Results	56
6. CONCLUSIONS.....	65
REFERENCES	67

ABSTRACT

This project concerned itself with two different chargers, both based on the same principle designs but both having fundamentally different output and input requirements and goals. Both chargers were built using a full bridge setup that was MOSFET based utilizing frequencies of 187 kHz to 1MHz being examined. The modulated DC voltage is applied to a transformer and then a multiplier cascade is used to complete the final voltage increases. The 40kV charger had a requirement of 100-300V_{DC} input with a 40kV, 40kW, 1kJ output requirement in 10ms or less. The 50kV charger required a higher output voltage with a considerably lower input voltage requirement of 40-50V_{DC} and was required to operate repetitively at 200Hz. Transformer, voltage multiplier, circuit board layouts, and battery system designs and tests are all covered.

LIST OF FIGURES

2.1: Half-wave voltage multipliers [4].....	4
2.2: H-Bridge, Single Phase [2]	6
2.3: H-Bridge output [2]	7
3.1: 40kV Layout in PSpice	20
3.2: 40kV Output Simulation in 6ms	21
3.3: PSpice Layout of 2nd 40kV charger.....	22
3.4: 40kV simulation result.....	23
3.5: Energy calculation	23
3.6: 50kV charger schematic.....	24
3.7: 50kV charger simulated voltage output waveform.....	25
3.8: 50kV charger simulated current input waveform	25
4.1: 40kV charger schematic in PSpice	29
4.2: 40kV charger driver board layout.....	30
4.3: Multiplier board schematic	31
4.4: Multiplier board layout	32
4.5: 50kV Driver Board Schematic.....	34
4.6: 50kV Transformer and Multiplier Schematic.....	34
4.7: Transformer and Multiplier Layout	35
4.8: Multiplier Module Schematic	36
4.9: Multiplier Module Layout	36

4.10: Driver Board and Multiplier Setup (40kV).....	37
4.11: Input Capacitor Bank	38
4.12: Capacitor Load Isolated	39
4.13: Driver Board and Multiplier Setup (50kV).....	40
5.1: 5V input to a 0.16 μ F load.....	42
5.2: 15V input to 0.16 μ F load.....	42
5.3: 20V input to 0.16 μ F load.....	43
5.4: 25V input to 0.16 μ F load.....	43
5.5: 65V input to 0.16nF load in oil.....	44
5.6: 75V input to 0.16nF load in oil.....	45
5.7: 85V input to 0.16nF load in oil.....	45
5.8: 95V input to 0.16nF load in oil.....	46
5.9: 100V input to 0.16nF load in oil.....	46
5.10: 100V input to full system, 26.5kV output	47
5.11: 110V input to full system, 30kV max output.....	48
5.12: 20V Input, 100ms	49
5.13: 30V Input, 100ms	49
5.14: 40v Input, 100ms	50
5.15: PWM and gate driver output with noise	51
5.16: PWM and gate driver output with erratic duty cycle.....	51
5.17: Transformer 30V Input, 4.5kV Out	53
5.18: Transformer 40V Input, 6kV Output	53

5.19: Lithium Ion Battery Test of 2.95V at 250mΩ Yielding 11.8A.	54
5.20: Lead Acid Battery Test of 10.4V at 150mΩ Yielding 69A.	55
5.21: 10V input, 1 multiplier.....	56
5.22: 20V input, 1 multiplier.....	57
5.23: 35V input, 1 multiplier.....	57
5.24: 35V input, transformer waveform	58
5.25: 10V input, 2 multipliers	59
5.26: 20V input, 2 multipliers	59
5.27: 35V input, 2 multipliers	60
5.28: 35V input, 2 multipliers, transformer drop	61
5.29: 25V battery input, 2 multipliers	62
5.30: 25V battery input, 3 multipliers.....	62
5.31: 25V battery input, 4 multipliers.....	63
5.32: 25V battery input, 5 multipliers.....	63
5.33: 25V battery input, 6 multipliers.....	64

CHAPTER 1

INTRODUCTION

High voltage applications of pulsed power are many. Obtaining high voltages in compact packages has been a major focus of research and industry. Transformers are limited in size by the frequency of the input voltage, in general the higher the switching frequency the smaller you can make your transformer. In order to reduce the transformer size one must utilize a high switching frequency. Thyristor devices can handle considerable currents, but limitations on their switching speed, due to having to reverse the current to turn them off, prevent their use in rapid chargers. Insulated gate bipolar junction transistors can handle considerable current, but the switching speed still leaves much to be desired with a maximum switching frequency in the 30's to 40's of kHz. This leaves MOSFET devices alone as a practical choice for higher speed switching applications. The project itself built two different chargers, both of which used similar modulation techniques. Both chargers were built using a full bridge setup using MOSFETs as it allowed for a less complex transformer design compared to a push-pull or resonant based system. A multiplier cascade is used to complete the final voltage step up as stepping a voltage up by a factor of 2, 3, or 4 is relatively simple to do compared to having to step up to a very high voltage on a transformer alone.

The two charger setups had different current and voltage requirements and as such had to be designed separately. A 40kV charger with a 100-300V_{DC} input with a 40kV, 40kW, 1kJ output needed different considerations in transformer and bridge design

compared to a 50kV charger, that had a lower input voltage requirement of 40-50V_{DC} that was required to operate at 200Hz.

CHAPTER 2

THEORY AND DESIGN

To increase the voltage from the low value to the high value, several methods were investigated. Using a transformer alone would be impractical due to the sheer volume and incredible winding insulation required to prevent breakdown between secondary coils when wrapped on the transformer core. It was determined that a transformer could step the voltage up to moderately high voltages and then a voltage multiplier could double or triple the voltage with little effort. Combining the multipliers in series allowed for even higher voltages to be obtained with minimal effort.

2.1 Voltage Multiplier Cascade

Voltage multipliers are simple and effective ways of raising the output voltage when only small output currents are needed. A Villard multiplier is the basis for the entire device [2]. A single Villard multiplier is formed by a single diode and capacitor forming a half wave rectifier as shown in Figure 2.1(a). Combining two identical multipliers in series yields the Greinacher multiplier configuration shown in Figure 2.1(b). One capacitor is charged on the positive half cycle of the input voltage and the other is charged by the negative half cycle [2]. Both capacitors are charged in parallel to the same voltage. The output at the load has the capacitors in a series configuration and the output voltage is double that of the input voltage.

For no load:
 $PIV = 2NA = 2V_o$
 $\langle V_L \rangle = NA = V_o$
 $V_{L\text{ peak}} = 2NA = 2V_o$

(a) Villard Circuit [17]

For no load:
 $PIV = 2NA$
 $\langle V_L \rangle \approx 2NA \approx V_{L\text{ peak}}$

(b) Greinacher Circuit [17]

Figure 2.1: Half-wave voltage multipliers [4]

As each capacitor is charged to the input voltage, cascading multiple setups in series with each other can yield extremely high voltages without any kind of complex circuitry. For each Greinacher cascade, twice the input voltage is added to the output. The expression for the output voltage is shown in equation 2.1.

$$V_{out} = N * 2 * V_m \quad 2.1 [4]$$

where N is the number of Greinacher stages. Each component of the multiplier setup needed to be able to operate at the input voltage from the transformer. High Voltage Component Associates Inc. manufactures a high voltage ultra fast recovery diode (part number UX-FOB). Some of the specifications for the UX-FOB include reverse voltage

hold off 8kV, a peak current of 20A for 8.3ms with a sustained current approaching 200mA, and a recovery time of 50ns. This fast recovery time would be more than adequate for megahertz range switching. Since the rated reverse voltage was 8kV, a maximum of 8kV input voltage from the transformer per diode could be used. The diodes would also drop a maximum of 14V_{Forward}.

2.1.1 40kV Charger Multiplier

The 40kV charger utilized 6 sets of 4x multiplier cascaded in series. With a transformer providing 2kV input to each, multiplied to 8kV on the output and then cascaded in series, the final output voltage would theoretically be 48kV. When the diode losses were factored in (14V per device and 24 devices) the output voltage would be closer to 47.6kV. As the device needed to operate quickly, it would not necessarily need to charge to the full 48kV and time could be saved in the charging scheme. For an output of 8kV, a single diode was all that was needed in the multiplier.

2.1.2 50kV Charger Multiplier

The 50kV charger would require 2 coils from the transformer and so only 2 sets of 6x multiplier cascades were needed. For an input voltage approaching 6kV and the output of each multiplier yielding 12kV, the obtainable output voltage would be close to 72kV. This would require doubling of components to handle the voltage. Each capacitor would have a second one in series to handle 12kV total, and another two in parallel to bring the capacitance value up to 1nF. The diodes would not immediately require doubling to handle the voltage as 6kV falls under their operating range, but if the input

voltage ever increased, the need for doubling of the diodes will become obvious. The current design took this into account and doubled each diode in the multiplier cascade. This made for a more robust device for future expansion, for instance, if a higher input voltage to the multiplier of 12kV was used, the final output voltage could yield as much as 144kV.

2.2 Gate Driver and H-Bridge

A full bridge topology was chosen to accomplish DC-AC conversion. The input of the bridge is a constant voltage V_{DC} while the output of the bridge is a square wave with maximum value of V_{DC} . Full bridges consist of two output legs A and B with a set of switches and diodes for each leg. With the transformer coil joining the output of the two legs an H-bridge is formed, as shown in Figure 2.2 in an example of a DC motor drive circuit.

Figure 2.2: H-Bridge, Single Phase [2]

Since the device would be operating with a bipolar PWM switching signal to achieve a positive and negative output voltage wave, the control signals to the switches in

one leg are such that the two switches never come on at the same time. This prevents shorting to the input supply [2]. Referencing Figure 2.2, we let T_{A+} and T_{B-} be switch pair A and T_{A-} and T_{B+} be switch pair B. The switch pairs alone control the magnitude of the output voltage as when switch pair A is on and switch pair B is off, the output voltage is a positive V_d while conversely when switch pair A is off and switch pair B is on, the output voltage is a negative V_d . The percentage of the switching period that a device is on is called the duty cycle and is defined below in equation 2.2.

$$D = \frac{t_{on}}{T_{period}} \quad 2.2 [2]$$

The duty cycle of the switching pairs determines the shape of the output waveform. If one pair is on for a longer percent of the switching cycle than the other, the output waveform will reflect this, as shown in Figure 2.3. In the figure, the control for leg A leaves the switched pair (T_{A+} and T_{B-}) on for considerably longer than the control signal for B, resulting in the unbalanced square waveform.

Figure 2.3: H-Bridge output [2]

In order to allow equal time for each capacitor in the multiplier to charge, a 50% duty cycle will be used. With frequencies approaching 500 kHz to 1MHz to be explored, this left IGBTs to be an unrealistic solution for the switching pair devices and lead to a MOSFET approach for the switches in the bridge.

2.2.1 40kV Charger H-Bridge

The gate driver system for the 40kV charger needed to be able to drive a MOSFET that was capable of handling between 100V_{DC} and 300V_{DC}. The choice of MOSFET fell to Semikron's SKM253B020 N channel enhancement mode MOSFET based half bridge module. The 253B device was capable of drain to source voltages of 200V with maximum sustainable drain current of 250A and 750A pulsed for 1ms possible. The documentation from Semikron listed the rise and fall times of the device at 100ns and 250ns, respectively. The delay times for on and off at 100ns and 750ns, respectively, with a drain current value of 150A, and all the while maintaining a low drain to source resistance of 8.6mΩ max. Using these values it was estimated that 833 kHz would be the maximum reliable frequency at which to operate the device.

Once the MOSFETs were decided upon, the decision to drive them needed to be made based on current and charge requirements. As such, the required charge to turn on the device needed to be calculated. The relationship between charge, voltage, and capacitance is shown below in equation 2.3.

$$C_{gate} = \frac{Q_{gate}}{V_{gate}} \quad 2.3 [3]$$

Using a V_{GS} of 15V and determining C_{gate} to be 35.5nF from the specifications sheet the required charge was calculated to be 532nC. When applied for 1us the input current needed to switch the MOSFET on and off was calculated to be 532mA. For a more conservative capacitance, which takes into account the miller capacitance of the device, of 50nF, the value was found to be 738mA. A maximum current draw was calculated by using equation 2.4 and was found to be 2.66A.

$$I_{max} = \frac{Q_{gate}}{t_{d(on)} + t_{rise}} \quad 2.4 [3]$$

The DEIC420 MOSFET driver, manufactured by Directed Energy Inc, was chosen due to its ability to drive MOSFETs at speeds of up to 45MHz with sourcing and sinking currents of up to 20A. A minimal output delay time of 35ns with 4ns rise and fall times were also part of the device's specifications.

Once the gate drivers had been chosen it was necessary to decide on a chip to drive them. Chosen was Texas' Instruments UC1825 PWM controller which is optimized for high frequency switching power supply applications. The device had a minimal propagation delay of 50ns and switching frequencies of up to 1MHz. Voltage and current monitoring pins were part of the device's feedback system, which allowed the device to be shut down should an over voltage condition occur or too significant of current be drawn from the power supply. In order to utilize the current monitoring features, current sense resistors were placed in series with the MOSFET bridge right above ground that would apply a voltage signal to the pin of the driver. The resistors chosen were Caddock MP916 10mΩ which could dissipate 30W and were a low

inductance design. Two of these were placed in parallel to achieve a $5\text{m}\Omega$ overall resistance that would yield 0.5V when 100A flowed through them. The output of this resistor pair is fed into a non-inverting amplifier with unity gain for isolation.

2.2.2 50kV Charger H-Bridge

With a lower input V_{DC} value of 40V for the 50kV charger, the MOSFET requirements needed to be re-thought. Much smaller devices could now be considered and would be easier to obtain due to the lower input voltage. The device chosen was the IXYS FMM300-0055P which is a single phase leg topology MOSFET package. It is able to sustain 300A at 55V with an even lower drain to source resistance of $3.6\text{m}\Omega$ max. Rise and fall times were 50ns and 40ns respectively while the delay time for on and off states were 25ns and 70ns respectively. Using these values a maximum theoretical attainable frequency of 5.4MHz is potentially available, well above the frequency exploration of this project.

To drive the device, values needed to again be calculated to determine current draw on the gate. The gate charge was specified as 172nC . Using a V_{G} of 12V and the rise and delay times the maximum current was calculated out to be 2.23A using equation 3 that was used in the 40kV charger. The power dissipated in the gate at a frequency of 350 kHz was calculated to be 0.722W and the equation used to calculate it is given in equation 2.5 below.

$$P_{\text{gate}} = Q_{\text{gate}} \cdot V_{\text{gate}} \cdot f_{\text{switch}} \quad 2.5 [3]$$

A gate capacitance of 14.3nF was calculated using the values from the specification sheet as well. The average current the supply would have to provide was calculated to be 60mA. The equation used is shown below as well.

$$I_{avg} = Q_{gate} \cdot f_{sw} \quad 2.6 [3]$$

The gate driver chosen to drive the MOSFET was the Maxim IC MAX4420, capable of translating TTL/CMOS input logic to high current (6A) and higher voltage (18V) outputs. The device also possesses minimal delay and rise/fall times of 40ns and 25ns, respectively. Since the device has an 8 pin dip footprint, putting the device on a board was considerably easier and smaller as footprint space was shrunk compared to the DEIC420.

The PWM controller chosen was the SX28 made by Ubicom. It is a RISC based modified Harvard architecture programmable communication controller. The device operates at 50MHz and can perform calculations at a great rate of speed. This device was placed on its own board and would be connected fiber-optically from the main driver board to the processor board to further isolate the device from potential noise interference caused by the gate driver.

2.3 Transformer

While the voltage multiplier would be increasing the voltage to its final value, a transformer will be used to allow the voltage to be stepped. This allows keeping the number of the multipliers to a few stages which in turn reduces charging time. As voltage multipliers increase the output voltage with respect to ground, the grounding

design and transformer secondary coils needed careful insulation techniques to ensure safety of the device and proper operation [4]. Proper design of the transformer would be needed also as the device would be pulsed at high frequencies. The pulsing of the transformer has the advantage of temperature rises being able to be neglected and since the transformer would only operate for a short time period, the temperature would not be able to rise as quickly as if it were operated continuously. As the inductance and turns squared are proportional to each other, minimizing the number of turns will in turn minimize the inductance of the coils. This is critical to achieving fast rise-times for a high frequency transformer to operate properly. Size is a major contributing factor in the design of the transformer, utilizing multiple cores to potentially reduce the leakage inductance is not an attractive option due to the increased weight and volume of the transformer that would be added [5].

2.3.1 40kV Charger Transformer

The input of the 40kV charger was going to be less than 200V. Limitations of the actual MOSFET devices would limit the applied voltage to no more than 175V to operate the devices safely. Using a conservative ratio of 1:10 would step the voltage up to 1750V and the 2-stage multiplier would then quadruple it giving a final voltage of 7kV. A ratio of 1:11 or 1:12 at an even lower voltage of 160 or 145 would also yield similar final output voltages while minimizing the input voltage to the system. Multiple taps on the order of 6 would need to be used to apply the output voltage to multiple cascade multipliers to achieve the 40kV output requirement. In order to handle the high current, heavy gauge wire would need to be used and the wire width would need to be calculated

to determine maximum possible size. The ferrite materials 3F3 and 3C90 were recommended for the frequency ranges [1] and would be simulated by computer software to determine how effective they would be at the specifications of the project. Both cores listed a maximum flux density of 450mT. Initial calculations were performed to determine the frequency and number of primary turns to prevent the device from saturating. Equation 2.7 below is used for calculating the flux density with a square wave input, where B_{peak} is the peak flux density, U is the voltage in Volts, f is the frequency in Hz, A_e is the effective area obtained from the specifications sheet of 368mm² and N is the number of turns.

$$\hat{B} = \frac{0.25 \cdot \hat{U} \cdot 10^9}{f \cdot N \cdot A_e} \quad 2.7 [1]$$

Using a 175V input, a frequency of 200kHz, and aiming for a single primary turn, it was determined that the B_{peak} was equal to 594mT, above the given value of 450mT. Three turns yielded a much easier to manage 195mT. A 3:30 wiring ratio was initially chosen as a result. Using an ETD59 core of 41.2mm width, the maximum diameter of wire with 0.15 inches overall clearance was 0.049 inches. This is a match with AWG-16 gauge wire.

2.3.2 50kV Charger Transformer

The input voltage requirements having been changed from the 40kV charger required re-thinking on how to setup the new charger. A transformer with a turns ratio of 1:150 allowed the 40V to be stepped up to 6kV quite easily which would allow a 36kV output at the end of a 3-stage multiplier which reduced the number of taps on the

transformer to 2 from 5. With 40V being a much lower input voltage and the operating frequency at 350 kHz, the peak flux density was calculated out to be 77mT. It was desired that the secondary coils take up as little space as possible with minimal exposure of copper to prevent breakdown between the high and low voltage side. One hundred and fifty turns would not practically fit in the bobbin, so a 75-secondary turn wrapped around twice was chosen as a starting base. With an ETD59 core width of 41.2mm and making provisions for a ¼" of clearance on one side to isolate the coils from the outside, it was calculated that the wire diameter could be no more than 0.018 inches. Reading the wiring gauge charts shows a wire gauge of AWG27 would be sufficient. AWG26 with a diameter of 0.016 inches was selected as it was more readily available. AWG28 with a diameter of 0.014 inches was also selected as an alternative.

2.4 Optical Isolation

In order to protect the sensitive gate driver circuitry from the high voltage and current of the MOSFET and multiplier side, optical isolation needed to be used. To actually be useful in the system the device needs to have very fast switching abilities that complement the MOSFET and gate driver systems and must have a minimal propagation delay time between the input and the output.

2.4.1 40kV Charger Optical Isolation

The HCPL-3120 device was chosen to optically isolate on the 40kV charger. This device was chosen due to its minimal propagation delay, on the average of 300ns. The device's maximum switching time was 500ns which leads to a maximum of 2MHz

switching operation ideally. The device also has a wide supply voltage range of 15-30V_{DC} with a required current input of 5mA. With the wide supply voltage range and V_{OH} characteristic of (V_{CC}-3), it was a decent match for the UC1825's output voltage of 15V.

2.4.2 50kV Charger Optical Isolation

Due to the different set of requirements of the gate driver circuitry of the 50kV charger and advances in isolation technology, a different optical isolation device was chosen. The HCPL-7710 CMOS optocoupler was chosen due to its 40ns max propagation delay and ability to fit with the CMOS logic that was used in the gate driver circuitry.

2.5 Power Supply

In order to power the system, different power conditioning needed to be taken into account for the performance of the system and board layout. In order to make up for the lack of a high side driver, each high end MOSFET needed the driver to operate as a high side. This means that the voltage applied to the gate to turn on the MOSFET needed to be applied with respect to the drain of the MOSFET rather than the ground reference of the module, which would be with respect to the drain of the low side MOSFET. In order to accomplish this, a DC to DC conversion method was utilized. In order to compensate for delays in the conversion devices which would result in a bridge that might not keep one MOSFET in the same half bridge off at all times one and could potentially short out

one of the half bridges and therefore reduce the effectiveness of the charger, all four MOSFET devices were optically isolated and utilized DC-DC conversion.

2.5.1 40kV Charger Power Supply

In order to decide on which conversion device to use, the total current and voltage needed to be taken into account. With the current required to turn on the MOSFET devices calculated out to be 738mA average with a maximum current of 2.66A, a little extra was given to the device to prevent any potential problems. The device settled on was C&D Technologies VKA60LS15 24V_{in}, 15V_{out}, 60W DC-DC converter. It was chosen due to its high efficiency of 88%, convenient square size, high power output and high input to output voltage isolation of 1.5kV over 2 seconds. The device also has internal circuitry that responds to changes in the load within 100μs. The device was rather large with a width of 2.28 inches and a length of 2.40 inches, but it was more than adequate to power the gate drivers. Heat sinks were recommended due to potential heat increases from power losses which in turn increased the size of the device, but they were never used as the system was to operate as adiabatically as possible to reduce the size.

2.5.2 50kV Charger Power Supply

With the considerably lower gate charge of the 50kV charger, the current needed to run the device was also a considerably lower 60mA. This opened the door for considerably smaller devices now that the power needed was lower. With the power needed approaching 1W sustained, a higher wattage was chosen to alleviate stress on the device. The jump to the 15W C&D Technologies NPH15S2415i was made due to

limitations in power output from previous family sizes of 1-2W and no change between a 10W and a 15W in size. The size was considerably smaller than the VKA60 series with a width of 1.97 inches and a length of 0.98 inches. The device had similar properties to the VKA60 series with 1.5kV isolation between input and output, 87% average efficiency, and regulatory controller circuitry.

CHAPTER 3

COMPUTER SIMULATIONS

Computer simulations served as proof of concepts before any actual circuits were ordered or built. With the simulations design areas that needed to be addressed could be found and taken care of on the first run through rather than on a second iteration.

3.1 Transformer Simulation

In order to gain a better understanding of the transformer needed to be built for the 40kV charger, computer simulations were utilized to determine parameters such as wire thickness and wire pattern. Ansoft's PExprt 5 was the program used in this case. An ETD59 core and the 3F3 and 3C90 core materials were put into the program to determine the optimum wire wrapping geometry. The 3F3 core material was chosen as it has an upper operating frequency of 1MHz with a sharp rise in losses at frequencies above 2-3MHz [1]. Since the voltage step up range was from 200V to 2kV, a simple N_1/N_2 ratio of 10 was needed. The maximum value that the program would allow for power was 20kW which was roughly half of what the goal for the project was. Switching frequency was set at a variety of frequencies from 150 kHz to 1MHz to determine changing geometries based on frequency while the duty cycle was set at 48% which gave 4% overall dead time. The maximum allowed temperature rise was set to 500°C.

The wiring geometry of the transformer was returned by the program to be 3 coils with 3 turns each on the primary side of 12-gauge wire with 32 turns of 16-gauge wire on

the secondary side with a temperature rise of 435°C. The temperature rise would be neglected as the transformer would be a pulsed application that the program was not able to factor in. Since the program itself would not simulate multiple taps the specifications were changed to simulate 12kV output with the remaining parameters being kept the same as the previous simulation. The simulation showed that the geometry would fit in the device.

3.2 40kV Charger Simulation

The 40kV charger was the first to be simulated using OrCAD PSpice 9. The H-bridge was simulated using an opening and closing switch with the impedances set to 1MΩ for open and to the SKM253 drain to source resistance of 8mΩ obtained from the datasheet. A 200V_{DC} was used for the input voltage. The PWM signal that would drive the switches was obtained by creating two pulse voltage sources and setting them out of phase with each other. The diodes used in the multipliers were custom models with a breakdown voltage allowed to be set that were obtained from Dr. Giesselmann. This setup would simulate the environment as close as possible despite not having identical models to the UX-FOB diode and SKM253 MOSFET half bridge. Inductance of 0.5μH was added to simulate the line inductance on the output of the transformer for each secondary tap. The transformer was modeled as a pair of coupled inductors which allowed for multiple taps to be simulated. The coupling was chosen to be 0.999 initially for proof of concept. After the inductors the multiplier cascades were added in sets of 2

in series and 5 overall cascades setups. These were to charge a 1uF load. The charger simulation layout is shown below in Figure 3.1.

Figure 3.1: 40kV Layout in PSpice

When simulated for 10ms the device was found to perform adequately and operate within 6ms. The resulting output waveform is shown below in Figure 3.2.

Figure 3.2: 40kV Output Simulation in 6ms

The simulation was redone later to compensate for a lower frequency and as such required two transformers with 3 secondary taps each. The input voltage was multiplied by 10 and then quadrupled with 6 cascade setups in series. The PSpice layout is shown below in Figure 3.3.

Figure 3.3: PSpice Layout of 2nd 40kV charger

This setup was also modified to include the capacitor bank from which the voltage was being drawn, the inductance from the lines of the capacitor bank, the on-board snubber capacitors, and the inductance between the MOSFETs and the transformer line. The simulation results are shown below in Figure 3.4, and the energy calculation is shown in Figure. 3.5.

Figure 3.4: 40kV simulation result

Figure 3.5: Energy calculation

3.3 50kV Charger Simulation

Using a similar method and parts as the 40kV charger, the 50kV charger was simulated in Cadence PSD 14.2. The PSpice schematic is shown below in Figure 3.6.

Figure 3.6: 50kV charger schematic

The switched load on the output of the charging capacitor is to simulate the effects of charging and discharging the device 200 times a second. The output waveform is shown below in Figure 3.7. The simulated output current of the device is shown below in Figure 3.8. The current was found to be within a range of 70-80Amps, which is within 15-25% of the calculated current of 62.5Amps.

Figure 3.7: 50kV charger simulated voltage output waveform

Figure 3.8: 50kV charger simulated current input waveform

The results of the simulation were within close range of calculations and gave more of an understanding of which parameters would need to be modified and how they

would affect the system. Most importantly it was found that the inductance between the MOSFET and the transformer primary coil needed to be kept as small as possible as changes to the value by more than an order of magnitude would have devastating effects on the rise time of the system. In order to have minimal rise time an inductance value of 50nH or less needed to be obtained.

CHAPTER 4

IMPLEMENTATION

4.1 Transformer Wrapping

Transformer wrapping for the 40kV charger followed the recommendations of PExprt with 12-gauge litz style wire for the primaries and 18 gauge wire for the secondaries. The secondary taps started at one side and were wound for 33 turns. Each transformer bobbin would yield 6 sets of 33 to make 3 coils of 66 turns each. Then insulating tape was applied to prevent breakdown between different separate layers. Permacel P-222 family tape was used to provide the insulation between the coils. The tape has a 2mil thick polyimide film layer for a 3.75mil overall tape thickness. The high dielectric strength of 13,000V and insulation resistance of $1 \times 10^6 \text{ M}\Omega$ provides for protection against breakdown as the difference between layers would approach 2kV. Each coil is soldered to every other pin to prevent breakdown between them. Due to limitations of pin space, the last secondary coil was forced to be soldered next to the previous secondary pin. Care would need to be taken when the board was assembled to prevent breakdown between the two coils as the potential difference between them would be 8kV due to the multiplier. This was helped as the ends of the transformers were covered in heat shrink tubing from inside $\frac{1}{2}$ " of tape all the way until they reached the pin for soldering.

The 50kV charger transformer was built using the same principles, except that it used a single transformer with 24 gauge wire and 4 sets of 75 turns to yield two coils with 150 turns. With the even greater voltage difference between the two coils, two layers of

tape were applied between the first two sets of 75 and the last two sets of 75. The coil positive and negative wires were placed 10 pins apart from each other on each end of the footprint as well to prevent breakdown. Litz wire was used to form the primaries on the second design as well.

4.2 Board Layout

Board layouts for both chargers needed to be taken seriously to prevent stray inductance and capacitances from interfering with the output of the PWM signal as the devices were operating at 100's of kHz. The layout would need to be treated as an RF system with multiple ground and source planes trying to eliminate as much unintended noise from other devices on the board and from the test equipment itself as possible.

4.2.1 40kV Charger Layout

The final schematic of the 40kV charger is shown below in Figure 4.1. The complete gate driver layout is shown below in Figure 4.2. Due to the higher input voltage of the 40kV charger, the MOSFET and gate drivers took up considerable amount of space on the board as well as the DC-DC converters required to power them. The 8 snubber capacitors needed also took up a good portion of the board layout as well. This lead to needing to place the voltage multiplier cascade on its own separate board as it would need to be submerged in oil to prevent breakdown when voltage potentials approached greater than 20kV between two transformer coils.

Figure 4.1: 40kV charger schematic in PSpice

Massive area fills were needed on the input voltage side in an effort to handle currents that needed to be switched in the MOSFETs. They were alternated between ground and $V_{DC(input)}$ layer for 4 layers with the ground on the very bottom and the $V_{DC(input)}$ at the top. With the maximum potential current drawn of 3A per converter and allowing for minimal temperature rises, the traces for the DC-DC converters were chosen to be 50mils in width.

Figure 4.2: 40kV charger driver board layout

The transformer and multiplier board needed to be laid out once the main gate driver board had been completed. While the schematic shown in Figure 4.3 was relatively simple as it consisted of only the transformers, diodes, and capacitors, the layout would need to take into account considerably high voltages between points. Care was taken when selecting trace widths as the traces would have considerable current

Figure 4.4.

Figure 4.4: Multiplier board layout

The darker colored traces ran on the surface of the board while the lighter colored traces ran below the board. The transformer coil joining traces were purposefully placed underneath the board to prevent breakdown between the primary and secondary coils. Only 5 capacitor layouts were used so that the number of capacitors occupying surface space would be minimal resulting in the bottom layer having 5 capacitors in parallel mirrored as the top for a total of 10.

4.2.2 50kV Charger Layout

With considerably less voltage on the low voltage side of the system the 50kV charger layout was different and less massive than the 40kV charger. Due to advances in components and lower voltage requirements, the gate driver system was able to fit on a single 6" by 6" board. The transformer and multiplier setup was able to fit on another 6" by 6" board that was mirrored in mounting holes for ease of stacking and space considerations. Considerable care was taken to minimize outside noise affecting the device. The schematic of the driver board is shown in Figure 4.5. The schematic for the transformer and multiplier board is shown in Figure 4.6.

In order to minimize the inductance of the transformer primary that runs between the driver board and the transformer, the transformer and driver output needed to be as close on the board layout as possible. With a 0.5 inch ring inside the outer diameter of the original circle being added for safety as shown in Figure 4.7, this requires positioning the transformer in a position that does not leave room for all of the multipliers on the board surface alone. This problem was solved with the creation of multiplier modules that sit vertically and take up 0.75 inches of width and 1.7 inches of length compared to the full multiplier that takes 1.8 inches width and 1.7 inches length. The schematic for the multiplier module is shown below in Figure 4.8. The module layout is shown in Figure 4.9.

Figure 4.7: Transformer and Multiplier Layout

Figure 4.8: Multiplier Module Schematic

Figure 4.9: Multiplier Module Layout

4.3 40kV Charger Assembly

The 40kV charger was assembled. The multiplier board was submerged in oil to prevent breakdown. Heavy gauge spark plug wire with a voltage rating of 50kV was used as the output leads from the multipliers to the capacitor bank. The completed assembly is shown below in Figure 4.10.

Figure 4.10: Driver Board and Multiplier Setup (40kV)

In order to provide the required 1kJ of energy to the device, a capacitor bank was built using Mallory LES21823-A 450V_{DC} 1500 μ F capacitors. Calculating out the number of capacitors needed based on the 1kJ needed and an input voltage of 125V yielded 84 capacitors for a total capacitance of 126mF. The bank is shown below in Figure 4.11.

Figure 4.11: Input Capacitor Bank

With the load capacitance being set at $1.3\mu\text{F}$ and a high output voltage of 40kV , a capacitor bank for the output needed to be assembled as well. Maxwell Labs $0.16\mu\text{F}$ 50kV sealed capacitors were used in the setup with 9 being placed in parallel to achieve a load capacitance of $1.35\mu\text{F}$. A ground line was added to the ground terminal of the power supply to prevent ground loops from destroying equipment. The capacitors were put in a plastic bin to prevent arcing to the metal table or any passerby. The capacitor load bank is shown below in Figure 4.12.

Figure 4.12: Capacitor Load Isolated

4.4 50kV Charger Assembly

The 50kV charger design is a much smaller design than the 40kV charger. The design allowed for two separate 6" circles to stack vertically on top of each other, with a 1" clearance between the lower high voltage board and the upper low voltage board. This allowed for the low inductance connection between the transformer and H-bridge. The high voltage side could then be submerged in oil to cover the multipliers and transformer while leaving the low voltage side exposed to air. The load was a 10nF spark gap setup designed to break across the gap at 50kV.

Figure 4.13: Driver Board and Multiplier Setup (50kV)

CHAPTER 5

RESULTS

5.1 40kV Charger Results

Due to problems with noise and board errors discussed later in the chapter, the H-bridge was unable to modulate at frequencies greater than 200 kHz. All tests were performed with the device operating at a frequency of 187 kHz. Initial tests were done to verify the design of the 40kV charger at considerably lower voltages. Starting with as low as 5 volts in 5V increments up to 25 volts the device was operated in air. The test was performed with a single 1nF capacitor in each set of the multiplier cascades, a single 200V 20 μ F input capacitor charged to 5V, and a considerably lower load capacitance of 0.16 μ F. The output voltage was approximately 1.2kV, 240 times the initial voltage and what the device was designed for. The input voltage was increased up to 25V to test the system in this configuration. The results are shown in Figures 5.1 through 5.4.

Figure 5.1: 5V input to a 0.16µF load

Figure 5.2: 15V input to 0.16µF load

Figure 5.3: 20V input to 0.16µF load

Figure 5.4: 25V input to 0.16µF load

Once the device had been tested thoroughly in air the remaining 9 1nF capacitors were added to the multiplier cascade and the system was then submerged in oil to allow considerably higher voltages to be achieved. The results of the tests are shown in Figures 5.5 through 5.9. The calculated multiplication factor from the input voltage to the output voltage came out to be a factor of roughly 264, with the transformer providing a turns ratio of 1:11 and the multipliers providing a factor of 24. The ringing experienced by the waveforms was due to the setup of the oscilloscope, and the actual peak voltage was lessened compared to the peak shown in the charts.

Figure 5.5: 65V input to 0.16nF load in oil

Figure 5.6: 75V input to 0.16nF load in oil

Figure 5.7: 85V input to 0.16nF load in oil

Figure 5.8: 95V input to 0.16nF load in oil

Figure 5.9: 100V input to 0.16nF load in oil

After the device had been tested to 100V, the capacitor input bank and output banks were added to truly test the system. Here the weak links of the system were

exposed in the inductances in the lines and noise. The rise time went from 50-60ms up to 200-210ms. The results of these tests are shown below in Figures 5.10 and 5.11 with the decreasing line being the voltage measured at the input capacitor bank and the increasing line being the output voltage at the load.

Figure 5.10: 100V input to full system, 26.5kV output

Figure 5.11: 110V input to full system, 30kV max output

Final tested output voltage was found to be roughly 30kV from 110V input with an output energy of 600J. The device was then tested with a 100ms operating time to determine how fast the output voltage of the multiplier would rise at the load. Figures 5.12 through 5.14 are in reference to these tests.

Figure 5.12: 20V Input, 100ms

Figure 5.13: 30V Input, 100ms

Figure 5.14: 40v Input, 100ms

A problem with the board was found out when this method of testing was implemented. The gate drive PWM signal was cutting off seemingly at random. There was dead time between signals and the output voltage was at least 75% less than expected based on calculations of the multiplier. The problem that occurred with the device was determined to occur back at the driver board. The input PWM signal looked as it should from the UC1825, but when the capacitors were charged above 25V noise began to enter the system. The PWM waveforms for a 25V input are shown below in Figure 5.15. The upper is the output of the UC1825 and the lower is the output of the gate driver.

Figure 5.15: PWM and gate driver output with noise

An even greater noise problem was found when the device was charged to greater than 40V. The waveforms appeared to have erratic duty cycles that were not related to each other. This resulted in pulses being on for considerably less than desired, leading to much lower output voltage as the device was not charging for the entire 100ms period. The waveform for erratic duty cycles with an input of 50V are shown below in Figure 5.16 with upper being the UC1825 output and the lower being the gate driver output.

Figure 5.16: PWM and gate driver output with erratic duty cycle

Upon examination of the board, it was determined that the noise was being caused due to a poor ground setup for the UC1825. When higher voltages were present, the ground reference for the device would rise to greater than 3V causing the device to shut off as the voltage difference between the supply and ground ceased to be 15V and fell accordingly. Once the device shut off the noise would be eliminated, the voltage would rise to 15V and the device would operate again until the noise became too great and then the cycle would repeat itself over again.

5.2 Transformer Results

The transformer for the 50kV charger needed extensive testing to verify that the output voltage would be achievable. The first tests were done with a turn ratio of 1 turn to 150 at 30V to determine the rise time and voltage output. The rise time was found to be on the order of 10-15 μ s and the output was found to be relatively close to 150x the input voltage. The results for 30V input and 40V input are shown in Figures 5.17 and 5.18, respectively. The stepping effect seen is caused by the 40kV charger noise shutting the PWM controller off sporadically as referred to in the previous section.

Figure 5.17: Transformer 30V Input, 4.5kV Out

Figure 5.18: Transformer 40V Input, 6kV Output

5.3 Battery Supply

The 50kV charger had a unique aspect compared to the previous setup; the input charging voltage was going to be supplied by batteries. Lithium ion (LI) 3.7V rechargeable batteries and sealed lead acid 12V batteries were selected for tests to determine which would be the optimum battery setup for the situation. Since the input voltage needed to be 40V, the batteries would at minimum need to be cascaded in series. In order to provide 40V, the lithium ion batteries would need to be tested to determine the voltage drop at a certain current draw. A threshold of 3V was set for the test to determine the current draw. A battery was connected to a 250mΩ load for a period of 1 second. With an average current draw of 11.8A the voltage held at 2.95V. A typical waveform is shown in Figure 5.19.

Figure 5.19: Lithium Ion Battery Test of 2.95V at 250mΩ Yielding 11.8A.

The sealed lead acid battery with an Amp-hour rating of 70Ah was tested through a 150mΩ load and shown to produce 69A at 10.4V as shown in Figure 5.20.

Figure 5.20: Lead Acid Battery Test of 10.4V at 150mΩ Yielding 69A.

Analyzing the results lead to a determination of 98 LI batteries to provide 70A at 42V and 4 lead acid batteries to provide 70A at 41V. The LI batteries would cost \$3 each compared to the lead acid battery cost of \$17.85 each, which is a considerable cost improvement for the lead acid batteries. The weight savings were dramatic with 98 LI batteries weighing in at 9.8lbs and 4 lead acid batteries weighing in at 34lbs total. The decision to go with the lead acid over the LI batteries was one of convenience and cost over weight. LI batteries would require complex wiring in series and in parallel to provide the desired current and would require much maintenance and monitoring to

verify that they were still working properly while 4 lead acid batteries were considerably simpler to setup and maintain in series alone.

5.4 50kV Charger Results

In order to smooth the transition to the new charger, the charger was assembled one multiplier cascade at a time and tested before adding the next. This allowed for many tests to ensure proper operation with minimal chances of break down and damage to equipment. The device was first operated at low voltages and stepped up in 5V increments to end at 35V for the initial tests. With one multiplier cascade and transformer on the input and a 70nF load, the output voltage and rise time was investigated as shown below in Figures 5.21 through 5.23 along with the transformer waveform in Figure 5.24.

Figure 5.21: 10V input, 1 multiplier

Figure 5.22: 20V input, 1 multiplier

Figure 5.23: 35V input, 1 multiplier

Figure 5.24: 35V input, transformer waveform

Of interest to note is that the voltage never rises to its full potential of 300x the input and the trend continues as the input voltage is raised. The transformer waveform of Figure 5.24 above explains this as the input voltage falls from an expected 35V to closer to 22-25V. This explains the output waveforms as operating as expected, but the voltage is dropping because the current supplied by the onboard capacitors and the power supply is too little a value to keep the voltage up. The voltage continues to fall as the charging pulse goes on and the voltage will eventually stop rising beyond a point regardless of allowed charging time as was found when the a second multiplier was added, the results of which are shown below in Figures 5.25 through 5.27.

Figure 5.25: 10V input, 2 multipliers

Figure 5.26: 20V input, 2 multipliers

Figure 5.27: 35V input, 2 multipliers

In Figure 5.28 below, the drop of the voltage of the transformer is shown over time. Even though the charger is still operating for a total time of 20ms, the output voltage has already begun to fall off as early as 15ms when the transformer voltage falls below a level where it cannot sustain charging of the load any further.

Figure 5.28: 35V input, 2 multipliers, transformer drop

With the inability of the source to provide enough current to keep the transformer voltage up, installing the sealed lead acid batteries for the input to the charger to provide enough current to the device became the next step in the process. Two batteries were used to provide a DC voltage of 12.5V each. As such, all the tests were performed with one or two batteries in series. The waveform for a 25V input to a two multiplier cascade is shown below in Figure 5.29 and the voltage rises higher than the 35V input shown in Figures 5.27 and 5.28.

Figure 5.29: 25V battery input, 2 multipliers

Figure 5.30: 25V battery input, 3 multipliers

Figure 5.31: 25V battery input, 4 multipliers

Figure 5.32: 25V battery input, 5 multipliers

Figure 5.33: 25V battery input, 6 multipliers

The final output voltage of the initial tests was 22.2kV from 25V input, a multiplication factor of 888 versus the designed 1500 for 5 multipliers and 1800 for 6 multipliers. This multiplication factor was obtained in only 120ms, lengthening the charging time would likely increase the output voltage to considerably closer to the theoretical value. This is obvious due to the result of the 5 multiplier test and the 6 multiplier test being within 100V of each other for all test shots. Limitations of the initial tests include inductance in the lines between the batteries and the driver board, increased length of the primary transformer coil, a charging frequency of 350 kHz, and a load capacitance that is 7x the designed load capacitance. Modifications to these parameters all affect the rise time of the device. Steps are being taken to reduce the rise time as much as possible to fit within the design constraints.

CHAPTER 6

CONCLUSIONS

Two chargers were built and tested using similar topologies and hardware to achieve two different goals in speed and output voltage. Computer simulations in addition to theory and hand calculations change the design process and allow us to foresee problem areas that would not have been obvious by looking at a schematic. Knowledge of the shortcomings of a design helps by anticipation of potential problem before spending money, time, and effort to build a complicated design, and can even allow for solutions to be run through a system without spending more time, money and effort on something that could potentially not work or make the problem worse.

The 40kV charger experiment was almost successful in reaching the goals set out for it. It came to within 75% of required output voltage despite major flaws and problems with the board. The dangers present on the device needed to be handled extremely carefully through the use of isolation and redundant grounds. The shortcomings in the design did not become apparent until late into the testing phase of the project. A second design of this board would yield a more reliable PWM signal. A bigger design change would need to be considered to minimize the inductance between the H-bridge output and the transformer, as this drastically increased rise-times and prevented the device from operating quickly under load.

The 50kV charger experiment has been built and tested and is proving to be a much more reliable and stable charger than the 40kV charger. Due to its more compact design, better grounding, and fiber optic isolation of the driver circuits the noise problems

present in the original charger are no longer a problem. Minimizing inductance between voltage sources and transformer coils is the biggest problem affecting rise time of the system.

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