MICROMACHINING PROCESS FOR MICROSENSOR FABRICATION

by

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ABSTRACT

MEMS (microelectromechanical systems) are an outgrowth of silicon technology. They are chip-sized systems that have the ability to affect their surroundings and to communicate what they know to the outside world in new and dramatic ways. And they can be made cheaply. In the fall of 1999, the Sensor Systems Center (SSC) was formed at Texas Tech University to capitalize on the growing interest in microsensors and microanalysis systems, the research was focused on the design, fabrication, and testing of wafer-based, compact microanalysis systems.

At SSC, micromachining processes are under development for this purpose. Oxidation, lithography, PCD, CVD, etching are inherited from semiconductor processing and are done using processing tools and characterization equipments housed at the Maddox Laboratory. Bonding process is new and a tailored anodic bonding system has been self-built. Bonding between Si/Si, Si/Glass, and Glass/Glass wafer pairs can be done using these tools. Channels are made in silicon and glass substrate. A bulk-micomachinined accelerometer has been successfully fabricated. More complex and functional microsystems are being developed using these processes.

In this paper these process steps are summarized with theoretical descriptions and actual fabrication examples, experimental results are investigated as well to optimize these process steps.

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CHAPTER I

INTRODUCTION

1.1 Thesis Overview

This thesis covers micro-fabrication steps used for building micro devices including theory, lab work, and result.

Micromachining is a technology under development, however, most process steps used for micro sensor fabrication are inherited from semiconductor processing. Oxidation and lithography are two examples. Some relatively new processes like wafer bonding are also being developed for this purpose. This thesis begins with theoretical descriptions of these processes. Then, examples are given to describe the actual operations. A complex project integrating of all these process steps is also presented. Finally, experimental results are investigated to optimize these process steps.

1.2 Why Micromachining?

MEMS (microelectromechanical systems) are an outgrowth of silicon technology. The silicon revolution began over three decades ago. The hallmark of the industry over the past three decades has been the exponential increase in the number of transistors incorporated onto a single piece of silicon. This rapid advance in the number of transistors per chips has lead to continuous increases in capability and performance of the integrated circuits. As time has progressed, large, expensive, and complex systems have been replaced by small, high-performance, inexpensive integrated circuits.

However, the next silicon revolution will be different and more important than simply packing more transistors onto the silicon. The new trend is the incorporation of new types of functionality. Structures that will enable the chip to not only reason, but sense, act and communicate as well. This will result in chips that will have the ability to affect their surroundings and to communicate what they know to the outside world in new and dramatic ways. Besides processing data, the chips of tomorrow will process such things as chemical information, motion, light, and knowledge. In short, the metric by which a technology is measured will change from how many transistors are on a chip into how functional a chip is. MEMS is making and will continue to make this possible.

Next, MEMS can be made cheaply, because they are made by exploiting the existing integrated circuit manufacturing infrastructure. For example, IC's are made by bulk manufacture techniques such as deposition, etching, implantation, and packaging. For MEMS, the same fabrication steps are used. What is more, because few applications in MEMS require line widths of less than one micron, a fabrication facility that is obsolete from the perspective of an IC company could be state-of-the-art from the perspective of a MEMS company. Thus, MEMS offers the opportunity to extend the useful life of aging microelectronic fabrication facilities.

The third factor making MEMS technology favorable is that it is mostly based on single crystalline silicon. Besides its well-known electrical characterization, single crystal silicon has a number of remarkable mechanical properties (see Table 1.1). First, unlike a metal, it is not ductile, so at room temperature, it can only be elastically deformed. There is no mechanical hysteresis. Next, the yield strength of silicon is extremely high,

comparable to stainless steel. Third, the creep effect of silicon is very small, in the range of a few 10s of ppm. So, for an electrical-mechanical mixed system like MEMS, it is an excellent material for micro-technology.

Table 1.1 Mechanical properties of common materials (complied from Petersen[1])

	Yield Strength (Gpa)	Young's Modulus (100Gpa)	Density (1000 Kg/m^3)	Thermal expansion (10^{-6}/°K)
Diamond	53	10.35	3.5	1
Silicon	7	1.9	2.3	2.33
Stainless Steel	2.1	2.0	7.9	17.3
Aluminum	0.17	0.7	2.7	25

Of course, MEMS technology has competition. First, markets for micromachined products are still mainly constrained inside automotive field, but TI's DLP has the most notable exception. New market and products are still being exploring. Second, today there are minimal standards for MEMS technology in design and fabrication. So, MEMS technology has a lot of prospects but still needs time to mature.

1.3 An Introduction to Micromachining

Micro-machining refers to a group of three-dimensional micro fabrication techniques enabling control of feature size dimensions to accuracies in the micrometer range. It is mainly based upon existing semiconductor processing technology.

There are also some new terms developed for micromachining technology. In order to facilitate the following description, they are defined here as follows:

- Surface micromachining

Refers to processing above the substrate. In other words, substrate is mainly used as a base, the micro-structure is built on top of the substrate.

- Bulk micromachining

Refers to processing inside the bulk substrate. For example, large pits, channels, and holes are made inside the substrate.

1.4 Application and Future of Micromachining

In its short history, MEMS products have been driven by the automotive market and are mainly within devices for sensing mechanical quantities such as pressure, force, flow, or acceleration. However, we are still at the innovative stage of development of these devices, and new ways of using this technology will emerge which will increase the feasibility and expand the application area. Actually, it is mainly restricted by the imagination of device designers to come up with innovative new designs.

Roughly divided by their usage, there have been a number of high-volume products introduced recently that are MEMS based.

1.4.1 Sensors

By far, the biggest components of the MEMS based product market are sensors. A lot of MEMS based sensors have been developed to measure acceleration, rotation, and other quantities. One prominent example is accelerometers for airbag triggering. Figure 1.2 shows the technical data for ADXL105, a product that is being used to trigger the airbag in a number of automobiles.

Shown in Figure 1.1, the ADXL50 is a differential capacitor sensor with fixed end plates and a movable "floating" central plate. When an acceleration is applied, the floating central plate moves closer to one of the fixed end plates and further from the other as shown below. When the sensor begins to move, a mismatch in the value of their capacitance is created, producing an output signal at the central plate. Note that the sensor needs to be oriented so that the measured acceleration is along its sensitive axis.

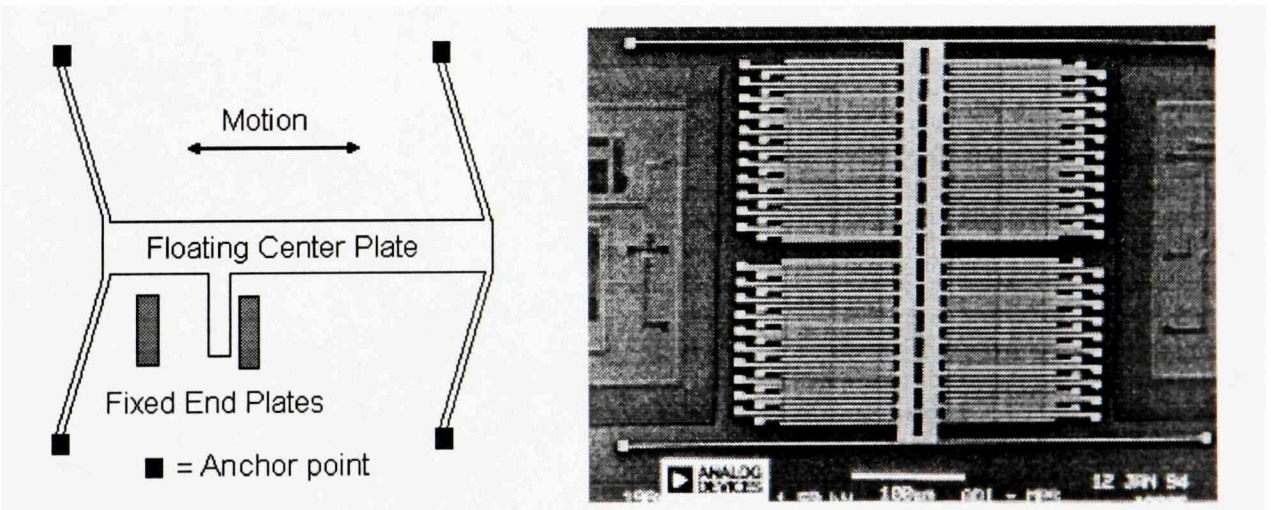


Figure 1.1. Working principle and structure of ADXL50

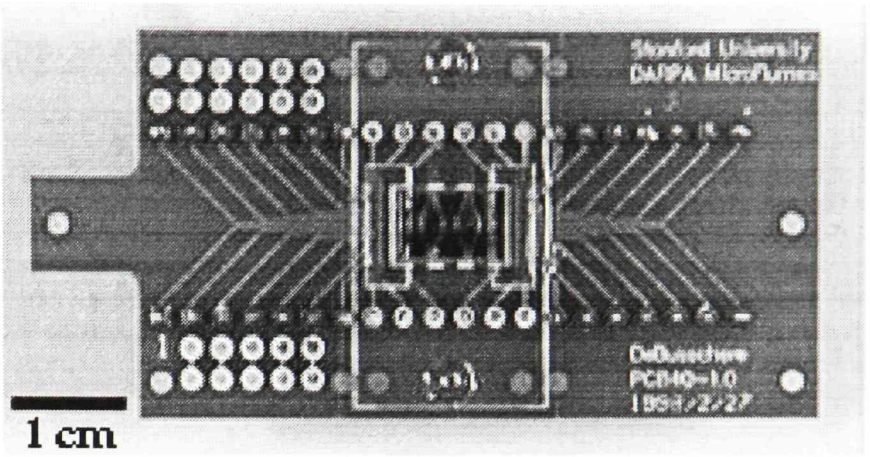
Single Axis with +-5g Range
Analog Output Ratiometric to Supply
2mg Resolution
10kHz Bandwidth
On Board Temperature Sensor
Low Power and Voltage. 2mA at 5V, Operation down to 2.7V
Uncommitted Amplifier
Surface Mount Package

Figure 1.2 Technical data for ADXL105 MEMS based accelerometer (complied from Analog Devices Inc. [2])

1.4.2 Biological/Chemical analysis systems

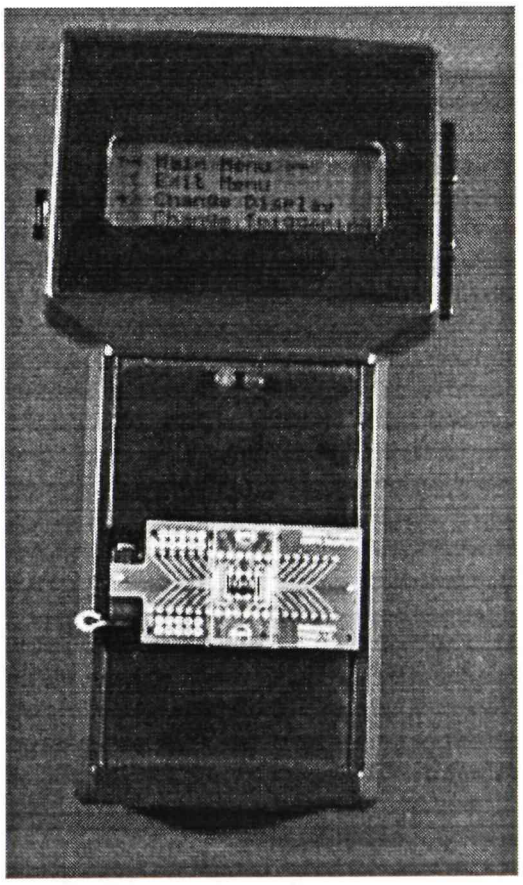
Batch fabrication MEMS technology can be used to make systems with micron-size features. It is possible to make what a normally bench top sized analysis system much smaller. Finally, portable field analysis systems are now possible. Figures 1.3 and 1.4 show portable biosensors under-development at the Center for Integrated Systems, Stanford University [3].

The handheld instrument is used to monitor cellular activity in the cell cartridges. The cell cartridge has two 10-microliter chambers that will allow differential measurements on the same substrate. An onboard Motorola HC12 microcontroller captures, processes, and stores data.

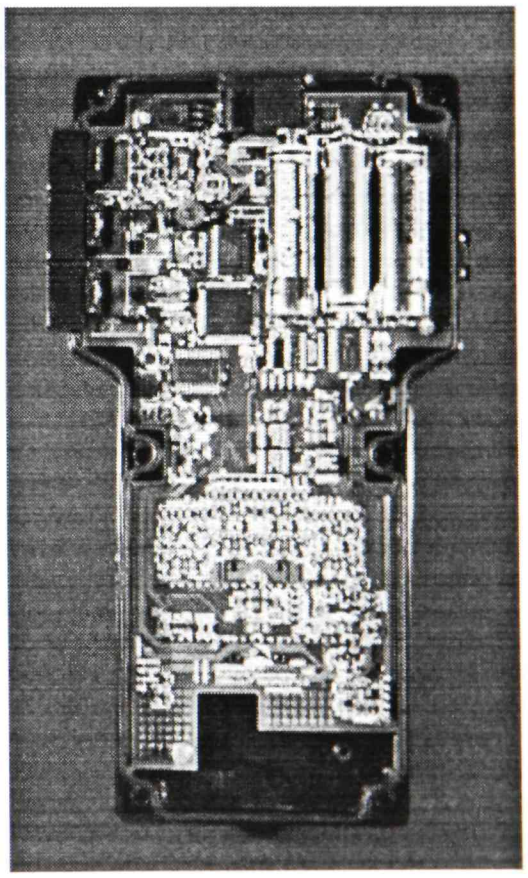


Top view of a cell cartridge. A silicon die with electrodes is mounted directly on the PCB and enclosed on the top and sides by a PDMS part. As the 40-pin cartridge is lowered into a ZIF socket, the needles pierce septa to form fluidic interconnects.

Figure 1.3. View of PCB board of portable biosensor



Front side of handheld sensor



Backside of handheld sensor

Figure 1.4. Assembled handheld biosensor

1.4.3 Optical application

Many MEMS structure have been developed for optical applications. The following are some examples:

- Fiber optic switch
- Micro lens
- Projection display
- Near field microscope
- Fiber optics sensor.

Figure 1.5 shows an electrostatic 2D scanning mirror developed by the Integrated Photonics Laboratory at UCLA. By applying a voltage of about 50 V, an electrostatic force will tilt mirror and reflect incident light at different angles. In this way, image projection can be realized.

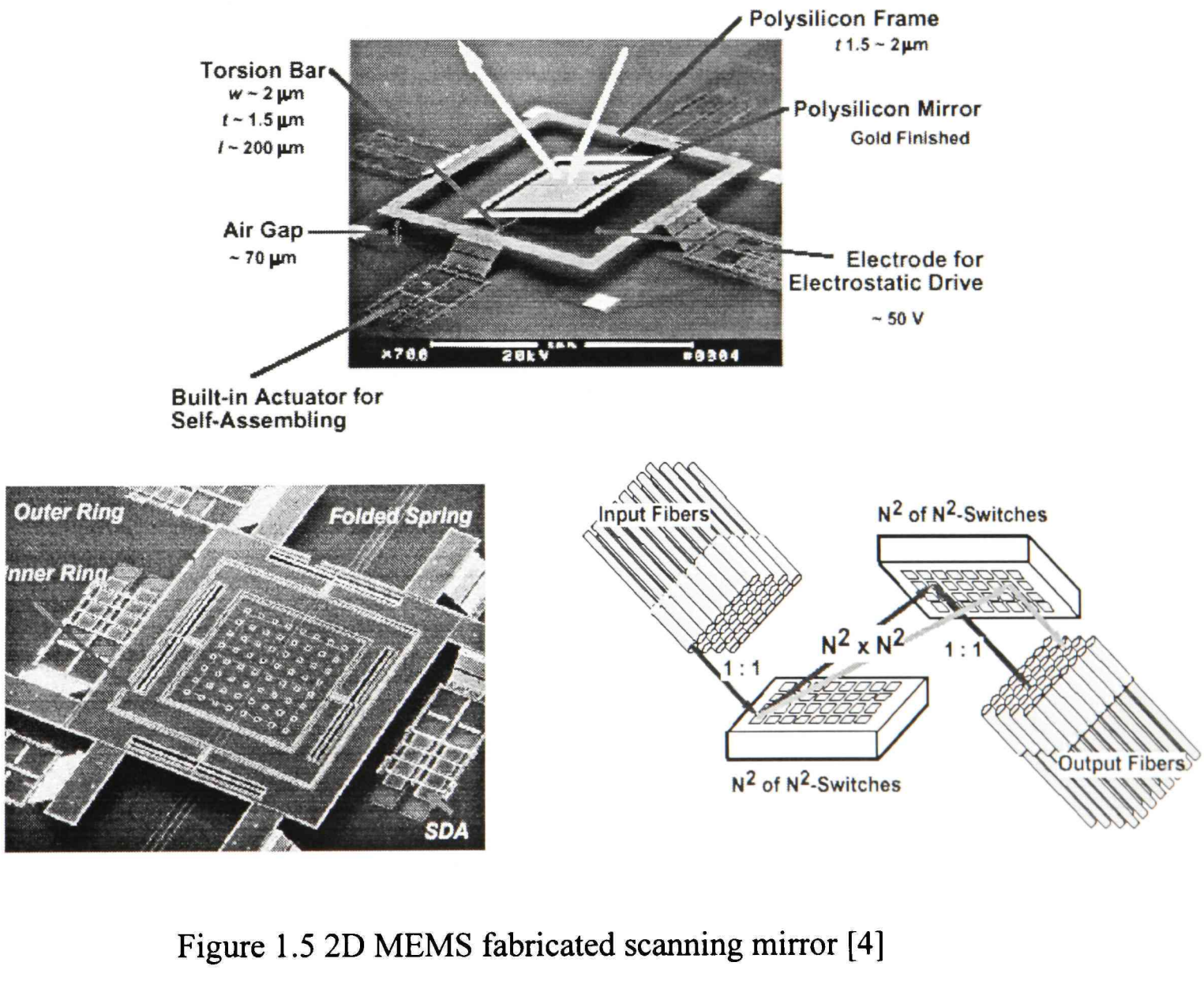


Figure 1.5 2D MEMS fabricated scanning mirror [4]

The above mentioned applications and technologies illustrate the potential of the MEMS technology. They represent only the tip of the iceberg, but are nonetheless important implementations. These successes show that MEMS can make the transition from laboratory demonstrations to variable commercial products. It is anticipated that successful MEMS-based products will be introduced into the market at an ever-increasing rate. As this happens, MEMS will become ubiquitous. They will become part of many consumer products. They will make existing products better, and eventually will enable totally new products not even imagined today. Their ability to give integrated circuits the capacity to understand where they are and what is going on around them will likely impact this century as profoundly as the integrated circuit's ability to think as impacted today's life.

CHAPTER II
PROCESS DEVELOPED FOR MICROMACHINED DEVICES

2.1 Bulk Micromachining

Bulk micromachining of silicon uses wet and dry etch process in conjunction with etch masks and etch stops to sculpt micro-mechanical devices from a silicon substrate. Processes steps such as oxidation, lithography, thin film growth, and wet etch are commonly used.

2.1.1 Oxidation

Oxidation is a fundamental process for all silicon device fabrication. In micromachining, oxidized regions of silicon wafers are used as a mask layer during etching, and as a dielectric film.

Silicon, when exposed to air at room temperature, will grow a native oxide about 20 Å thick. Thermal oxide layers can be grown by either a dry or wet process. Table 2.1 shows the results of oxidation by a THERMCO thermal oxidation oven in the Maddox Lab. At a given temperature, the relationship between the thickness of oxide and time is parabolic (see Figure 2.1). The relationship of thickness versus time with temperature and orientation as parameters can be found in many books [5-9]. From Figure 2.1, it is clear that a thermally grown oxide layer thicker than 1μm is very time consuming. If an oxide with a thickness of more than 1.5μm is required, other methods should be used, such as

chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD). A typical recipe for CVD grown oxide is

$$SiH_4 + O_2 \rightarrow SiO_2(solid) + 2H_2(gas).$$

Often hydrogen is added as a diluent to improve the uniformity of the deposition. The deposition rate can be as high as 100 nm/min.

Normally, thermally grown oxides induce high stress, which can make the silicon substrate bow or even break.

Table 2.1 Thermal Oxide thickness of oxides at 1100°C.

Oxidation Method	Time (min)	Oxide thickness (μm)
Dry	40	0.06
Dry	60	0.095
Wet	40	0.6
Wet	60	0.7

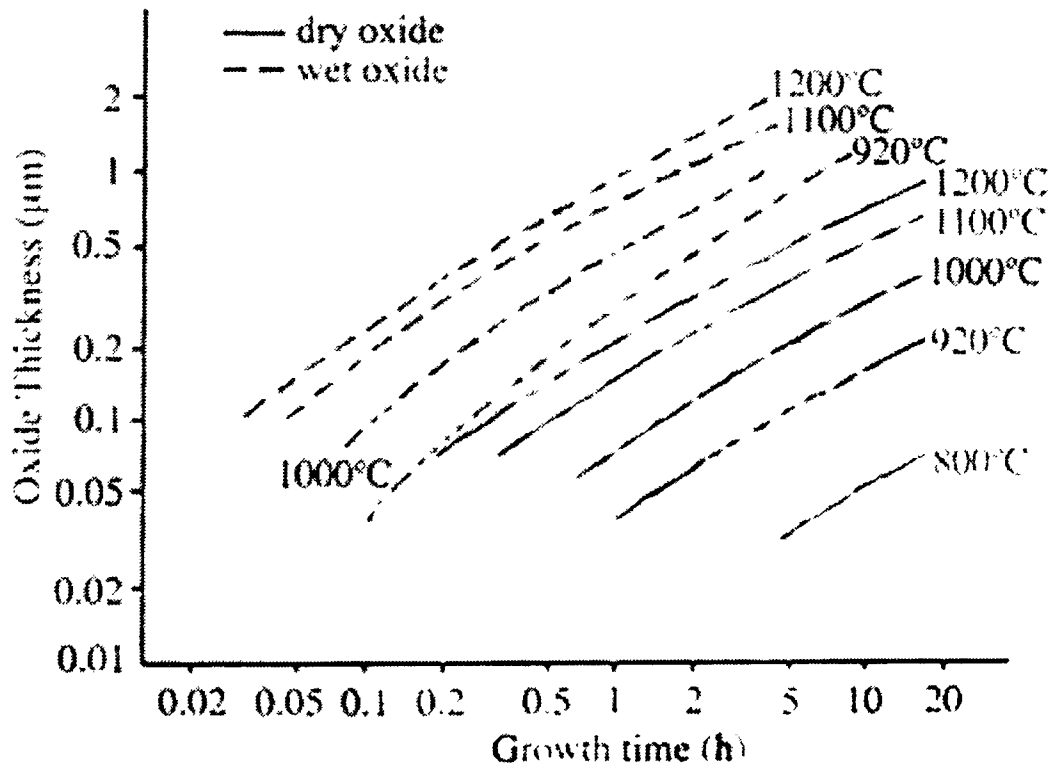


Figure 2. 1. Thermal Oxidation rates [10]

2.1.2 Lithography

Lithography is the process of transferring a pattern on a mask to a photo sensitive polymer which, in turn, is used to transfer the pattern to the films or substrates through etching processes or other fabrication processes. The entire lithography process involves several sequential steps:

- Mask making
- Wafer cleaning
- Application of photoresist
- Pre-baking
- Optical exposure to print an image of the mask onto the resist
- Immersion in developer solution to dissolve the exposed resist.

In most cases, the mask consists of a patterned opaque chromium layer on a transparent glass substrate. For our projects, besides factory made masks, we printed gold foil covered transparencies using an ALPS MD5000 photo quality color printer. The minimum feature sizes the printer can print is on the order of 100μm.

There are two types of resist, positive and negative. A positive resist is an organic resin material containing a "sensitizer." It is spin coated on the wafer to a typical thickness between 1μm and 100μm. In general, the higher the spin speed, the thinner the resist layer will be. As mentioned earlier, special types of resist can be spun to a thickness of up to 100μm. The sensitizer prevents the dissolution of unexposed resist development. Exposure to light in the 200 to 400 nm range breaks down the sensitizer, causing exposed

regions to dissolve in a developer solution. The exact opposite process happens in the negative resists. Exposed areas remain while unexposed areas dissolve in the developer.

After the wafers are coated with photoresist, they are baked for 1 minute at 120°C. This step is called pre-bake and it is used to:

- drive off the solvent from the photoresist and thus, improve the adhesion of the substrate with the photoresist during the development step, and
- anneal stresses caused by the spinning process.

Optical exposure can be accomplished in one of the three different modes: contact, proximity, or projection. In contact lithography, the mask touches the wafer, which shortens the life of the mask and can leave undesired residue on the wafer and the mask. In proximity mode, the mask is brought to within 20-50μm of the resist surface. In contrast, projection lithography projects an image of the mask onto the wafer through complex optics.

Resolution is defined as the minimum feature the optical system can resolve in photoresist. For a proximity system it is limited by Fresnel diffraction to a minimum of about 5μm. For a contact system, it is less than 1 μm. For projection systems, it is given by

$$0.5\lambda/NA$$

where λ is the wavelength and NA is the numerical aperture of the optics. Resolution in projection lithography is routinely much better than one micrometer.

Depth of focus, however, is a more severe constraint on the lithography, especially when exposing thick resist. Also, accommodating geometrical height

variations across the wafer can be challenging. Depth of focus for contact and proximity system is also limited by Fresnel diffraction. In projection systems, the image plane can be moved by adjusting the focus settings, but once it is fixed, the depth of focus about the plane is limited by

$$0.5\lambda/NA^2 .$$

In nearly all cases, depth of focus is at most a few microns. For our projects, the contact printing mode is chosen. A CANON Parallel-light Mask Aligner PLA-501F was used to expose the wafers. The exposure light is a high intensity broad band Hg-arc lamp which emits both G-line and I-line UV wavelengths.

2.1.3 Thin film technology

Physical vapor deposition (PVD) is a technique for depositing solid material on a substrate by vaporizing a target material by heating or ion bombardment in a vacuum chamber. Substrates can be covered by a uniform polycrystalline or amorphous film of the target material.

In micromachining processing, PVD is used to deposit dielectric films such as SiO_2, or to deposit metals such as aluminum or gold as conducting interconnections and bonding pads. In our projects, E-beam evaporation was used to deposit gold and aluminum film on the substrates. The detailed description and configuration of that E-beam evaporation system can be found in reference [11].

2.1.4 Wet etching

The objective of wet etching is to selectively remove material using imaged photoresist or another material as a masking template. The pattern can be etched directly into the silicon substrate, or into a thin film, which in turn can be used as a mask for subsequent etches. For a successful etch, there must be sufficient selectivity between the masking material and the material being etched. Table 2.2 shows common etchants and their characteristics. Both wet and dry etchants are present in that table and their etch rates are dramatically different. Wet etchants in aqueous solution offer the advantage of low-cost batch fabrication. Several wafers can be etched simultaneously. Dry etching involves the use of reactant gases in a low-pressure plasma. The equipment is specialized and requires high-purity reactant gases being feed into the vacuum chamber.

Etch processes can also be divided into anisotropic and isotropic types. The isotropic etchants etch uniformly in all direction, resulting in rounded cross-sectional features. In contrast, anisotropic etchants etch in one direction preferentially over others, resulting in trenches or cavities delineated by flat and well-defined surfaces. Most dry etching is anisotropic while wet etching can be either.

Table 2.2 Common etchant used in micromachining and their etch rates [12]

	Wet Etchants	Etch Rate (nm/min)	Dry Etching	Etch Rate (nm/min)
Silicon Dioxide	$HF:NH_4F(BHF)$	100-500	CHF_3+O_2	50-150
Silicon Nitride	H_3PO_4	5	SF_6	150-250
Aluminum	$H_3PO_4:HNO_3:CH_3COOH$ HF	660 5	Cl_2+SiCl_4 $CHCl_3+BCl_3$	100-150 200-600
Gold	KI	40		
Titanium	$HF:H_2O_2$	20-100	SF_6	100-150
Tungsten	H_2O_2	20-100	SF_6	100-150
Organic layers	$H_2SO_4:H_2O_2$ CH_3COCH_3	>1000 >4000	O_2	35-3500

2.1.4.1 Isotropic wet etch. Isotropic wet etching of silicon is much less popular for micromachining than anisotropic etching because the shape of the etched structures is hard to control and is much less reproducible than anisotropic etching. However, isotropic etching has its own advantages. First, it is a room temperature process. Next, it is much faster than anisotropic etching. Last, photoresist can be used as the mask material.

A common isotropic etchant of silicon is a mixture of HNO_3 and HF in water. The overall reaction is given by

$$Si + HNO_3 + 6HF \rightarrow H_2SF_6 + HNO_2 + H_2 + H_2O \ .$$

Often acetic acid (CH_3COOH) is used as an alternate for water because it can act as a buffer. Figure 2.2 shows the results for various constituents by weight.

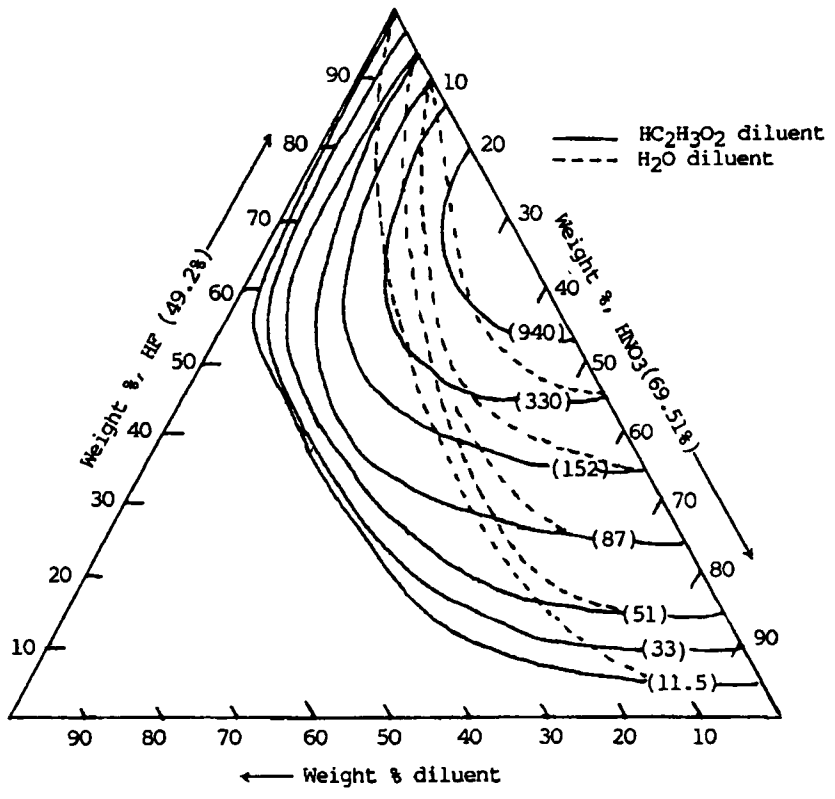


Figure 2.2. The etch rate of silicon in HF and HNO_3 [13]

Another common isotropic wet etchant used in micromachining silicon dioxide is buffered HF (BHF); a mixture of HF and NH_4F, the hydrofluoric acid removes silicon dioxide, and NH_4F provides fresh HF so the reaction rate can be kept constant. The reaction can be formulized as:

$$SiO_2 + 6HF \rightarrow H_2 + SiF_6 + 2H_2O$$

and

$$NH_4F \Leftrightarrow NH_3 + HF\,.$$

The etch rate can vary a lot from 600Å/min to 2500Å/min, depending on the proportion of the acid in the mixture and the reaction temperature. Etch rate and surface uniformity are normally hard to control. Figure 2.3 shows SiO_2 etch rates at different temperatures.

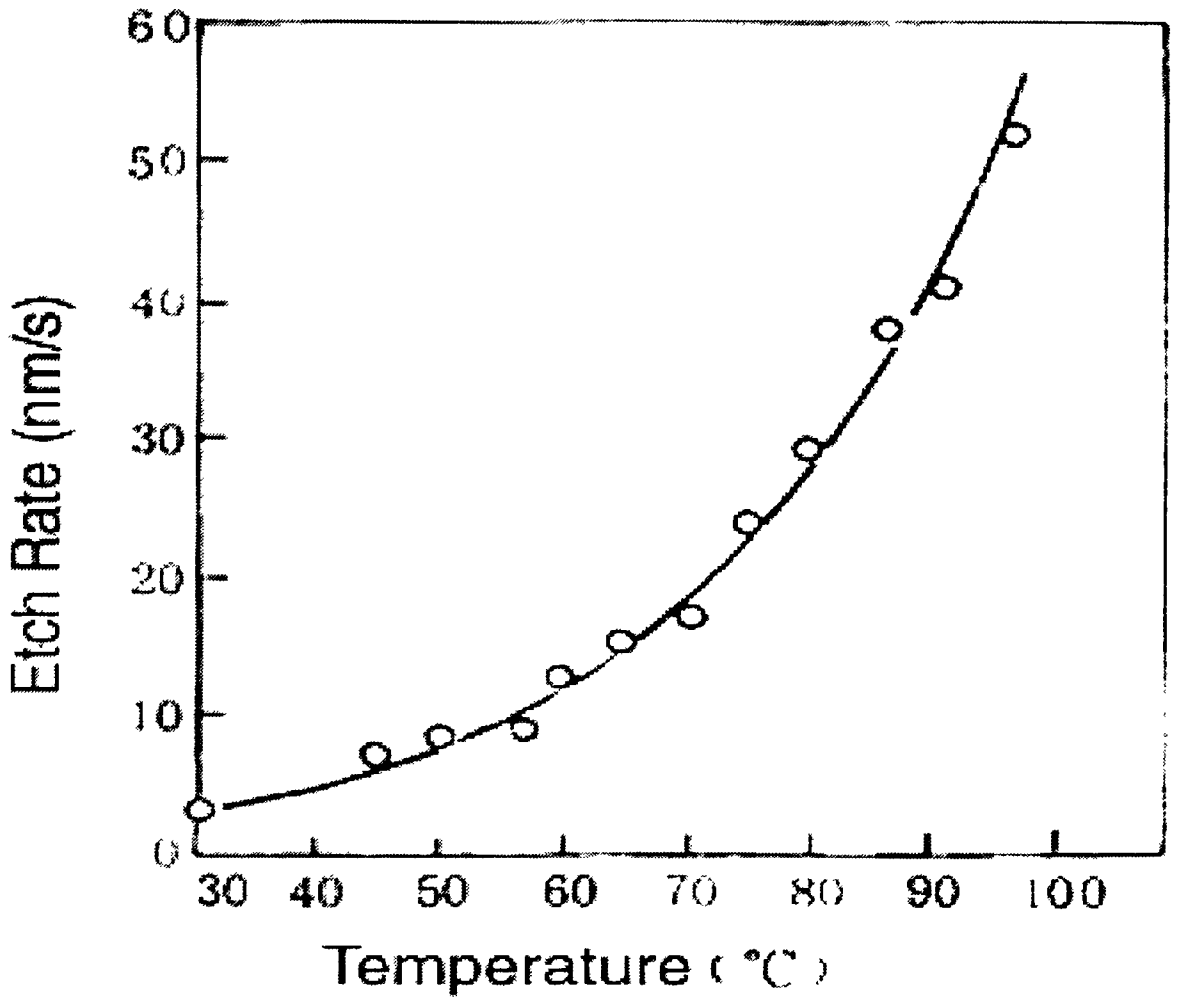


Figure 2.3. SiO_2 etch rate related with temperature of BHF [14]

2.1.4.2 Anisotropic wet etch. Among anisotropic etchants of silicon, KOH is the most popular. The overall reaction consists of two steps:

$$Si + 2OH^- \rightarrow Si(OH)_2^{++} + 4e^-$$

and

$$Si(OH)_2^{++} + 4e^- + 4H_2O \rightarrow Si(OH)_6^- + 2H_2(gas).$$

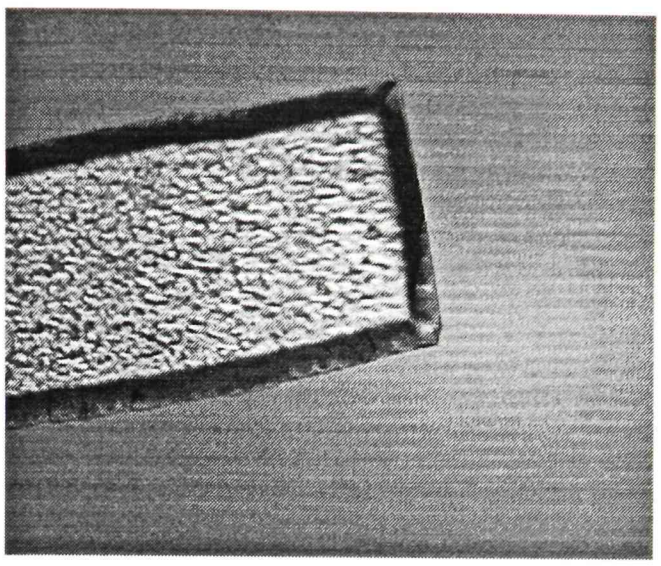
During KOH etching of silicon, bubbles can be observed.

KOH etching of silicon is orientation dependent. This means KOH etches the (100) and (110) planes significantly faster than the (111) plane. Etch rate ratios of 400:1 have been published [15]. Silicon nitride and silicon dioxide are the commonly used etch masks for KOH etching at silicon. These films are used to mask areas of silicon that are to be protected from etching.

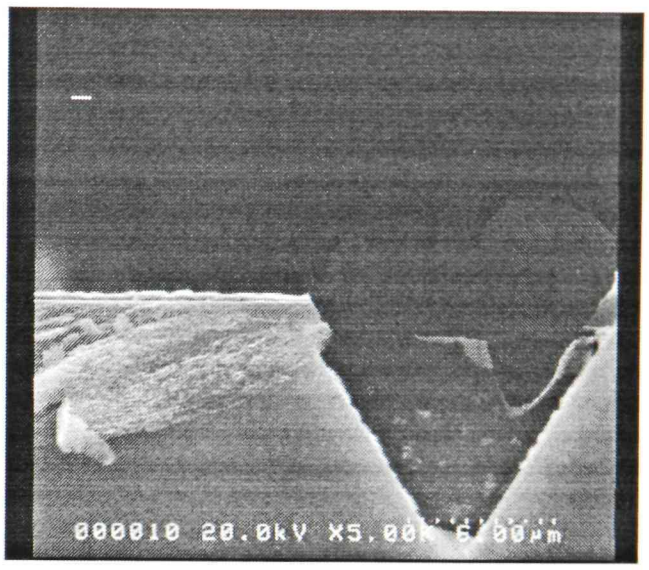
Another widely used technique in the anisotropic etching of silicon is the use of an etch stop. Heavily-boron-doped silicon (above $7x10^9\,cm^{-3}$) is effective in stopping the etch. Alternatively, the pn-junction technique can be used to stop the etch when one-side of a reverse-biased junction is etched away.

Because the KOH etch is orientation dependent, various shapes can be formed. V-shaped cavities can be etched in [100] oriented wafers. The etch front begins at the opening in the mask and proceeds in the <100> direction, which is the vertical direction in [100] oriented substrates, creating a cavity with a flat bottom and slanted sides. The sides are [111] planes making an angle of 54.74° with respect to the horizontal [100] planes. The etch ultimately self limits on four intersecting [111] planes, forming an inverted pyramid or V-shaped trench. Of course, this occurs only if the wafer is thicker than the projected etch depth. Timed etching from one side of the wafer is frequently used to form cavities or thin membranes. Funnel and oblique-shaped ports are also possible in [100] wafers by etching aligned patterns from both sides of the wafer, and allowing the two etch fronts to coalesce. Figure 2.4 shows the V-shape groove formed in

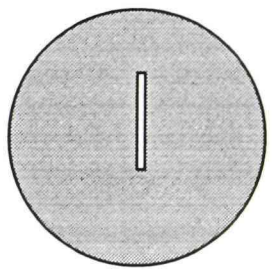
this way. The sidewall and self-limited groove are clearly shown on AFM and SEM photos.



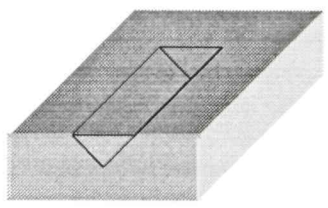
AFM photo of a cavity with a flat bottom



SEM photo of crosssection of a self limited V cavity



Mask used for etch

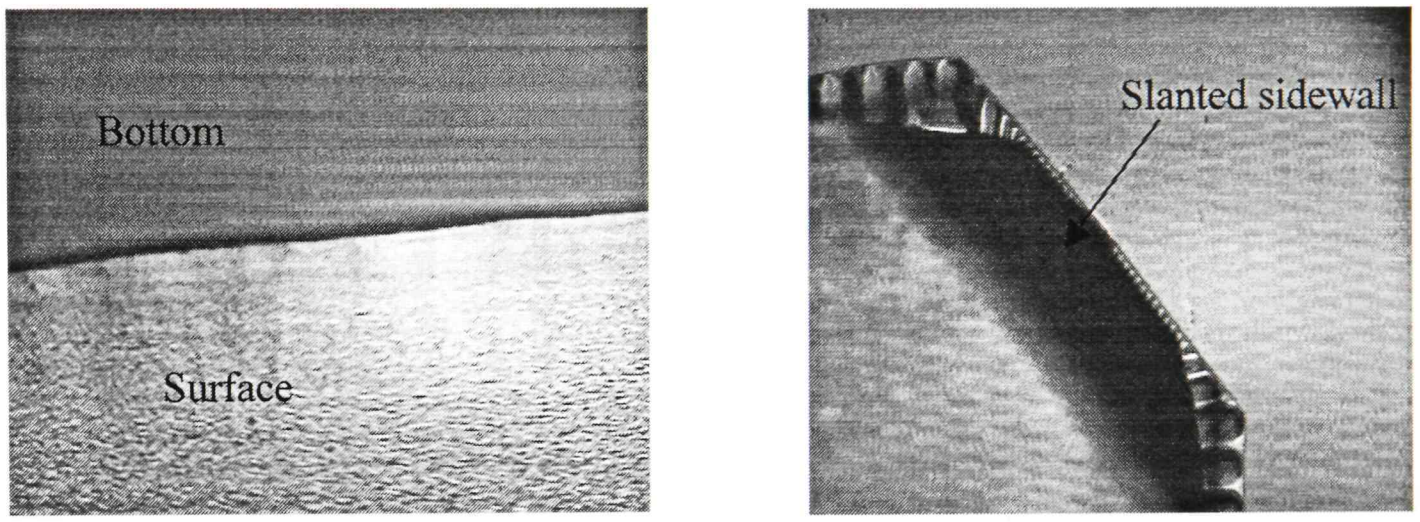


3D view of formed cavity

Figure 2.4. V groove formed using KOH etch of <100> Si wafer

Etching in [110] oriented wafers is quite different. The etch is still ultimately self-limited in [111] planes; however, there are eight <111> planes, four of them are

perpendicular to the [110] wafer surface, the other four are slanted at 35.26° with respect to the surface, so a groove etched in [110] wafers will have the appearance of a complex polygon limited by six <111> planes. Etching [110] wafers is useful to form trenches with vertical sidewalls. Figure 2.5 shows an example of etching a <110> oriented wafer.



Vertical wall formed by etching 110 wafer

Slanted 111 surface when etching into 110 wafer

Figure 2.5. Trenches formed by etching <110> oriented silicon wafers

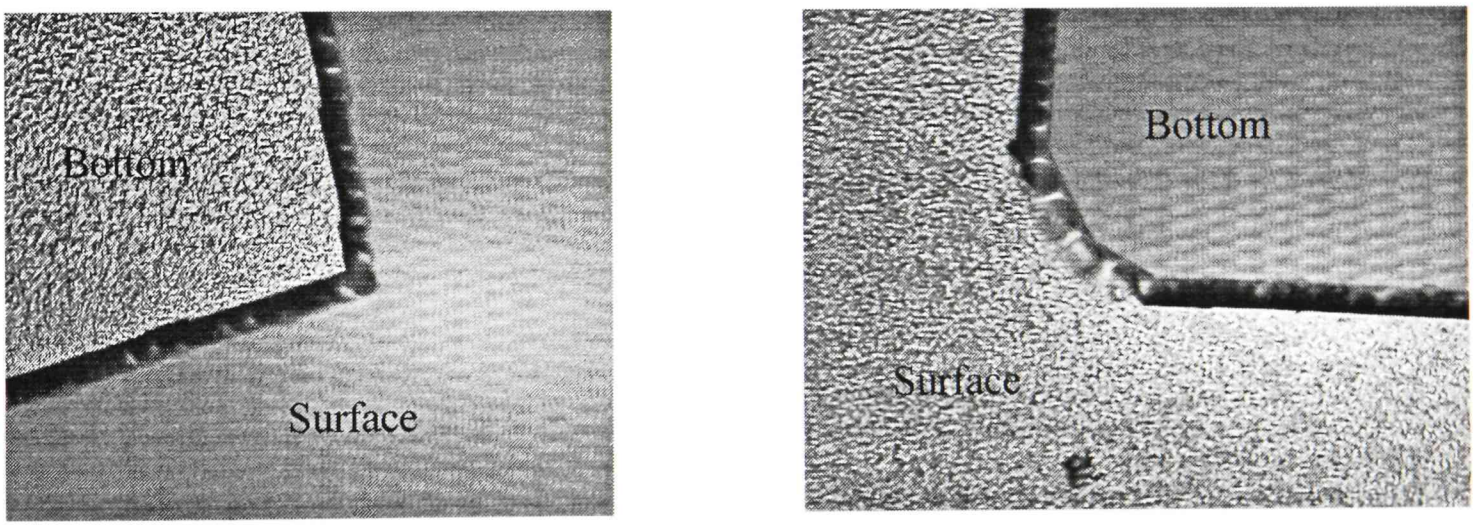
3D view of etched trench

Mask used for etching

Figure 2.6. Possible trenches formed by etching <110> oriented silicon wafers

Another important phenomenon of KOH etching is the undercut of convex corners. While concave corners bounded by [111] planes remain intact during the etch,

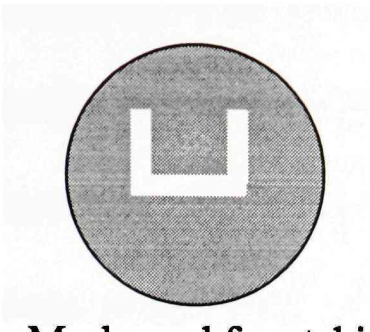
convex corners are immediately attacked. This is because any slight erosion of the convex corner exposes planes other than [111] planes, thus accelerating the etch. Consequently, a convex corner in the mask layout will get undercut during etching. In other words, the etch front will get underneath the masking layer. The photos and drawing in Figures 2.7 and 2.8 give a clear view of this. In some instances, such as when a square island is desired, this effect becomes detrimental, and is compensated for by clever layout schemes called "corner compensation." The effect is often intentionally used to form beams suspended over cavities.



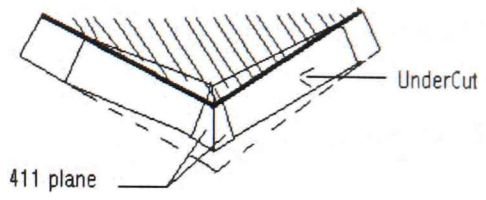
Concave corner after etching

Convex corner after etching

Figure 2.7. Undercut of convex structure



Mask used for etching

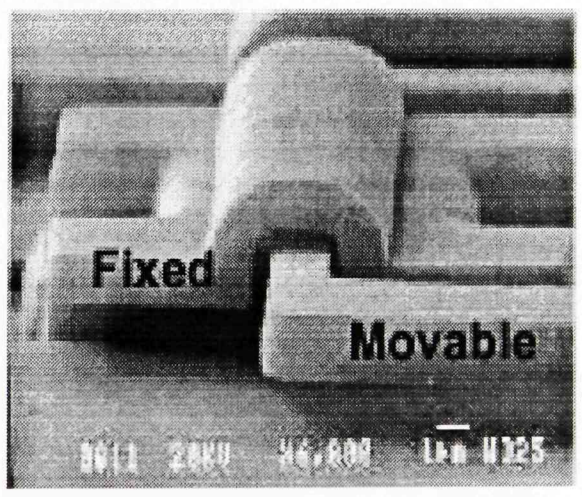


Convex corners are attacked, so compensation structure is needed to keep the layout

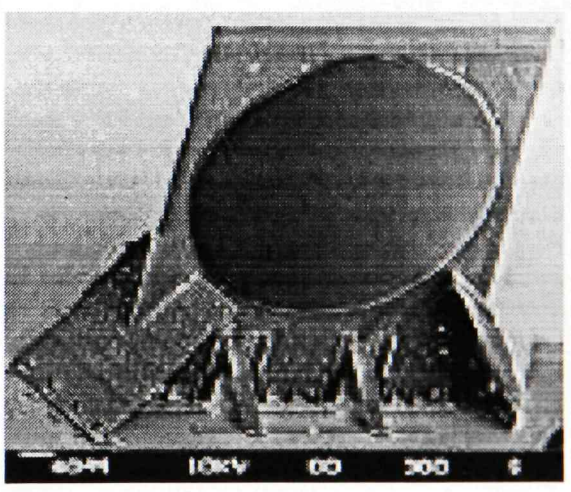
Figure 2.8. Exposed extra plane during KOH etch at a convex structure.

2.2 Surface Micromachining

Surface micromachining refers to processing above the substrate. In other words, the substrate is mainly used as a base and the micro-structures are built on top of the substrate. The biggest advantage is the capability to build mechanical structures with larger freedom of motion than bulk micromachined structures. Figure 2.9 shows the movable structure fabricated above the substrate by surface micromachining [4].



Hinge structure



Refractive lens

Figure 2.9. Refractive lens fabricated by surface micromachining

One basic fabrication technique for surface micromachining is the sacrificial layer etch. The idea is to deposit and subsequently pattern a layer of sacrificial material. Then a layer of structure layer is deposited and patterned. Next, the sacrificial layer is selectively etched away so the structural layer can be partially released to form moveable parts. Many papers have detailed description of this technique [16-19].

Another important technology used in surface micomachining is wafer bonding. Wafer bonding refers to the phenomenon in which extremely flat, and clean wafer of almost any material, when brought into contact are attracted to each other by Van der Waals forces and adhere to each other. The wafers involved in actual applications are typically semiconductor wafers such as silicon. The surface of two mirror-polished silicon wafers, which may or may not contain structures such as cavities, are conditioned and prepared for the bonding process. The wafers are made hydrophilic by a proper surface treatment. The flatness and clean of the wafer is critical to the success of bonding.

Several terms have been used to classify the different types of wafer bonding:

- " direct bonding" or "fusion bonding"

These terms refer to bonding of two silicon wafers with or without a thin layer of thermal or native oxide. The term fusion bonding is misleading. By no means is it a requirement for the silicon to be processed at a temperature as high as its fusion point.

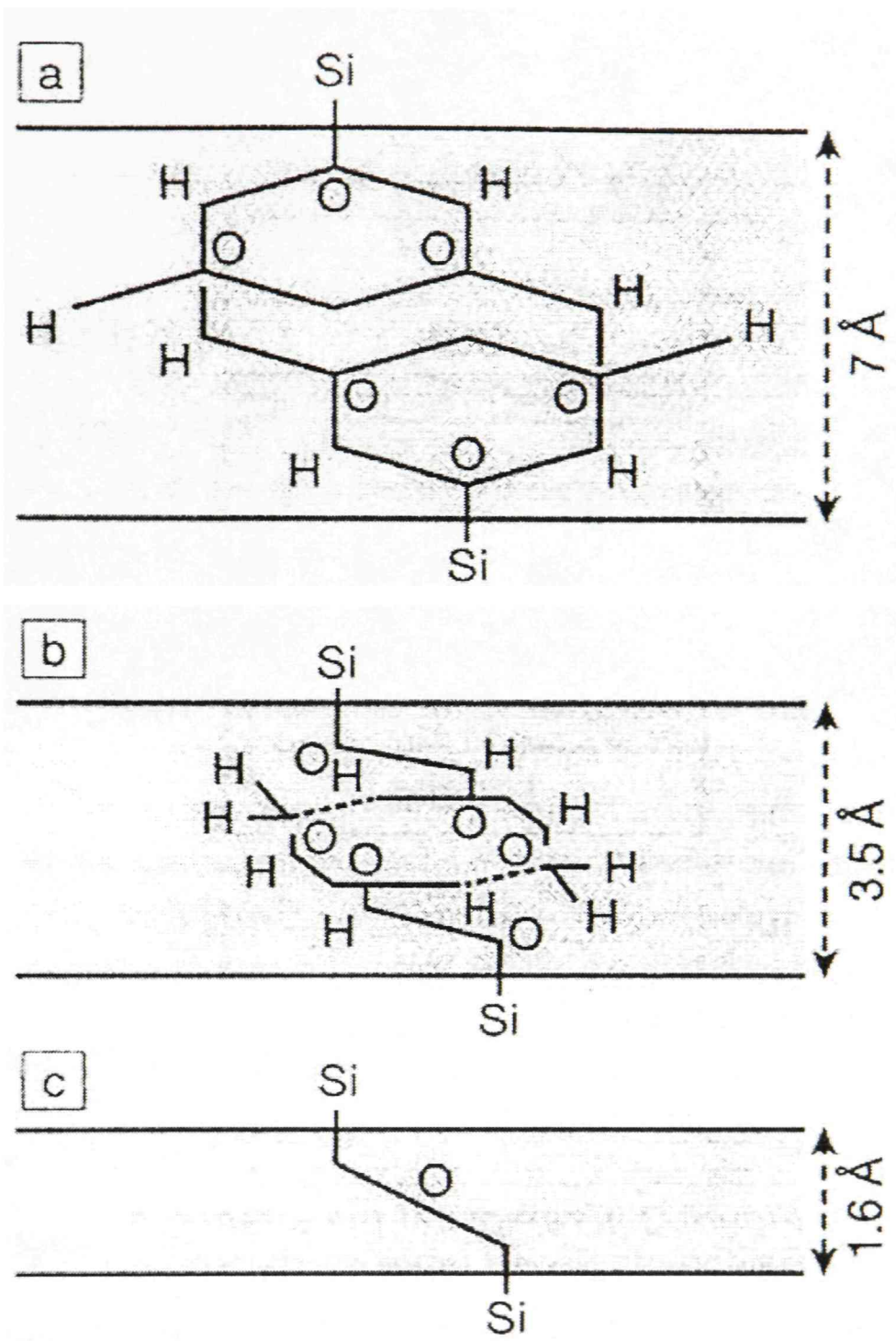
- " anodic bonding" or "electrostatic bonding"

These terms refer to bonding in the presence of an electric field.

2.2.1 Wafer Fusion Bonding

In fusion bonding, or silicon direct bonding, the polished sides of two silicon wafers are contacted face to face and the wafer pair is annealed at high temperatures. During annealing, a bond is formed between the wafers, which can be as strong as bulk silicon.

The process is carried out in two steps. First, the wafers are cleaned in a strong oxidizing solution. A strong RCA clean process is often used, consisting of an organic clean, HF dip, and ionic clean. This procedure results in a hydrophilic wafer surface. After an RCA clean, the wafers are rinsed in DI water and dried. Second the wafer surfaces are squeezed together for bonding at room temperature in air or in a sufficiently clean environment (normally in a clean room) in order to avoid particles between the wafers. On contact, the wafers will stick firmly together due to hydrogen bonding of hydroxyl groups and Van der Waals forces on the surface of the wafers. The bonding strength is one or two orders of magnitude lower than is typical for covalent bonding. The bonded pair is then annealed in oxygen. The anneal must be at a high temperature of more than 1000°C, because the bond becomes stronger at higher temperatures. Hydrogen is freed from the surface hydroxyl groups and diffuses out from between the wafers. Si-Si or Si-O bonds are formed across the bonding interface. Typical anneal times are about one hour. The fusion bond is very stable and the bond exhibits little dependence on time. Figure 2.10 shows the change of the interface structure during the annealing process. Figure 2.11 shows the interface of a well-bonded wafer pair.



(a) Room temperature bond: $SiOH:(OH_2)_2:(OH_2)_2:HOSi$

(b) T = 200 °C bond: $SiOH:HOSi+(H_2O)_4$

(c) T > 700 °C bond: $SiOSi + H_2O$

Figure 2.10. Proposed models for silicon wafer bonding at different temperatures ranges [20].

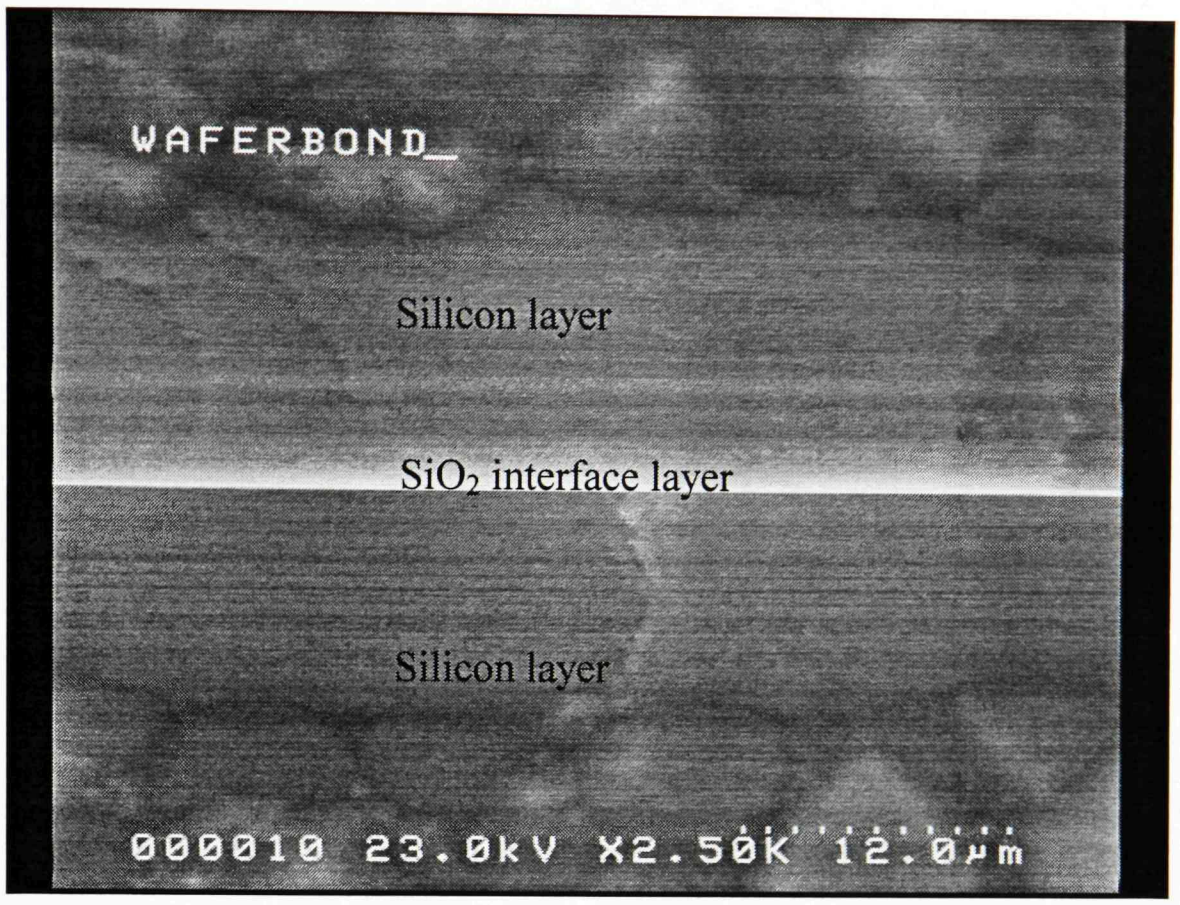


Figure 2.11. Cross section of directly bonded silicon wafer

There are several variations to the silicon direct bonding process [21]. In addition, silicon dioxide coated surfaces may be used for bonding. If both wafers are micromachinined prior to bonding, then it is necessary to align the wafers prior to bonding. One of the most common problems associated with wafer bonding is the occurrence of unbonded interface areas termed "voids" or "interface bubbles," The causes of bubbles during room-temperature bonding include: (1) particles on the bonding surface, (2) localized surface protrusions, (3) localized absence of sufficient density of bonding species, and (4) trapped air pockets. Figure 2.12 shows bubbles formed during bonding.

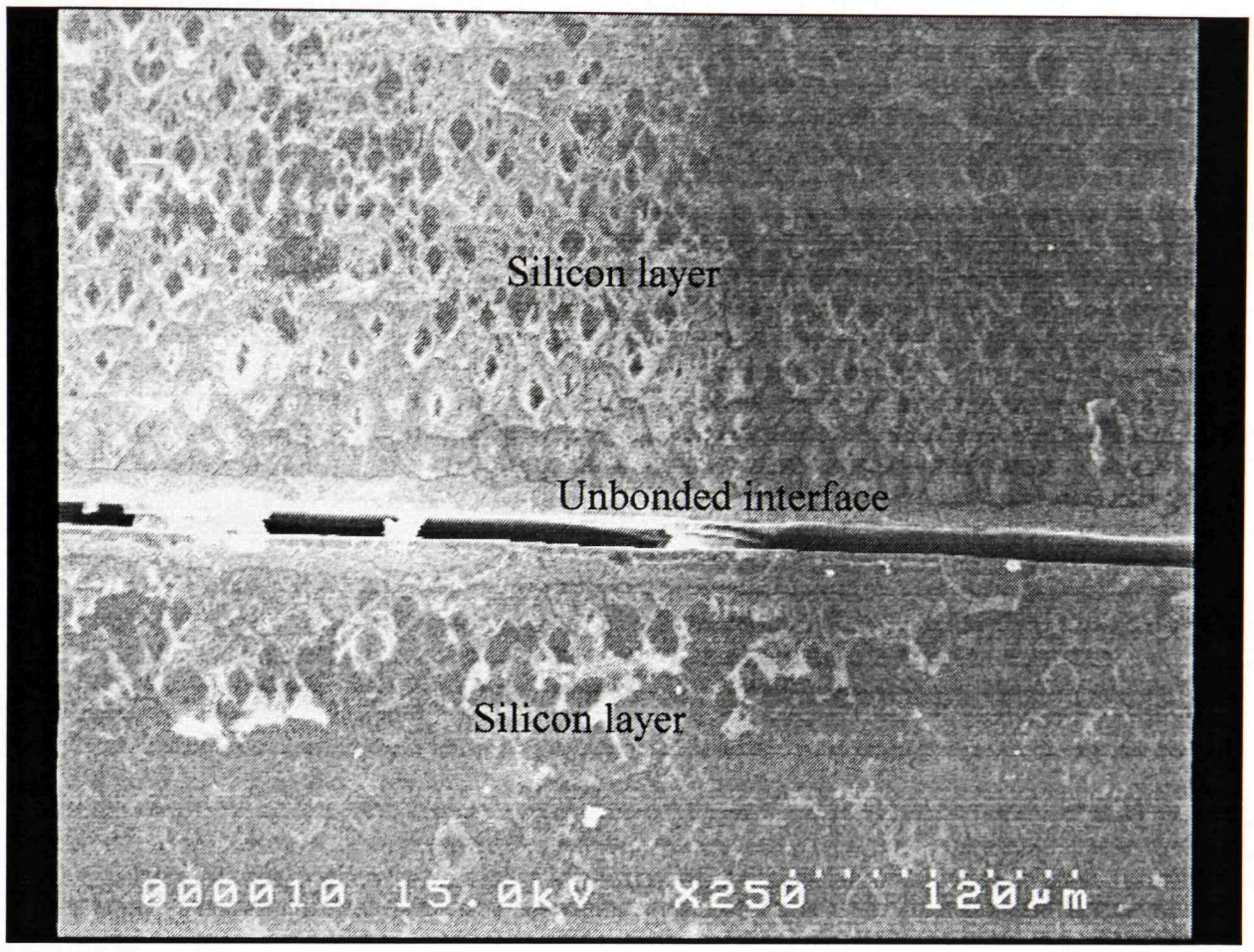


Figure 2.12. Voids formed during direct wafer bonding

2.2.2 Anodic Bonding

Silicon anodic bonding, or electrostatic bonding is used to bond silicon to glass. A polished silicon wafer is placed face to face with a glass wafer with a high content of alkali metals. With the help of an elevated temperature and high voltage, a permanent bond can be created. If a silicon wafer is coated with a sputtered glass, anodic bonding is possible for two silicon wafers. Anodic bonding is possible under atmospheric conditions as well as in vacuum. The following requirements must be met for this to occur:

- The glass must be slightly conductive in order to build up a space charge region.
- The temperature must be well below the softening point of glass.
- The native or thermally grown oxide layer on the silicon must be thinner than 200 nm.
- The thermal expansion coefficients of the bonded materials must match in the process temperature range.

Anodic bonding is performed in a temperature range of 200-500°C. A large voltage (500-1500V) is applied across the substrates. The glass is held at the negative potential. Figure 2.13 shows a typical configuration of anodic bonding systems. Figure 2.14 shows an actual system.

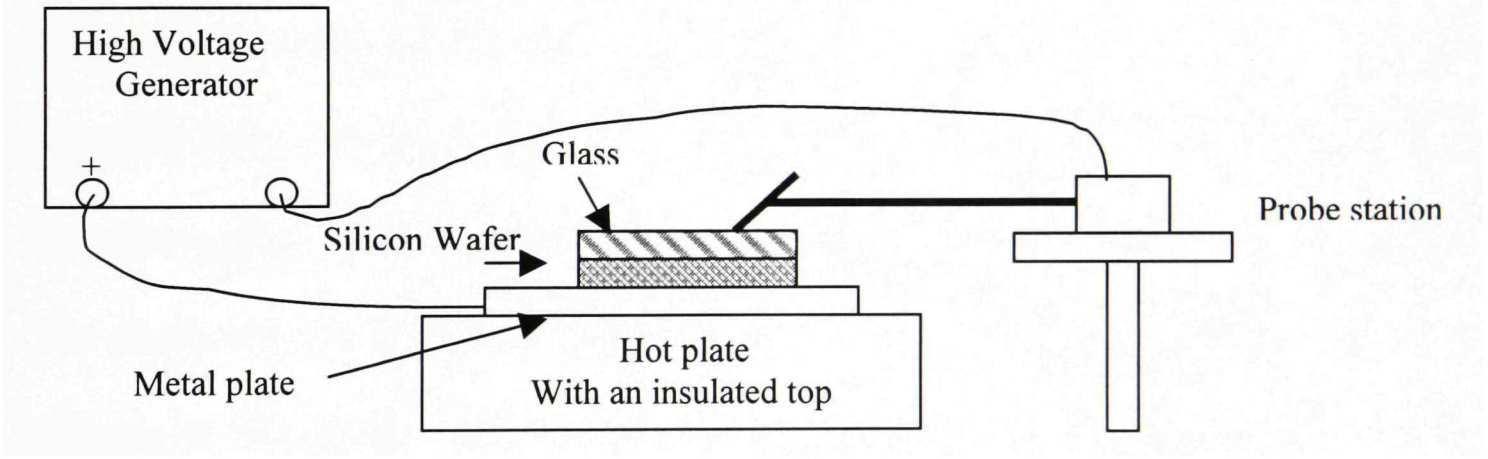


Figure 2.13. Configuration of an anodic bonding system

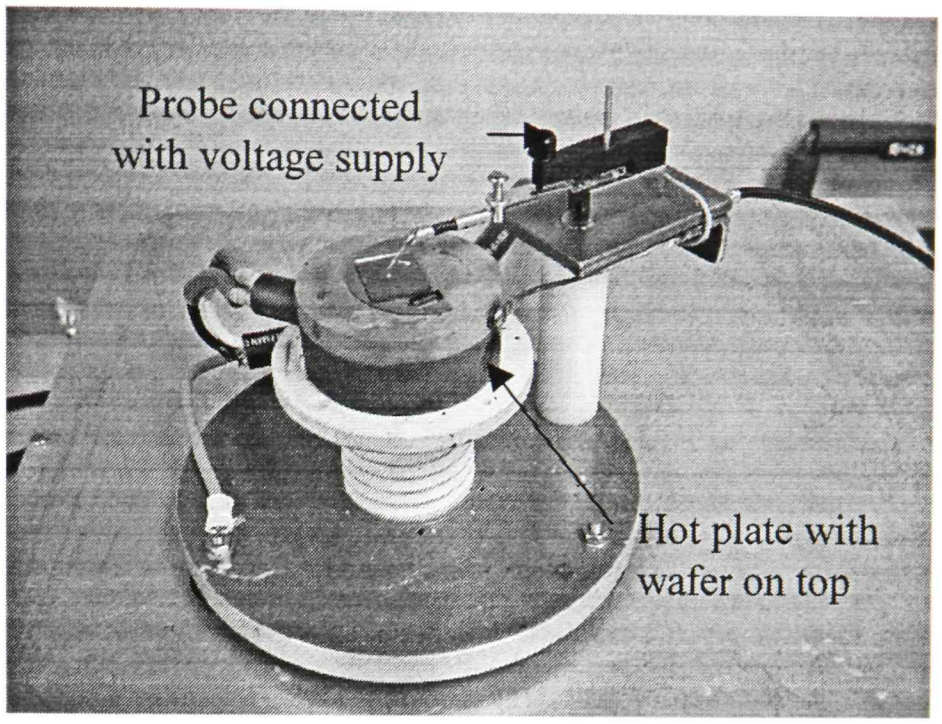
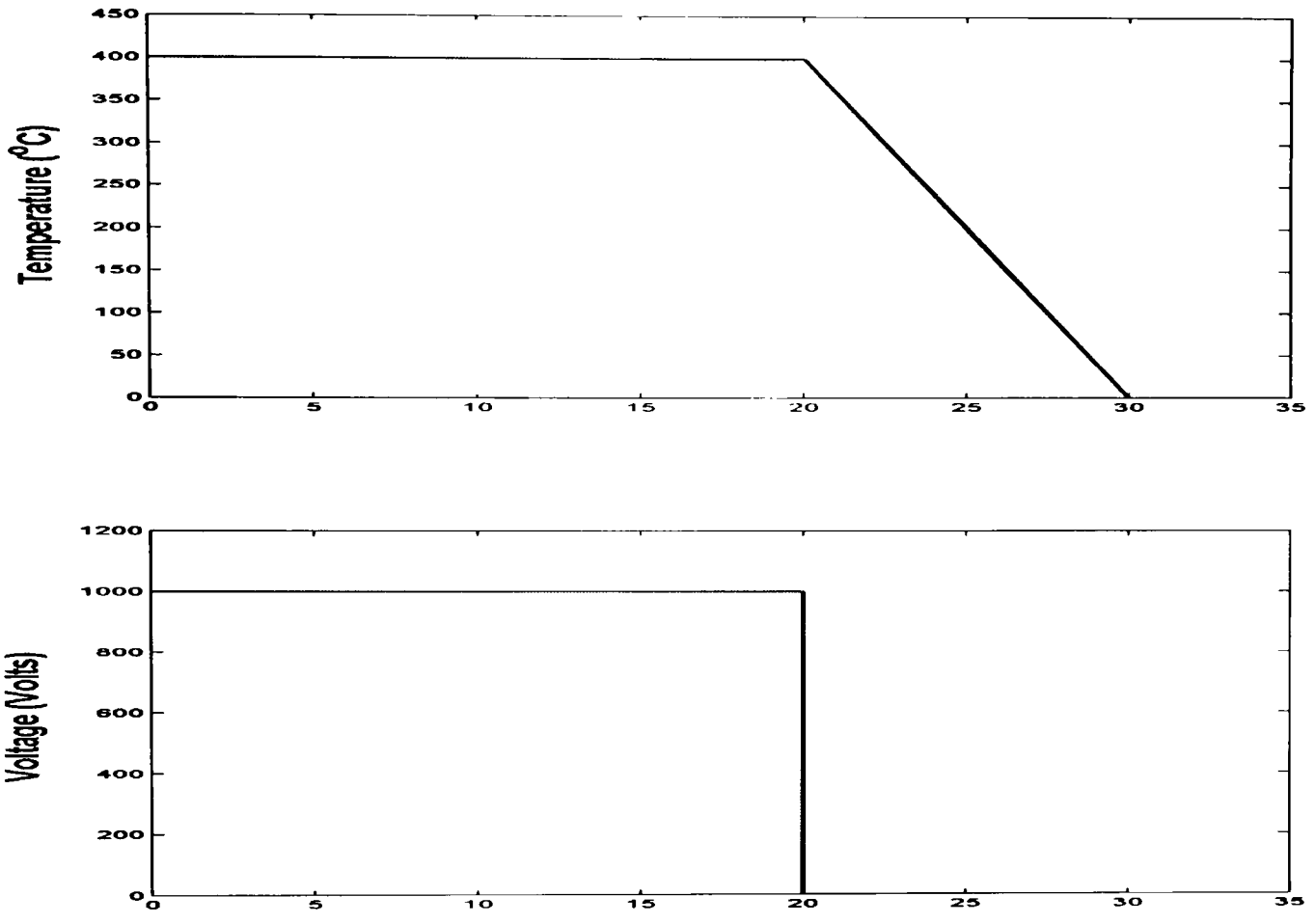


Figure. 2.14 Structure of anodic bonding system

The reason to apply high voltage and elevated temperature lies in the fact that high temperatures make the sodium ions in glass becoming mobile. Under great negative potential across the glass, the sodium ions in the glass are forced to migrate away from the silicon-glass interface and towards the cathode, leaving behind fixed negative charges. The electrostatic attraction between the fixed negative charges in the glass and positive charges in the silicon force the two substrates into intimate contact, and facilitates the chemical bonding of glass to silicon. (The oxygen atoms are bonded with silicon in the silicon wafer.) When the ion current vanishes, the bonding is complete, indicating that all mobile ions have reached the cathode. The bonding is permanent and a hermetic seal is formed. Figure. 2.15 shows ideal anodic bonding procedure, and Figure 2.16 shows the surface of a bonded Si/glass pair.



Notice that the current has a peak at the very beginning, then decrease rapidly. It shows that the movement of alkali ions under applied voltage.

Figure 2.15. Anodic bonding parameters

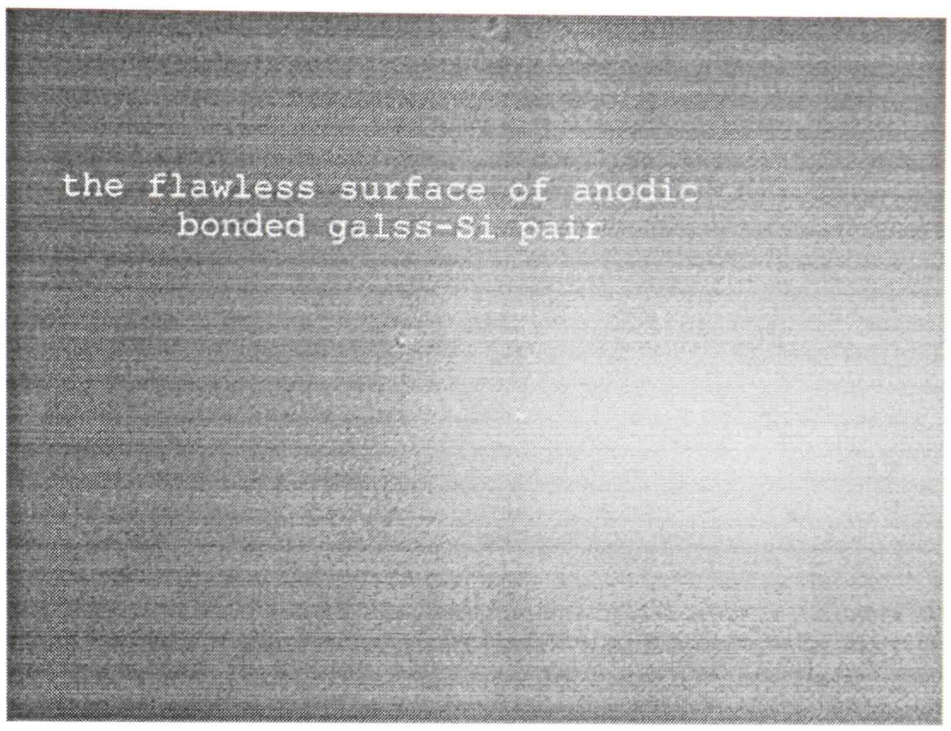


Figure 2.16. Surface of an anodically bonded glass/Si pair

Anodic bonding is quite popular for making MEMS devices since it can bond sodium-rich glass to silicon with good adhesion strength at lower temperature than fusion bonding, allowing the metal layer to survive. It can introduce thermal strain due to different coefficients of thermal expansion between silicon and glass.

The glass selection is important in anodic bonding. First, the glass should be polished, though the requirement for smoothness is not as critical as in fusion bonding, because the high electrostatic forces will pull small gaps into contact. Second, the glass should have a thermal expansion coefficient that matches that of silicon. A large difference in the thermal expansion coefficient will result in stress causing the bonded pair to bend, or worse, to crack. Pyrex 7740 is the preferred glass, because it has the

most closely matched thermal expansion coefficient to silicon. Third, the thickness of the glass wafer should be as thin as possible to induce large electrostatic forces.

2.2.3 Inspection of wafer bonding

Several ways can be used to determine the quality of the wafer bonding.

2.2.3.1 Interface etching. In this detection approach, the bonded wafer pairs are cut into pieces. The cross section of bonded Si/Si pairs is etched by a KOH aqueous solution. The bonded pair must have sufficiently high bonding strength to withstand the dicing and etching process. After etching in 50% KOH at 85°C for 10 min, a clear, straight etching groove can be seen at the interface when no bubbles exist. At unbonded areas, KOH etches preferentially, resulting in etched holes deeper than the groove. This method can only decorate the interface at the cross section and is used to investigate very small bubbles. That is destructive and time consuming.

2.2.3.2 Optical observation. The most commonly used method is based on optical transmission. We know that when the energy of incident light photons is smaller than the band gap energy E_g of the material under observation, the material is transparent to that kind of light ($\lambda > hc / E_g$).

To view the image with the light of wavelength λ, a detector that is able to sense the wavelength must also be employed. Since the silicon has a band gap energy of 1.12 eV at room temperature, light in the infrared region can pass through silicon. An IR lamp and an IR viewing camera are thus employed.

CHAPTER III

MICROMACHING PROCESS EXAMPLE

3.1 Micro-Channel on Silicon Wafer

Almost all bulk micromachined structures have channels or grooves in a silicon substrate. These channels or grooves can be implemented several ways. The most common way is by wet etching. The following process steps describe how to make a straight-line channel in a <100> orientated silicon wafer.

The process begins with a thermally grown layer of silicon dioxide on a silicon wafer. Two wafers are prepared. 9000 Å of oxide is grown on one of the silicon wafer surfaces. This is done by wet oxidation at 1100°C for 4.5 hours. 4500 Å of oxide is grown on another silicon wafer surface. This is done by dry oxidation at 1100°C for 3 hours and 45 minutes.

Next, photolithography is used to form the required pattern on the silicon surface. Two masks are prepared. The masks are printed gold foils on a transparency film. The line widths are 50 and 280μm, respectively. The shape of the masks is shown in Figure 3.1.

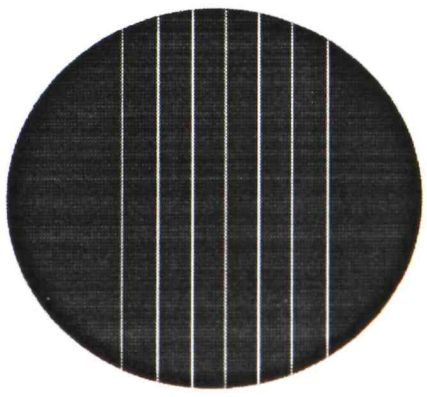


Figure 3.1 Mask used for channel making

Lithography is done by this process sequence of spin on coating of photoresist, soft bake, expose, develop, and hard bake. The process parameters are:

- Spin speed is 5000 rpm, soft bake (120 °C for 1 minute),
- Exposure time 30 seconds,
- Develop 25 sec in diluted developer solvent (1 part developer concentrate and 1 part of DI water), then the wafer is rinsed by DI water for 1 min.
- Hard bake at 150 °C for 10 minutes.

In order to obtain smooth sidewalls in the final channel structure, alignment should be done carefully to ensure the pattern orientation is parallel to the <110> orientation. Otherwise, the resulted sidewall will be composed of pieces of <111> orientated side walls, making the sidewall zigzag shaped.

In case of deep channel etching, the back side of the silicon wafer needs to be protected. This is done by coating photoresist on the back side of silicon as well. In order to protect the front patterned photoresist layer, the backside coating is normally done before front side coating.

The next step is opening etch windows in the SiO_2 layer. This is done by HF wet etch. To make the reaction stable and controllable, buffered HF is used rather than pure HF. Because glass is etchable by HF, Teflon containers and tweezers are used.

Because SiO_2 is hydrophilic and Si is hydrophobic, we can see the completion of the SiO_2 etch by watching the wafer surface. If the patterned area is free of water, SiO_2 is completely etched. Sometimes, when the pattern is too small, water will stick to that area

even though it is free of SiO_2. In that case, the surface can be examined by a white light illuminated microscope. The silicon has a white color while SiO_2 is yellow or brown.

After etching, the wafer is removed from the ecthant and rinsed with DI water for 1 minute. The photoresist is washed away by acetone, methanol, and DI water. Finally, the wafer is blown dry with nitrogen.

Sometimes, the photoresist is too thick to clean by the recipe mentioned above. In that case, the wafer can be bathed in H_2SO_4 and H_2O_2 solvent (20 ml 96% H_2SO_4 and 20 ml 30% H_2O_2) at 60 °C for 10 min, This recipe can clean photoresist and other organic contamination effectively. After this step, the cross section of wafer is as shown in Figure 3.2.

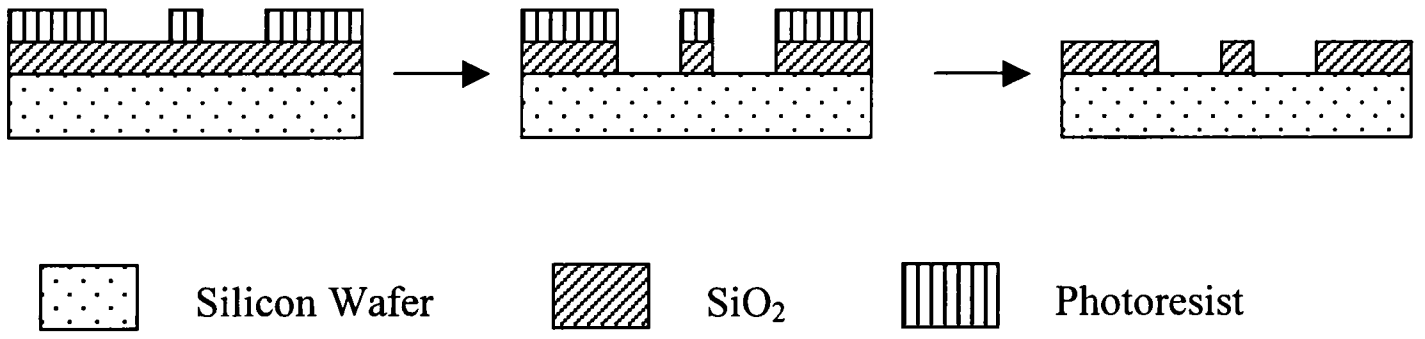


Figure 3.2. Open etch window for silicon wet etch

The final step is to use KOH etchant to wet etch silicon to form the micro channels. Different KOH concentrations and different temperature were chosen for these two wafers. The one with 4500 Å oxide is etched by 44 weight % KOH at 85°C until the SiO_2 is gone. The one with 9000 Å oxide is etched by 50 weight % KOH at 70°C until the SiO_2 is gone. The results are shown below in Table 3.1 and Figure 3.3.

Table. 3.1 Results of wet etching Silicon wafer

Sample	1	2
Oxidation Thickness (nm)	450	900
Etch condition	44% KOH 85°C	50% KOH 70°C
Etch time (hr)	0.82	6.3
SiO_2 Etch rate (nm/h)	555	140
<100> plane Etch Rate (nm/h)	75	26
<100>:(<111> plane Etch rate (nm/h)	16:1	2:1

The etch result for the first sample is shown in Figures 3.3 and 3.4. Because the etch window is only 50 μm, the etching is self-limited on the <111> plane and forms a V-groove. The sidewall is very smooth.

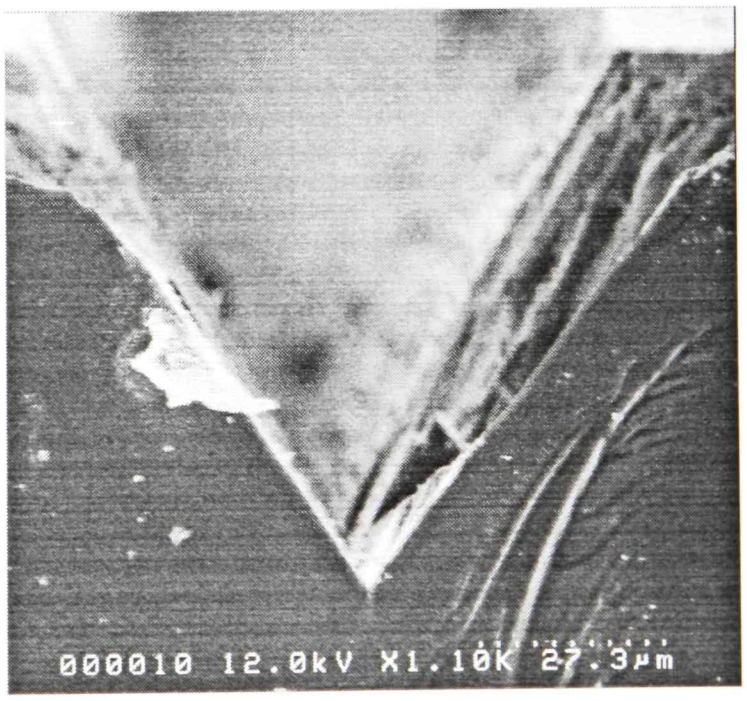


Figure 3.3 SEM photo of Cross section of a self-limited V-groove

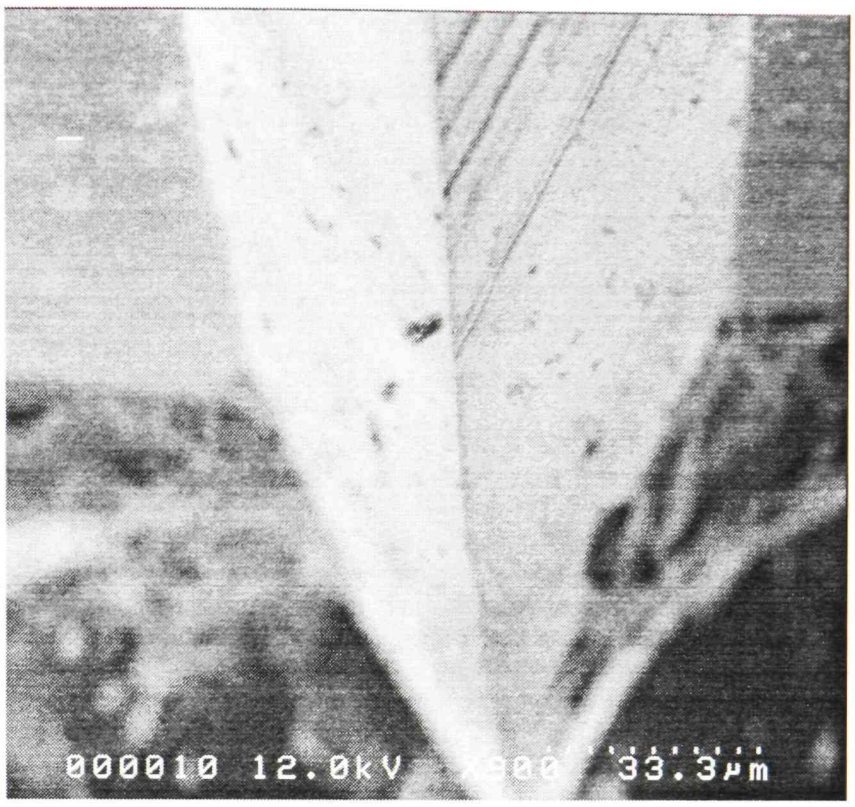


Figure 3.4 The inside view of V-groove sidewall

The etching result of the second sample is shown in Figures 3.5 and 3.6. Because the etch window is very big, the etching is not self-limited and forms a V-groove. Because the etch opening is misaligned with the <110> plane, the sidewall is composed of many overlapped <111> planes rather than a smooth sidewall. For the same reason, etching also happened on fast etching planes like the <311> plane. The undercut was big and the final opening reached 382 μm, much larger than the original 280 μm.

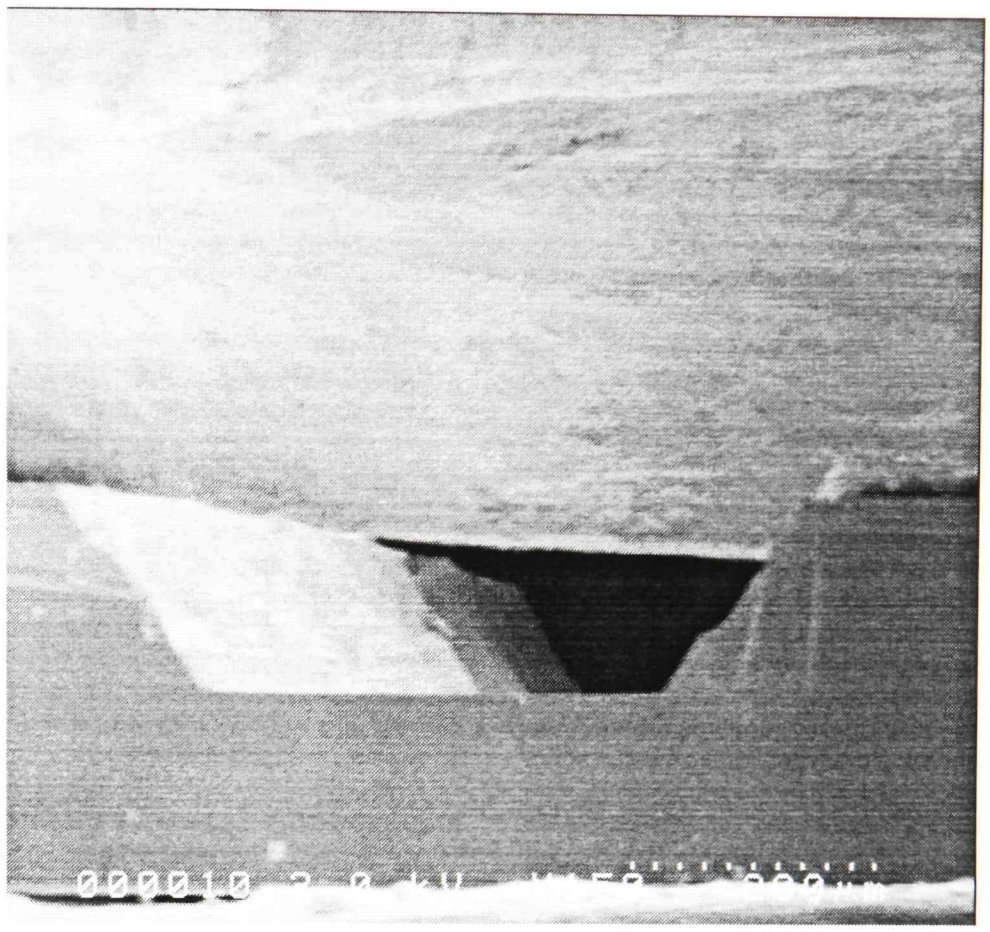


Figure 3.5 Cross section of channel.

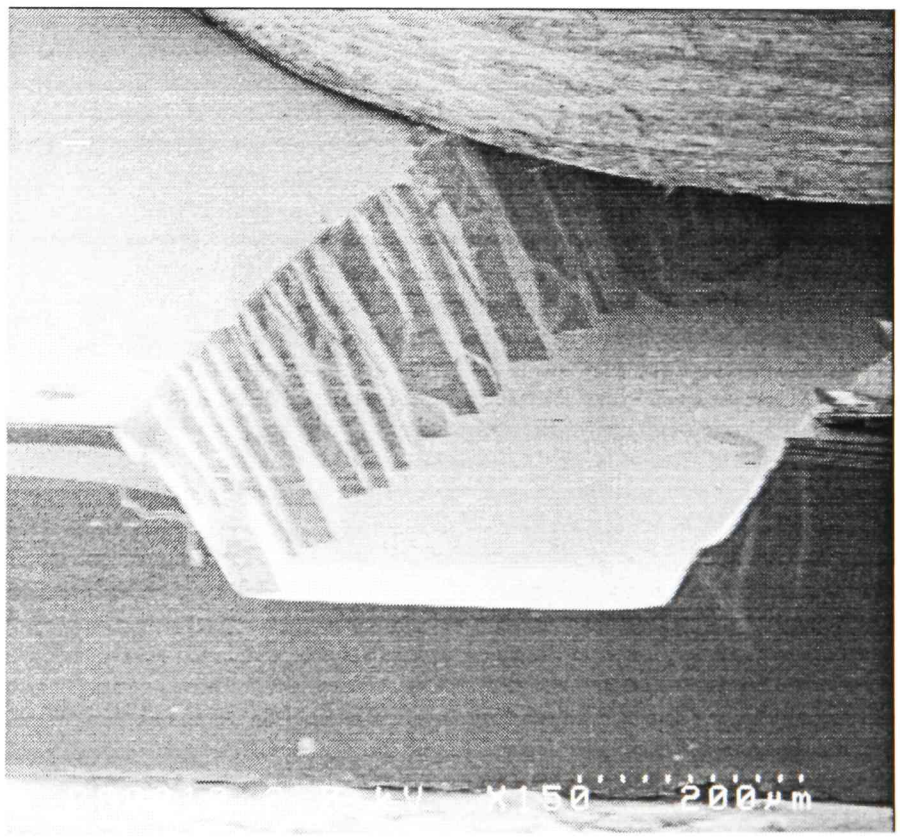


Figure 3.6 View of sidewall.

3.2 Micro-Channel in Glass Wafers

In order to make a fluid based separation system, a process for etching channels in glass wafers was developed. Microscope slides were chosen as the substrate material and their chemical compositions are listed in Table. 3.2.

Table. 3.2. Chemical composition of microscope slide

Chemical	Percentage
Silicon dioxide	72.2
Sodium Oxide	14.3
Calcium Oxide	6.4
Magnesium Oxide	4.3
Aluminum Oxide	1.2
Potassium Oxide	1.2
Sulfur Trioxide	0.3
Iron Oxide	0.03

From Table 3.2, it is shown that the major part of the glass slide is SiO_2, so buffered HF is chosen as the etchant. Photoresist was chosen as the mask, so only one etch step was used. The whole process can be shown graphically as in Figure 3.7.

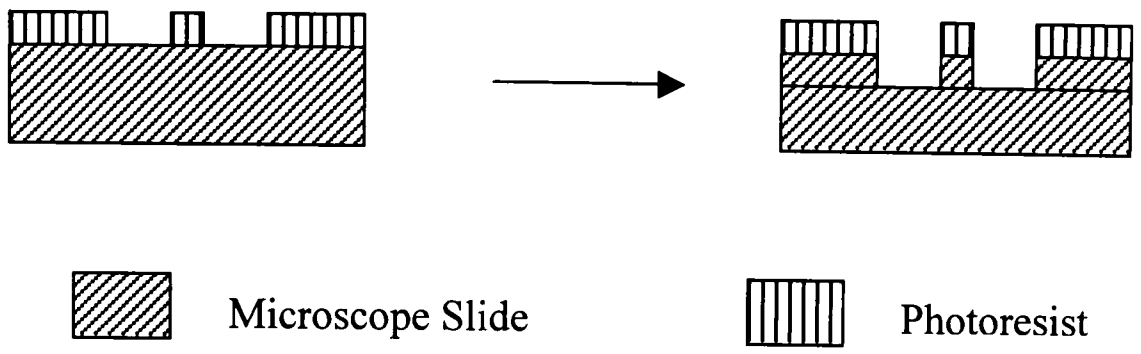


Figure 3.7. Process flow for etching channel in glass slides

The process begins with spining on a coating of photoresist on a glass slide. Because photoresist will act as an etch mask as well, a low spin on speed (1000rpm) is chosen and coating is repeated two or three times to achieve a thick layer.

Next, the wafer is soft baked, exposed, developed and hard baked to transfer the mask pattern into the glass. The parameters are:

- Soft bake at 120°C for 1 minute,
- Expose 30 seconds by hard contact mode,
- Develop in 1:1 developer solvent for 40 seconds,
- Blow dry and hard bake at 150°C for 10 minutes.

After the hard bake, the wafer is cooled down to room temperature. Then the wafer is immersed in a buffered HF solvent.

It was found that photoresist is not an optimal mask for HF etching of glass, because the photoresist does not adhere well to the glass surface. It cracked or had pinholes after a certain period of etching. HF penetrated the resist layer and etched the glass surface, thus causing the glass surface underneath to be etched as well.

Experiments show that the maximum time the photoresist layer can stay un-attacked is only about 30 minutes. In order to etch deeper channels into the glass substrate, the etchant is normally heated, Table 3.3 shows the etch rate at different temperatures.

Table 3.3 Etch rate of glass in BHF etchant under different temperatures

Sample No.	Etch temperature (°C)	Etch Rate (nm/min)
1	22	60
2	60	420

A BHF etch of SiO_2 is almost isotropic, so the expected channel shape was semi round. However, the resulting etched shape is severely deformed from the expected shape (shown in Figure 3.8). The reasons for this are the high concentration of impurities, and the lack of agitation of the solution during etching.

Figure 3.8 Channel shape after BHF etch

3.3 Wafer Fusion Bonding of Two <100> Silicon Wafer

Silicon wafers with or without thermal oxidation can be bonded together through direct bonding. The force leading to bonding was mainly short-range and intermolecular.

The silicon wafer (with or without thermal oxidation) bonding process can be summarized as a three-step sequence: conditioning, bonding, and annealing.

Conditioning makes the wafer surface clean and hydrophilic, so the bonding can happen at room temperature. The process is composed of several steps of acid bath cleaning, which is commonly called RCA cleanup. It is consists of RCA1 and RCA2. Table 3.4 shows their composition and operation parameters.

Table 3.4 Composition of Standard and Modified RCA1 and RCA2 cleaning and operating conditions

	RCA1	Modified RCA1	RCA2
Compositions by Volume	$NH_4OH:H_2O_2:H_2O$ =1:1:5	$NH_4OH:H_2O_2:H_2O$ =0.01~0.25:1:5	$HCl:H_2O_2:H_2O$ =1:1:6
Operating Temperature (°C)	75~85	70~75	75~85
Operating Time (min)	10~20	5~10	10~20
Function	Remove particles, organics, some metals	Remove particles, organics, some metals	Remove Alkali and heavy metals

Modified RCA1 is used instead of standard RCA1 to avoid microroughening of the silicon surface. Normally, the RCA clean is carried out by a sequence of modified RCA1 followed by RCA2. However, the experiment shows that a reverse RCA clean (RCA2 followed by modified RCA1) is also acceptable. Between the two RCA cleans, an optional diluted HF dip can be done to insure the elimination of SiO_2, the process parameter is dipping into 0.5% HF for 10 seconds.

Some papers suggest activating the wafer by immersing in a nitric acid bath (75%) at 95°C for 30 minutes. However, it has proven to be very hazardous because many acid fumes are emitted during bathing. More importantly, this step did not help much in activating the wafer. To make thing worse, it often made the wafer surface rough. Therefore, this step was eliminated from the clean steps.

After the RCA clean, the surface of the silicon wafer showed hydrophilic characteristics. Water sticks to the silicon surface. The wafer was blown dry with a nitrogen gun and the bonding was done immediately. Because the silicon surface was now activated and very prone to dust and other particles, this step was carried out inside the cleanroom to decrease the chance of contamination. The two wafers were placed surface to surface and an initial force is applied in the center of the wafer. Normally, the tip of the tweezers was used to apply the force. The bonding begins at that point and spread out like a water wave. The whole process usually took only a few minutes. The activated wafers stuck to each other immediately and the bonded pair could be held by tweezers vertically, and did not slide apart from each other. At that time, the bonding

strength was small and the wafer pair could be separated easily by inserting a blade into the interface. If the wafers were put together, they could be bonded again.

Annealing followed to increase the bonding strength and to make the bonding permanent. The bonded pair was put into an oxidation oven at 1100°C and kept there for one hour.

After annealing, the bonded pair was so strong that its strength can be in the same range of bulk silicon. It was diced and underwent other process steps. Figure 3.9 shows a bonded wafer pair.

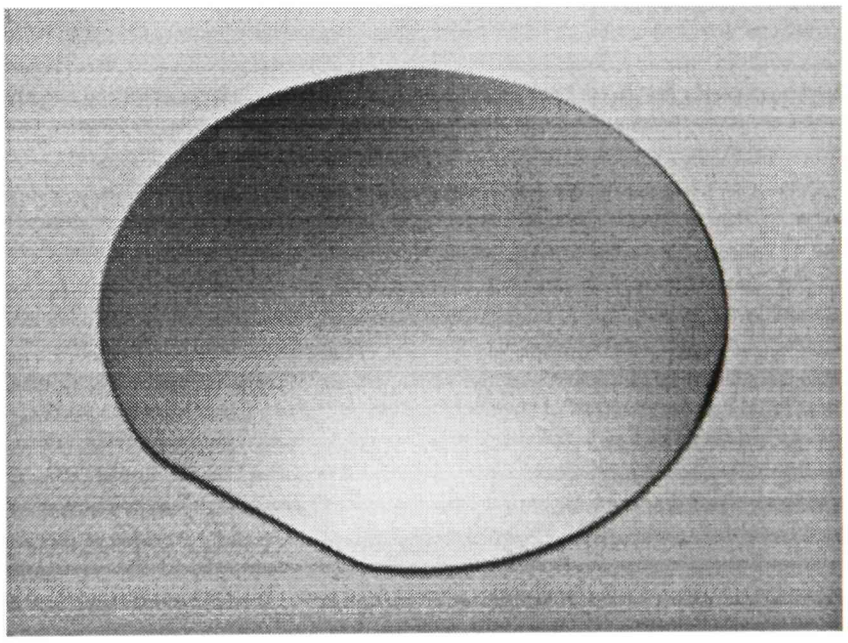


Figure 3.9. The bonded wafer pair

Normally, IR inspection is used to check the quality of bonding, because silicon is transparent to IR light. The bonded area and unbonded area show different color. This method is straightforward and the inspection system is simple.

Since an IR inspection system was not available in our lab, the interface inspection method was used to check the bonding quality. The bonded wafer pairs were cut into pieces, the cross section of the bonded Si/Si pair was etched by a KOH aqueous solution. After etching in 50% KOH at 85°C for 10 min, a clear, straight etched groove can be seen at the interface when no bubbles exist. At unbonded areas, KOH etches preferentially, resulting in etched holes deeper than the groove. This method can only decorate the interface at the cross section and is used to investigate very small bubbles. It is destructive and time consuming.

3.4 Glass-Glass Direct Bonding

Glasses are also found to have the ability to be bonded together through direct bonding. They are bonded together mainly by melting. The Cole-Palmer microscope slides are selected for this purpose. Table 3.5 shows the physical properties of this kind of glass slides.

Table 3.5 Physical Properties of Microscope slides for glass bonding:

Property	Value
Annealing Temperature	545°C
Softening Point	720°C
Strain Point	494°C
Density	2.48 gm/cm^3

The glass (microscope slide in the experiment) bonding process was primarily the same as silicon wafer fusion bonding. Three steps, surface cleaning, bonding, and annealing were also necessary.

Surface cleaning was also done by a RCA clean. Forward and reverse RCA cleans worked well for cleaning the slides surfaces. Table 3.4 can be used for a reference. After cleaning, the glass slides were rinsed thoroughly in DI water; then nitrogen was used to dry the slides. The glass slides were free from organic, metal and alkali particles.

Glass piece bonding is different from wafer bonding in that glass pieces can not be bonded solely by the attraction between the two surface. After the two clean glass slides were put into contact face to face, even pressure was used to help keep the two surfaces in intimate contact. Figure 3.10 shows the pressure system used for glass bonding.

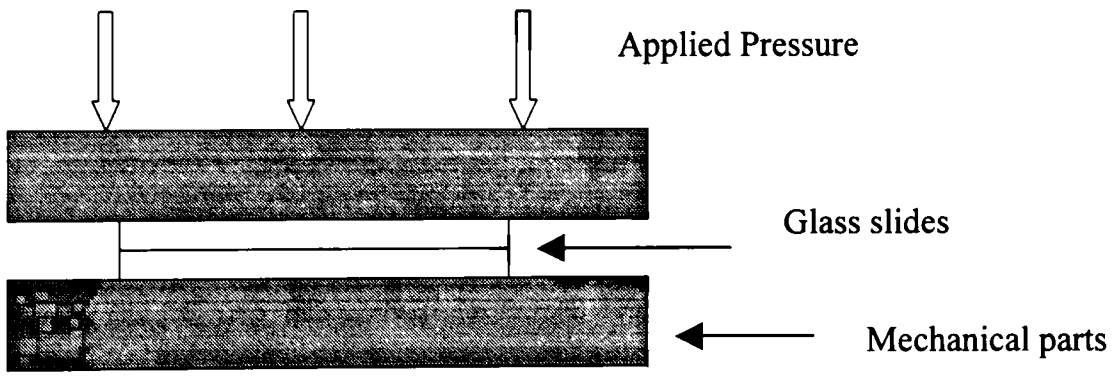


Figure 3.10. Pressure system for glass bonding

Then, the glass pairs were moved into a heated oven for at least 4 hours. The temperature was kept at around 500°C for this kind of glass slide. A slow cool down was needed to avoid cracking the glass slides.

Channels can be made on glass by HF etch, holes can be added by drilling directly on glass pieces. The final bonding result will not be affected. Figures 3.11 and 3.12 show a bonded glass pair with channels in between.

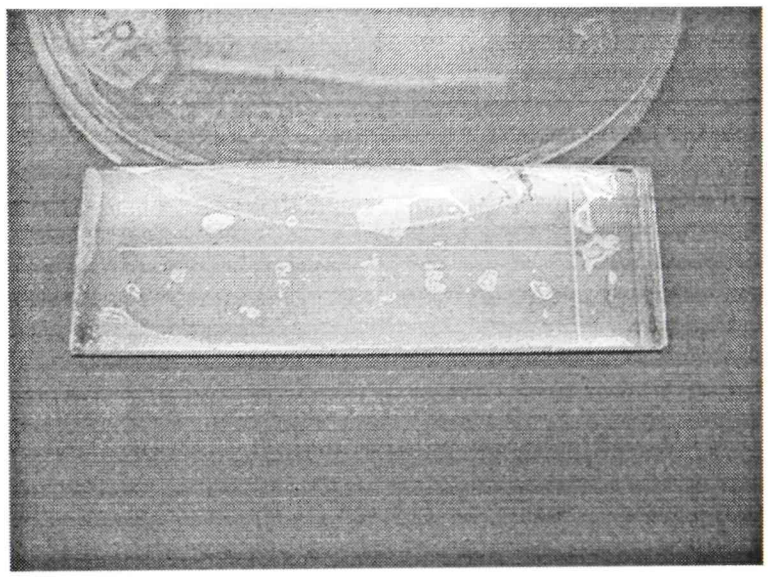


Figure3.11. Bonded glass pair

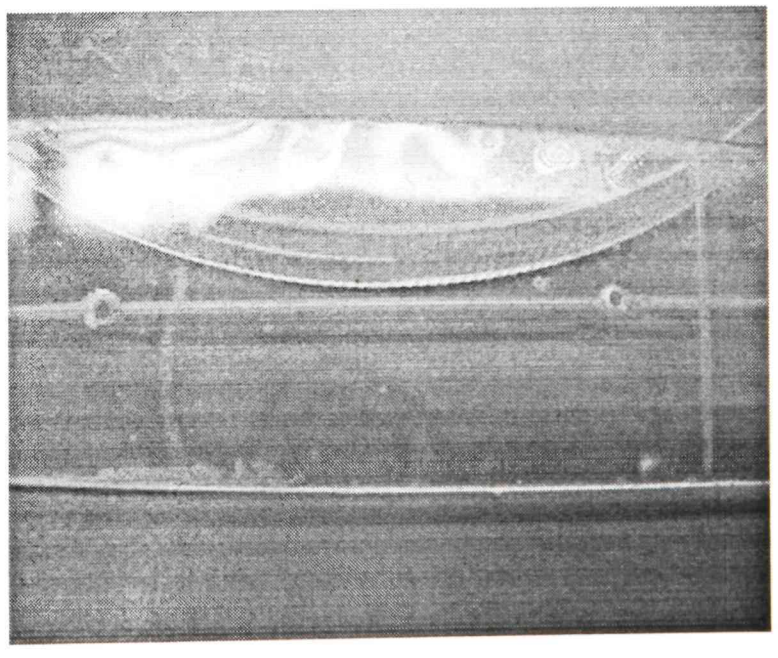
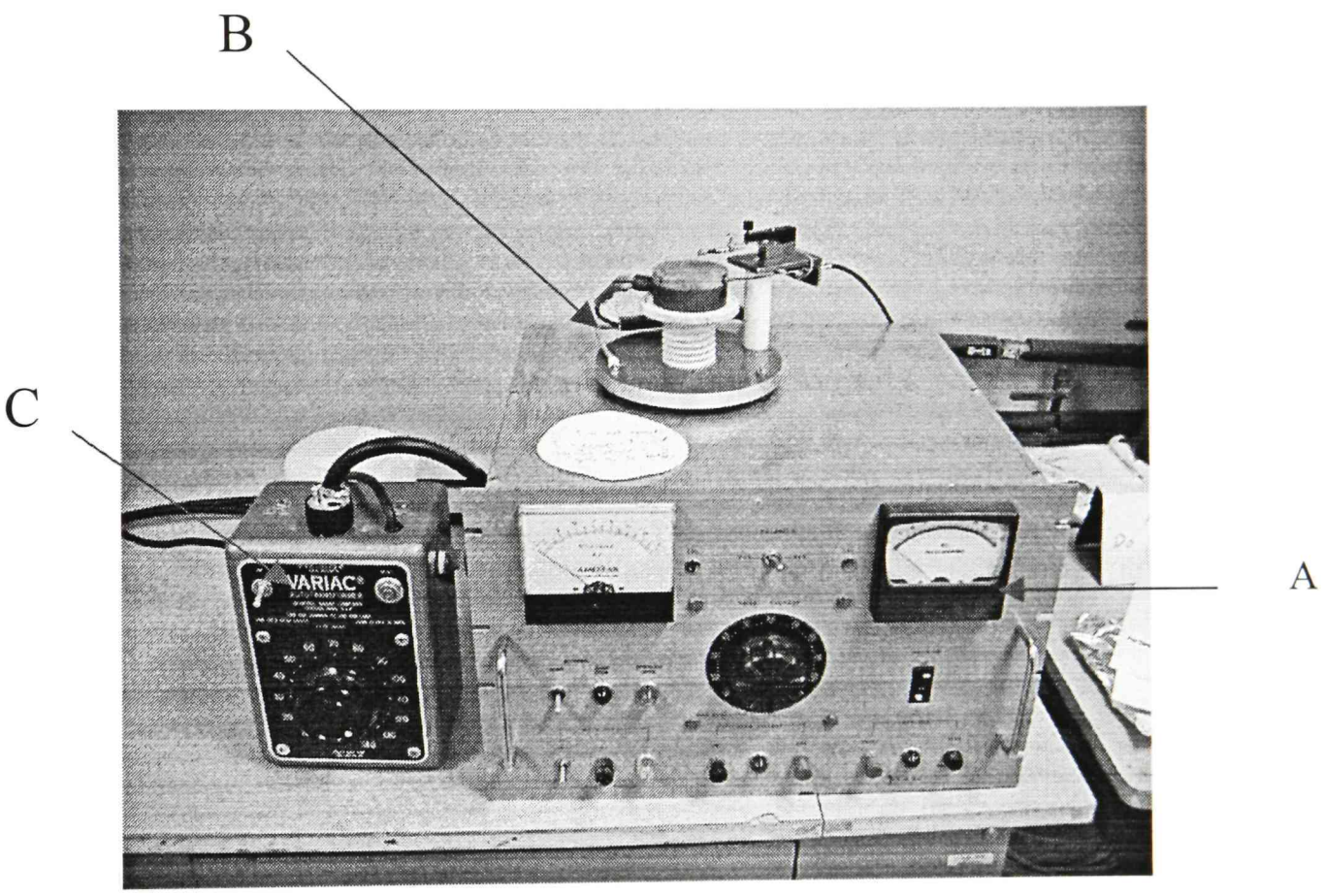


Figure3.12. Bonded glass pair with channel and holes.

3.5 Anodic Bonding of Silicon Wafer and Glass Wafer

Anodic bonding can bond silicon to glass by placing a glass wafer on top of a silicon wafer, heating the pair up to around 300°C, and applying a high voltage to press them into intimate contact. An anodic bonding system has at least three parts: heating plate, high voltage generator, and probe station. The anodic bonding system used in our experiment is shown as in Figure 3. 13.



A: High Voltage Generator B: Heating plate C: Voltage transformer

Figure 3. 13. Anodic bonding system

To insure an accurate control, calibration is needed before bonding. A multi-meter was used to measure the error of the internal voltage meter of the high voltage generator.

then the reading of that internal meter was calibrated by adjusting the zero-offset knob. Using a temperature probe, the relationship between the output voltage of the voltage transformer and the surface temperature of the bonding platform surface was established.

After calibration, the circuit was connected and checked. Wires were separated from each other so that no short would happen and the polarity was correct. In order to have a particle free bonding platform, the bonding platform surface was cleaned by ethanol before heating up.

The silicon wafer and glass wafer should be cleaned before bonding. This was done by a normal acetone and methanol clean. An ultrasonic cleaner was used to help remove particles from the wafer surface. After cleaning. The wafers were dried using a nitrogen gun.

The silicon wafer/glass pairs were put on top of the heating platform. The silicon wafer was put under the glass wafer (see Figure 3.14 as an example). The power to the heating coils was turned on. The platform is heated by slowly increasing the supply voltage. The voltage was increased by approximately 10 volts every 3 minutes. The heat was increased up until the surface temperature reached around 350°C (supply voltage set around 50V).

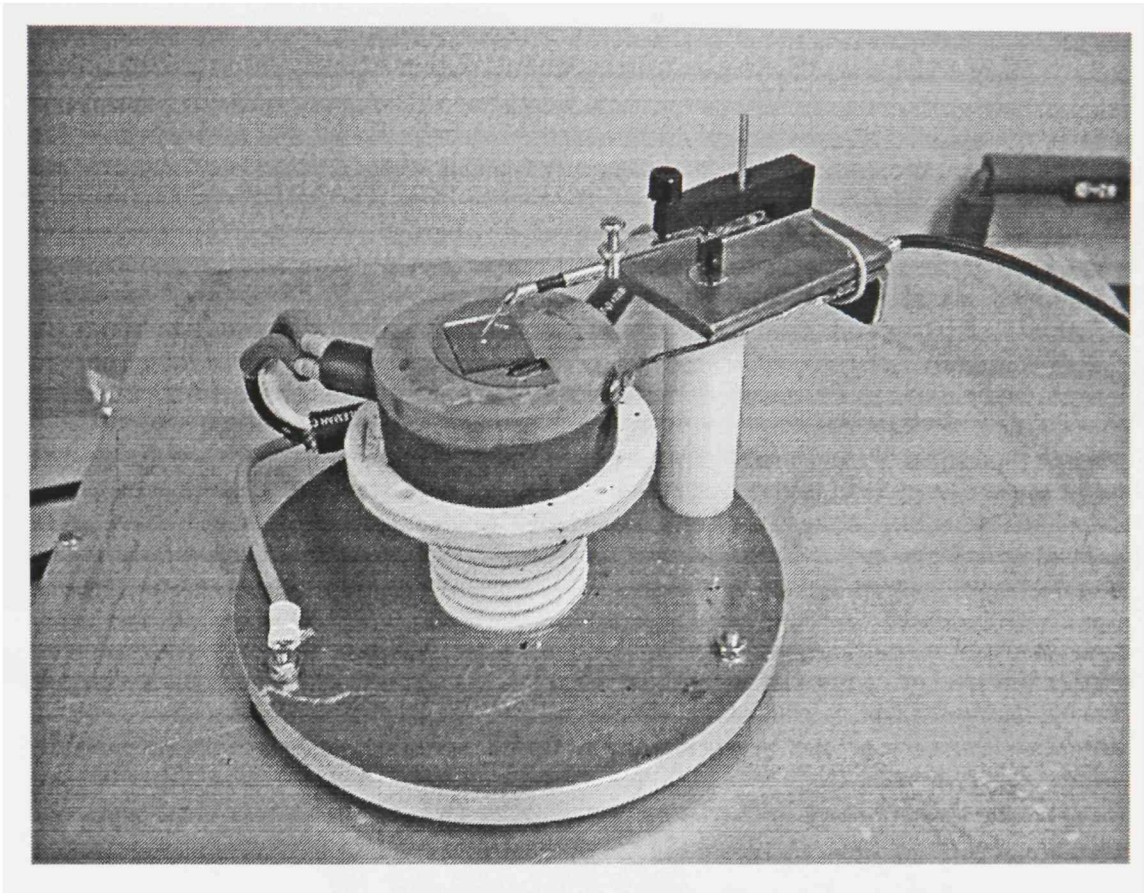
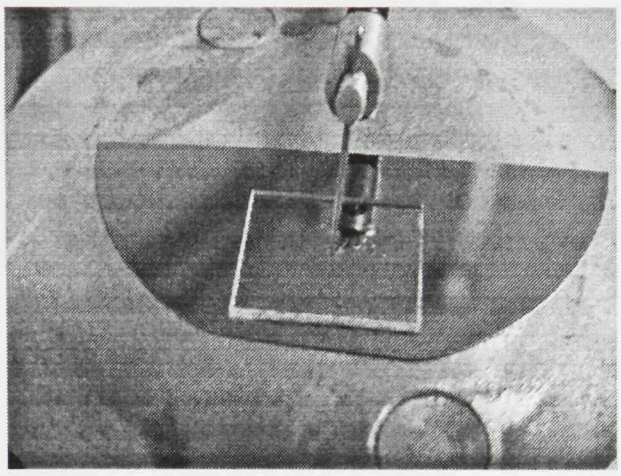
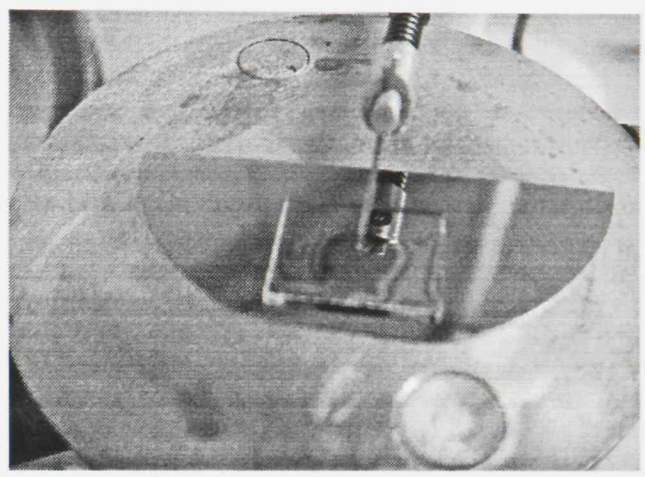


Figure 3.14 Detail of bonding area

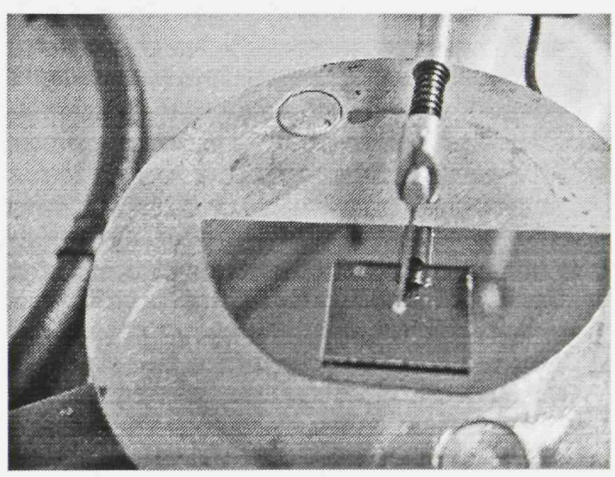
After the wafer pair had been heated up to the desire temperature, the high voltage was applied. This was done by pressing the negative voltage connected probe onto the glass surface and using a layer of aluminum foil to help the electrical field spread. The bonding voltage was applied slowly (approximately 100V/min) until it reached 1000V. The voltage was applied for about 6 minutes. Normally, the bonding begins at once with the application of voltage. It can be observed by the color change of the bonding surface. The bonded area was brown while other areas were not. Because the point probe is used, the bonded area spreads from that point to the outside and the trapped air is squeezed out (see Figures 3.15 and 3.16).



Before applying high voltage



5 seconds after applying high voltage



6 minutes after applying voltage

Figure 3.15. Bonding process of anodic bonding

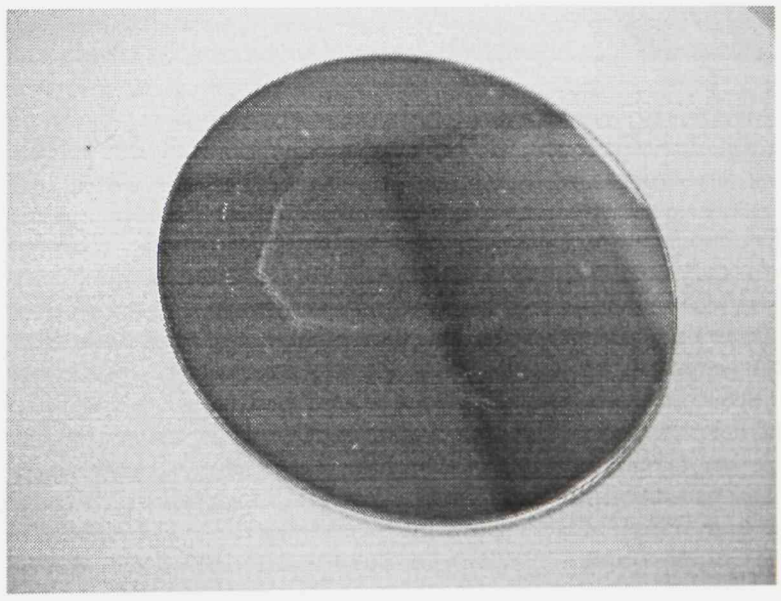


Figure 3.16. Bonded glass-silicon pair

After the bonding is completed, the high voltage was turned off first, and then the heating power was reduced very slowly to zero in about 25 minutes, so the bonded pair could be cooled down. The final step was turning off the power of all equipment and cleaning the working area.

The advantage of anodic bonded parts was that the glass itself was a dielectric material, so no dielectric film was needed at the interface. More important, the bonded parts have no parasitic capacitor, which is an excellent feature for electrical related sensors. The accelerometer mentioned in Chapter VI is such a component. Its measurement was based on the change of capacitor. A low parasitic capacitor is essential to its measurement.

CHAPTER IV

MICROMACHINING PROJECT

4.1 Introduction

MEMS based accelerometers are some of the most widely used sensors. It was chosen for fabrication to employ the most commonly used MEMS processing steps. The project began with the design and simulation of the accelerometer [22], followed by developing proper process step. The final testing step is also included.

4.2 The Working Principle

There are several types of MEMS based accelerometers. We have chosen the capacitive type and fabricated it using a bulk micro-machining process. It can be symbolized as shown in Figure 4.1. The device makes use of a cantilever with a plated end-mass. Acceleration causes the cantilever to vibrate at some amplitude, which is measured by capacitive means. A schematic diagram for the main part of the accelerometer is illustrated in Figure 4.2.

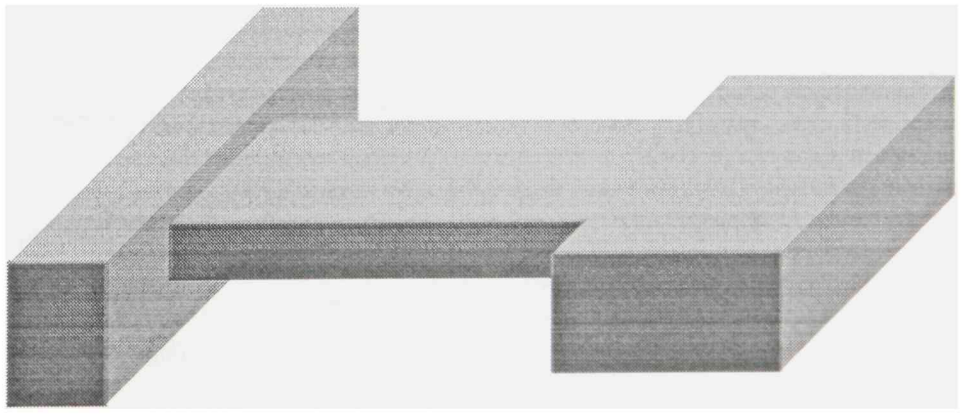


Figure 4.1. Structure of main part of accelerometer

The structure can be modeled as follows.

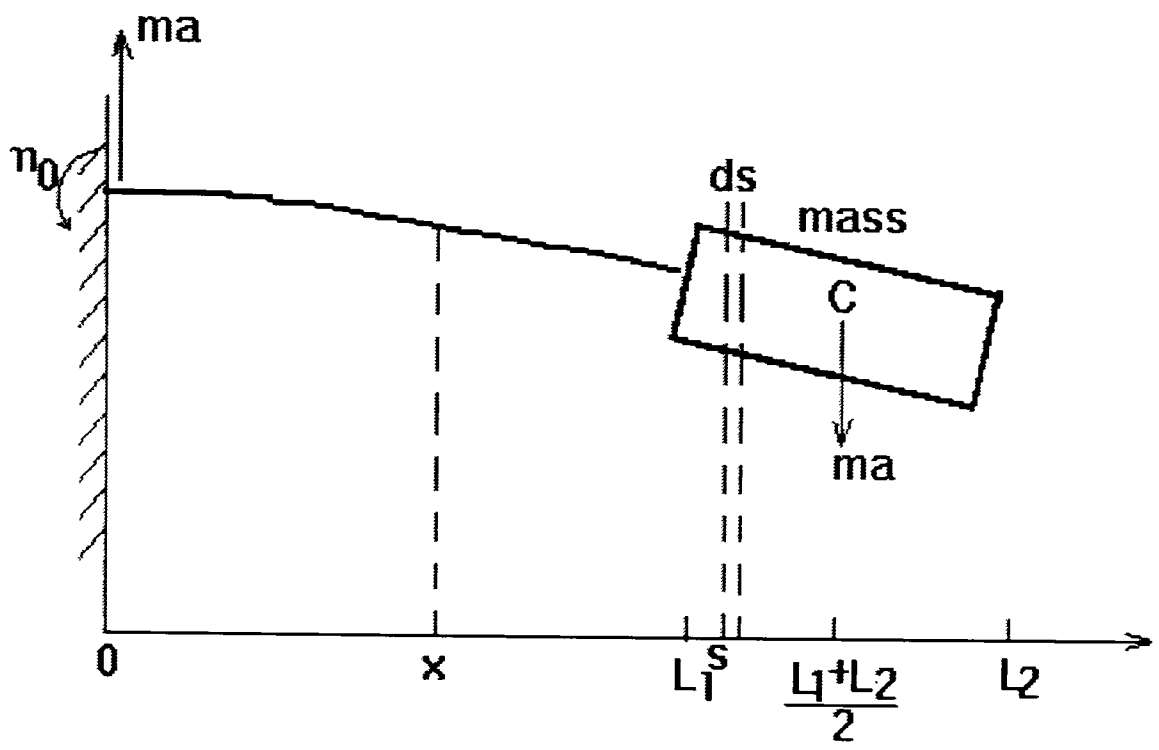


Figure 4.2. Physical model of accelerometer

Considering the beam, we get:

$$-EI_1 y_1'' = M_1(x) = -m_0 + m*a*x \qquad 0 < x < L_1 \ . \tag{4.1}$$

Considering the end mass, we get:

$$-EI_2 y_2'' = M_2(x) = -m_0 + m*a*x - \int_{L_1}^{x} \rho * b_2 * h_2 * a * (x-s)ds \quad L_1 < x < L_2 . \tag{4.2}$$

The boundary conditions of these differential equations are:

$$y_1 \mid_{x=0} = 0$$
$$y_1'' \mid_{x=0} = 0$$
$$y_2'' \mid_{x=L_2} = 0 .$$

Solving these equations, we get:

$$y_1' = \frac{ma}{2EI_1}[(L_1 + L_2)x - x^2]$$
$$y_1 = \frac{ma}{12EI_1}[3(L_1 + L_2)x^2 - x^3] \quad , \tag{4.3}$$

where:

y_1: the displacement of the beam center from balance point

y_2: the displacement of the mass from the balance point

m: accelerometer mass

a: acceleration

L_1: the length of the beam

L_2: the length from the center of mass to the root of the beam

E: Young's modulus Silicon (170 GPa)

I_1: rotational inertial moment of the beam

I_2: rotational inertial moment of the mass

$$I = (1/12)bh^3$$

b: Width of the beam

h: thickness of the beam.

The displacement of the mass at the center is the combination of the beam and mass displacements.

$$y_c = y_1|_{x=L_1} + y_1'|_{x=L_1} * (\frac{L_2 - L_1}{2}) = \frac{ma}{12EI_1}(L_1^3 + 3L_1L_1^2) \tag{4.4}$$

By substituting for a with the gravitational constant of acceleration g, we get the displacement sensitivity of the accelerometer per g:

$$S_{th} = \frac{mg(L_1^3 + 3L_1L_1^2)}{12EI_1} \quad . \tag{4.5}$$

Considering the relationship between the distance and capacitance, we get the capacitance sensitivity of accelerometer per g:

$$S_c = \frac{\varepsilon_0 * \varepsilon * mg(L_1^3 + 3L_1L_1^2)}{12EI_1d^2} \quad . \tag{4.6}$$

Since no acceleration simulation equipment was available, we applied voltage across the device and used the induced electrostatic force to simulate acceleration. Two further formulas are:

1. the displacement sensitivity of the accelerometer to voltage :

$$S_d = \frac{\varepsilon_0 \varepsilon V^2 S(L_1^3 + 3L_1L_1^2)}{24EI_1d^2} \tag{4.7}$$

2. the capacitance sensitivity of the accelerometer to voltage :

$$S_c = \frac{\varepsilon^2{}_0 \varepsilon^2 V^2 S^2(L_1^3 + 3L_1L_1^2)}{24EI_1d^4} \tag{4.9}$$

where S is the bottom surface area of the end mass. After optimizing these parameters, we set the dimensions of the accelerometer to the values listed in Table 4.1.

Table 4.1 Optimized dimensions and parameters for the accelerometer

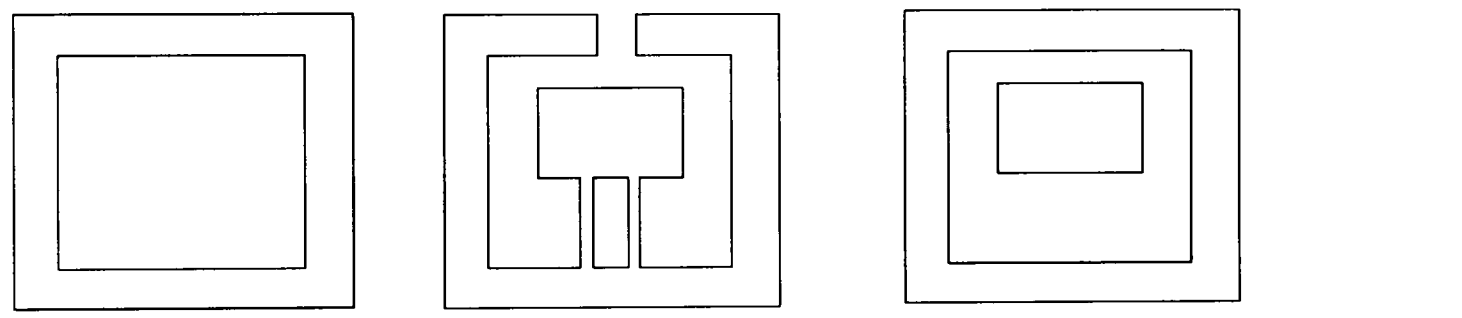
Parameter	Dimension
Width of beam (μm)	1400
Length of beam (μm)	2000
Thickness of beam (μm)	30
Width of Mass (μm)	3600
Length of Mass (μm)	3000
Thickness of Mass (μm)	280
Capacitance gap (μm)	20
Static Capacitance (pF)	2.16
Intrinsic Frequency (kHz)	2.18

4.3 Fabrication steps

The MEMS processing techniques involved in this project as follows.

Oxidation. Oxidation was important in this process procedure because it formed the mask for wet etching. Because deep and high quality wet etching was needed, thermal oxidation was chosen for the oxide grown.

Photolithography. Lithography was used to transfer the desired beam and end mass shape into silicon so that we could etch out the desired 3D structures. Three masks were used for this purpose. One extra mask was used to define the aluminum pad on the glass substrate. The mask patterns are shown in Figure 4.3.



(a) mask for first photolithography to form the capacitance gap

(b) mask for second photolithography to form the shape of beam

(b) mask for second photolithography to etch through the wafter and release the beam

Fig.4 Mask design for photolithography on Si

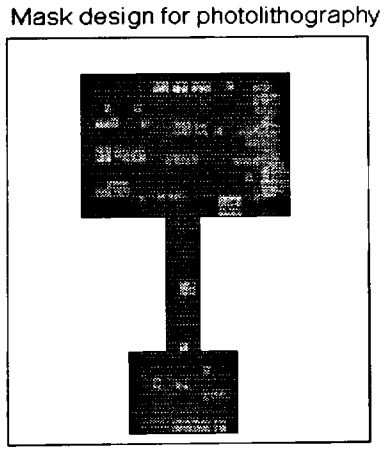
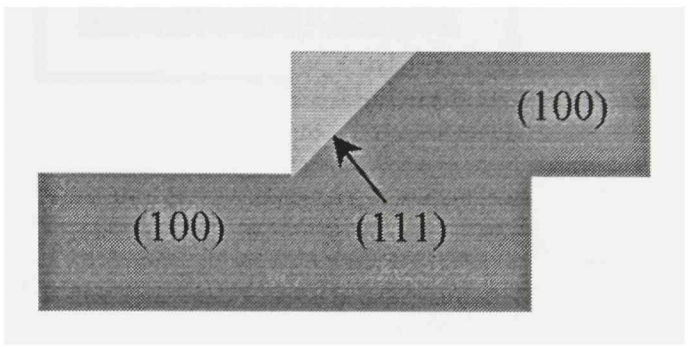


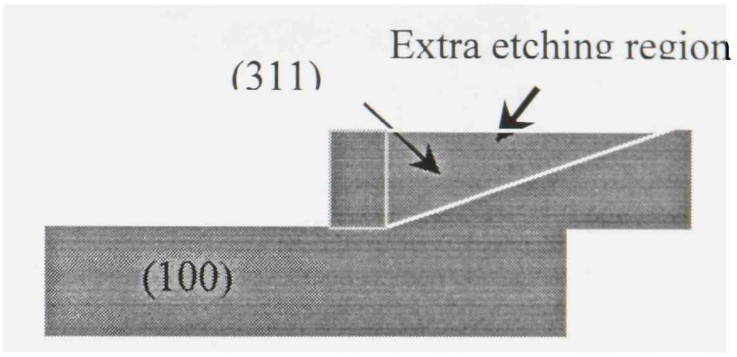
Fig.5. Photo-mask design for Al electrode (positive photoresist design)

Figure 4.3. Masks for accelerometer fabrication

Four points will be discussed regard to mask making, First, during a KOH wet etch, an undercut will occur along the <311> plane. The original beam design was two separated thin beams, which proved to eroded away because of a severe undercut. The two beams were revised into one wide beam, which can withstand the undercut during wet etch (Figure 4.4).



Ideal etch without undercut



Real profile after etch

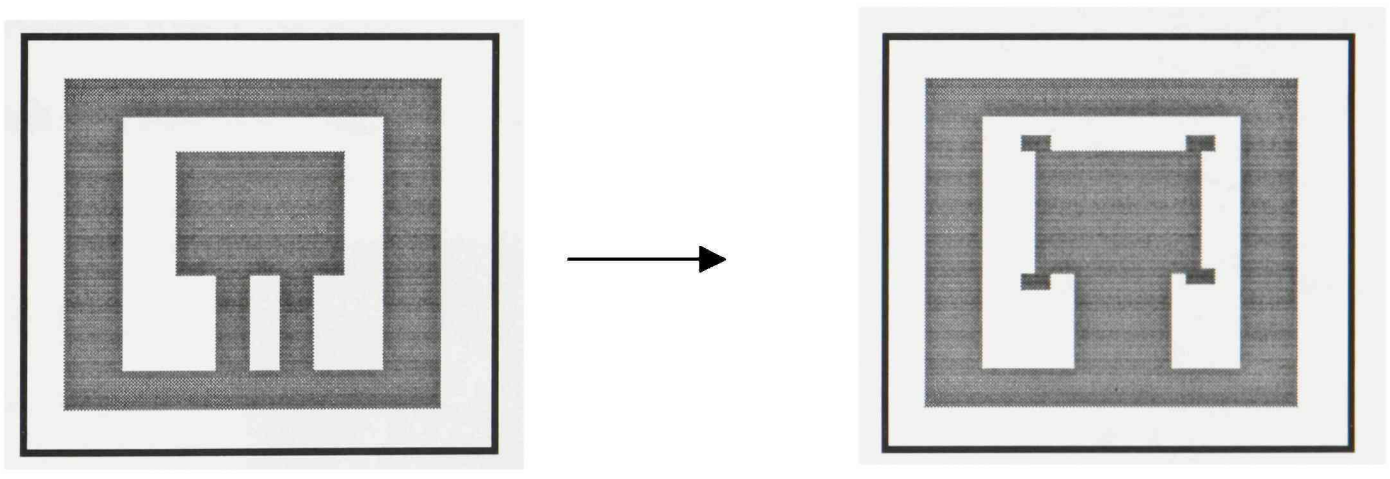


Figure 4.4 Undercut and revisement of beam

Second, because an undercut will happen during convex corner formation, compensation structures have to be added to the third lithography mask. The third mask was revised in the following way as shown in Figure 4.5.

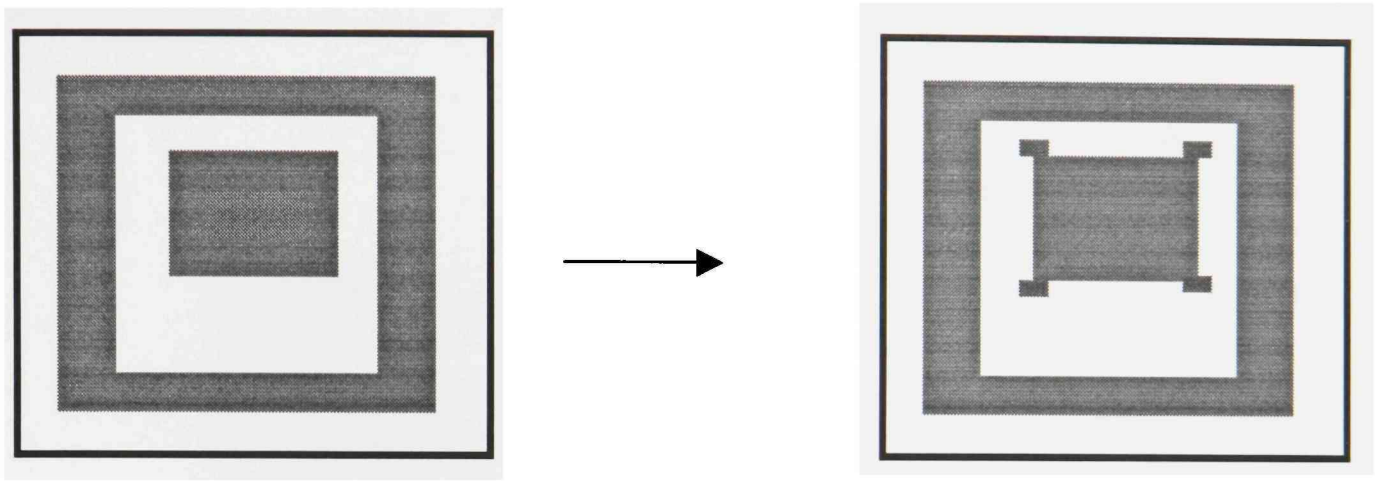


Figure 4.5. Compensation structures on the mask

Third, because double sided lithography equipment was not available, all etch processes were done from the front side of the wafer. During each lithography step, the mask was manually aligned to the prior pattern (Figure 4.6).

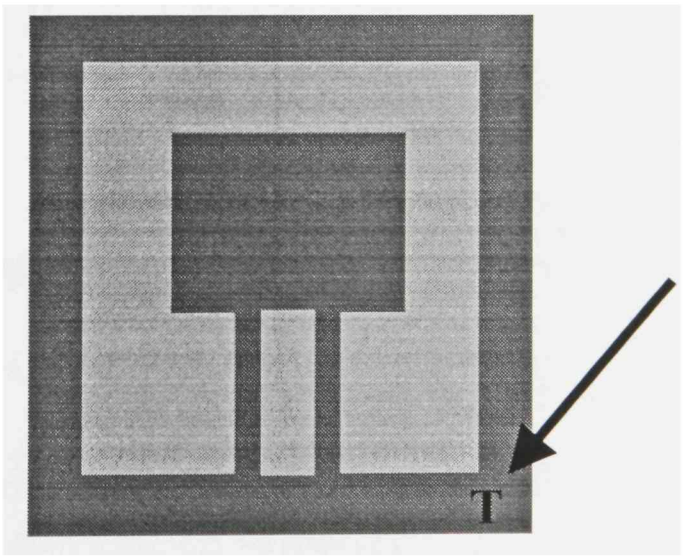


Figure 4.6. Alignment mark on the mask

Fourth, before packaging, the etched beam structure was too fragile to undertake intense shock, so a dicing saw could not be used to dice the wafer. The wafers were scribed and cleaned by hand. The mask considered for this purpose is shown in Figure 4.7.

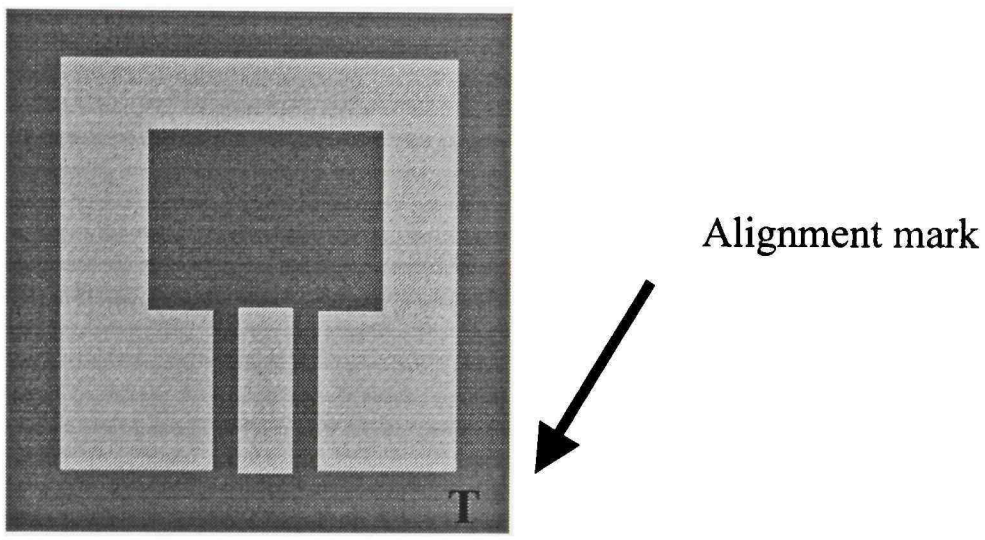


Figure 4.7 Etched groove for Dicing

KOH anisotropic wet etching. This is the most critical process used to form the desired 3D structures. Temperature, solution concentration and time were strictly controlled.

BHF SiO_2 etching. This step is used to open etch windows on the silicon wafer surface so the etch could be done with the required patterns.

E-beam thin-film deposition. This step was used to from a uniform aluminum layer on glass to form an electrical pad.

Aluminum metal etching. This step was used to form the metal pad shape. H_3PO_4 was used as an etchant.

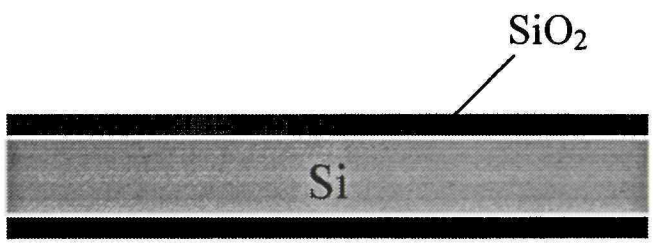
Si-glass anodic bonding. Silicon was bonded to glass to form a complete device. Anodic bonding was chosen to avoid using glue.

Diamond sawing. The glass wafer was cut into pieces by a diamond dicing saw.

Now, the overall process flow can be summarized as the following:

1. Clean silicon (100) wafer, the wafer thickness was around 280μm,

2. Double sided oxidation (SiO_2) by wet oxidation. The temperature is 1140°C and the thickness of SiO_2 expected was 2900 Å,

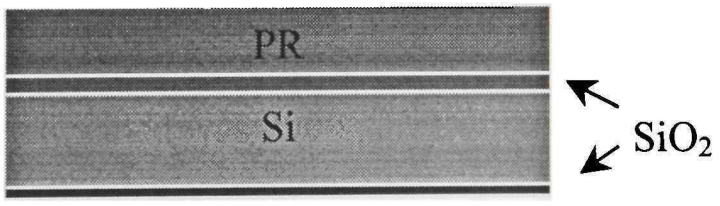


3. First lithography

a. Cleaning (first by acetone, then washed by methanol, finished by DI water rinse),

b. The wafer was dried by a nitrogen gun,

c. Positive PR coating by spin coater at 5000rpm for 30sec,



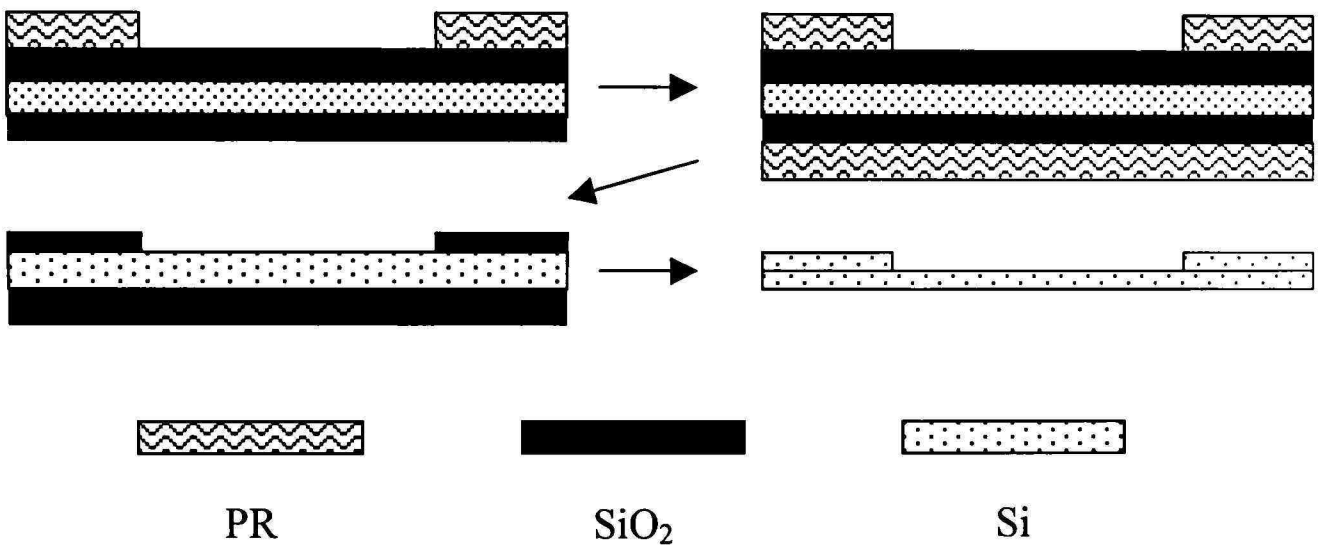
d. Pre-baked at 110°C for 1min,

e. Exposed for 20 seconds by hard contact mode,

f. Developed in developer for about 40 seconds, the developer was a mixture of 1:1 Shipley® S1813 developer concentration and DI water,

g. Post-baked at 110°C for 1min,

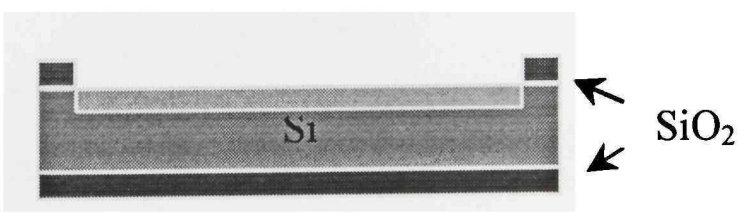
h. Photoresist coating of back side of the wafer to prevent the removal of backside SiO_2,



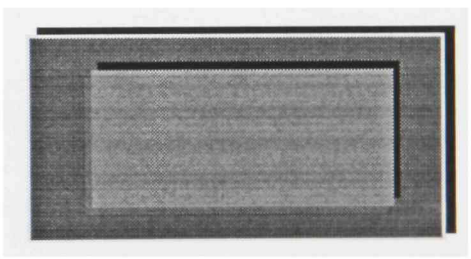
i. SiO_2 etching by buffered HF for about 10min,

j. Get rid of photoresist and clean using acetone, methanol and DI water,

4. Wet etch 10um~15um by 50 weight % KOH solvent. The etch parameter was 2 hours at 50°C, the etch rate was about 7.5μm/h. After etching, the wafer is cleaned using acetone, methanol and DI water,

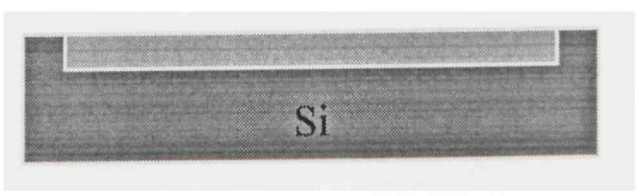


Side view

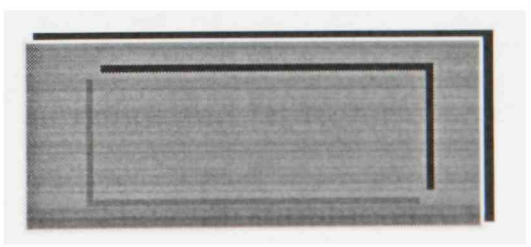


Top view

5. Remove SiO_2 on wafer surface by buffered HF,

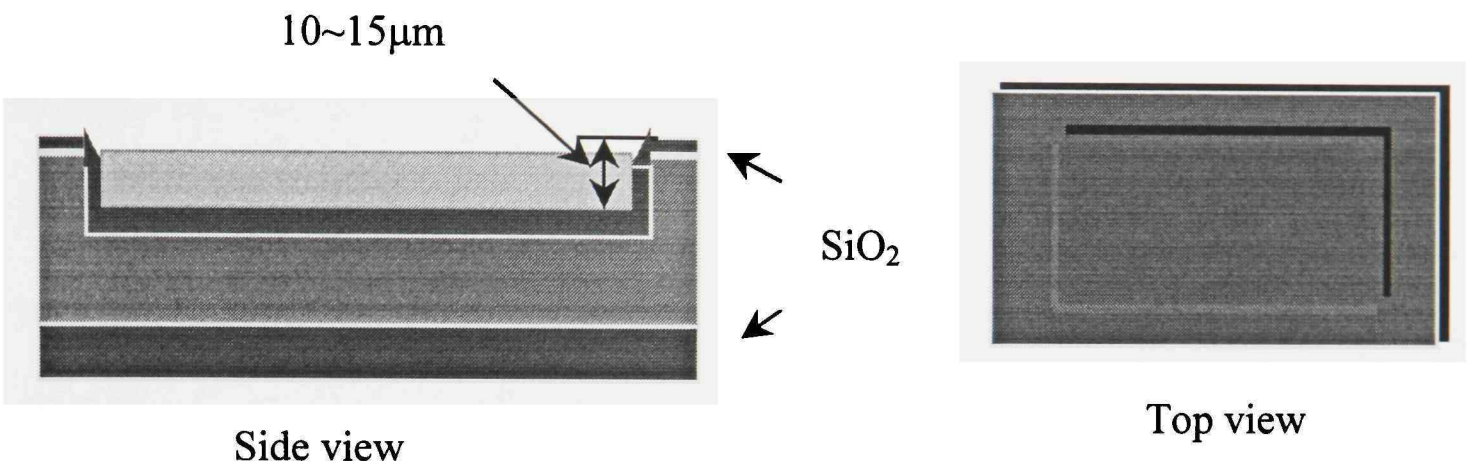


Side view



Top view

6. Double-sided oxide by wet oxidation. The temperature was about at 1140°C and the thickness was about 1μm,



7. Second lithography

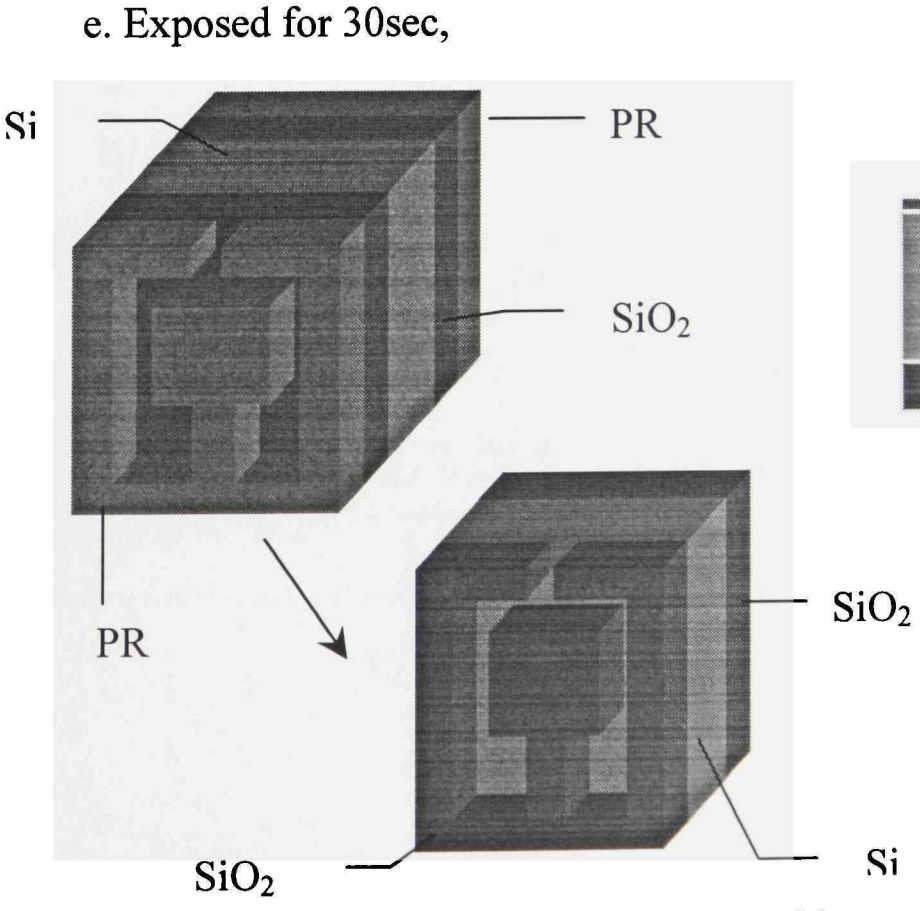
a. Cleaned using Acetone, Methanol and DI water,

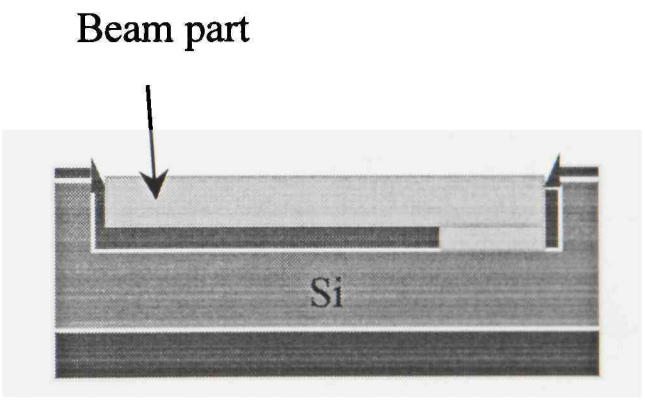
b. The wafer was dried using nitrogen,

c. Positive PR coated using spin coater. The thickness was inversely proportional to spin speed,

d. Pre-baked at 110°C for 1min,

e. Exposed for 30sec,





f. Developed for 40 seconds. The developer was a mixture of 1:1 developer concentrate and DI water,

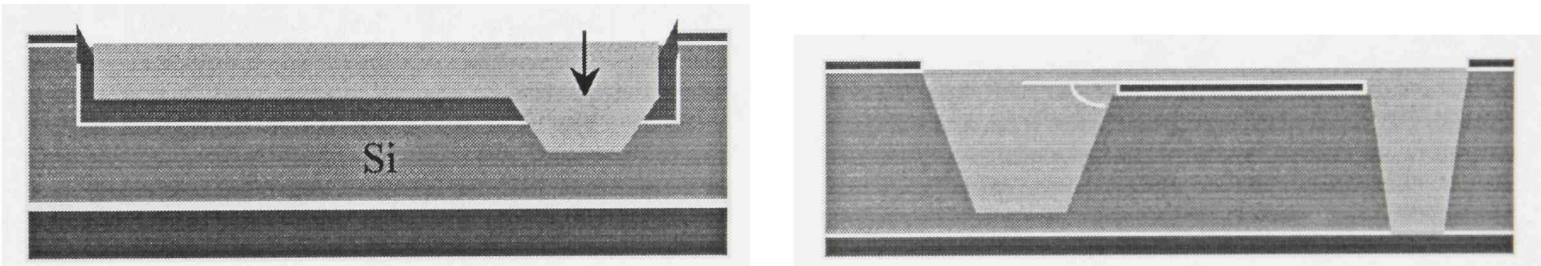
g. Post-baked at 110°C, for 1minute,

h. Back side PR coated to prevent the removal of backside SiO_2,

i. SiO_2 etched by Buffered HF for 10 minutes,

j. Get rid of PR and clean by acetone, methanol, and DI water.

8. Wet etch 30μm to form the shape of the beam. Etching was done in aqueous 50 weight % KOH solvent at 60°C for 1hour 15min. The etch rate was about 24.4μm/h. Then the wafer was cleaned by acetone, methanol, and DI water.



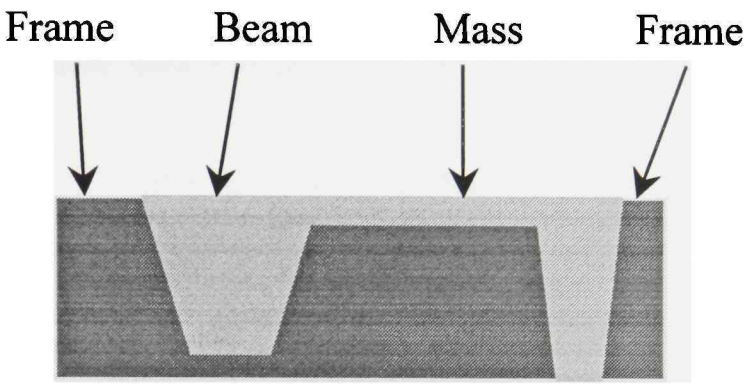
Side view

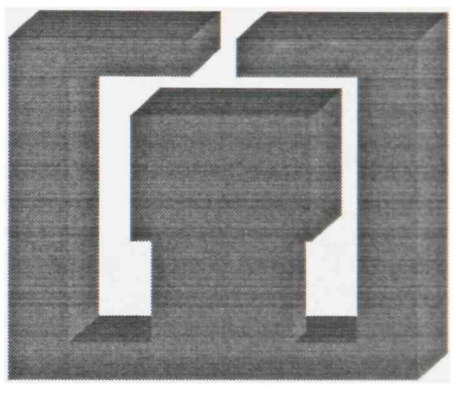
9. Third Photolithography

Same method as second photolithography was used here.

10. Wet etch about 260 μm until the silicon wafer end mass was released. Etchant was 50 weight %KOH. Etching was done at 60°C for 11 hours. The etch rate was 24.4μm/h. The wafer was cleaned by acetone, methanol, and DI water.

11. Get rid of the rest SiO_2 by Buffered HF etching. The beam was p doped to allow the capacitor structure to be formed,





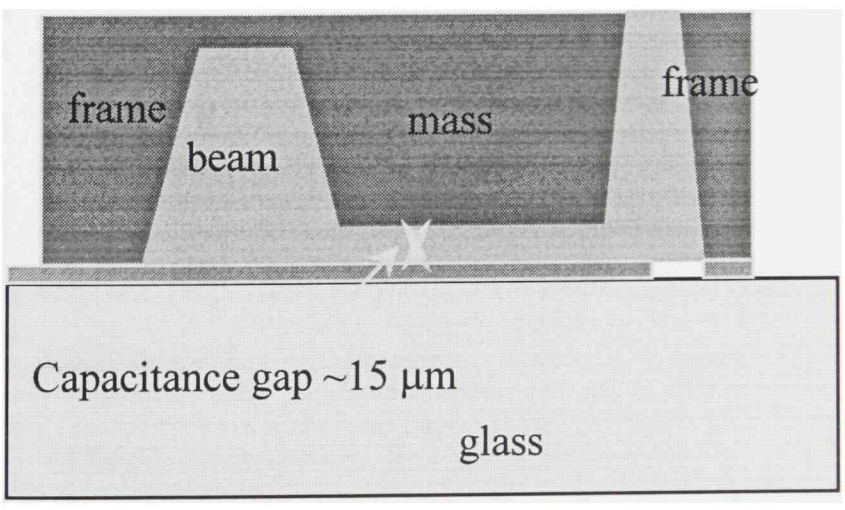
12. Wafer is hand diced into individual device for further fabrication,

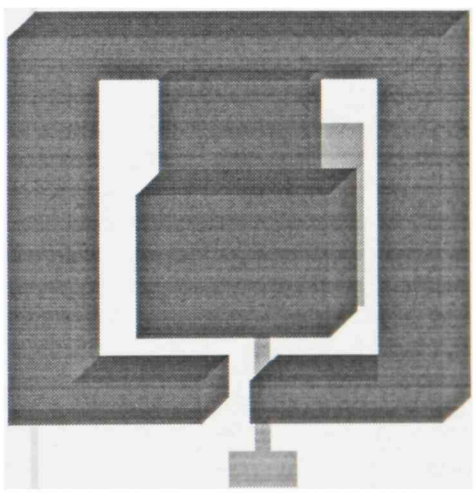
13. Evaporated aluminum film on glass surface using e-beam evaporator,

14. Etched aluminum to form metal pad,

15. Glass was also diced into individual parts using the diamond saw.

16. Glass-Si anodic bonding





The accelerometer was fabricated and was ready for test. However, a usable accelerometer would need to be packaged. This means the outlet wire could be bonded to the contact pad and the whole device would be packaged for protection.

The fabricated accelerometers (before dicing and bonding) are shown in Figure 4.8.

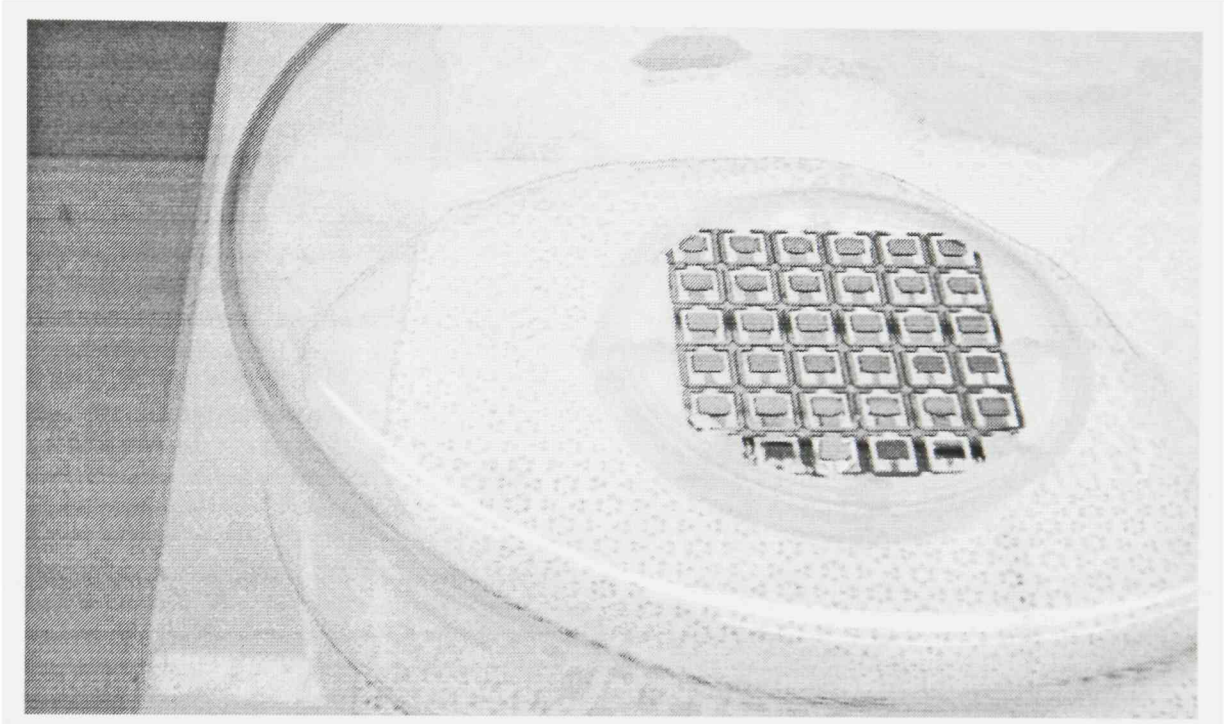


Figure 4.8. Accelerometers before dicing

4.4 Testing

To test the device and see how the capacitance changed with an applied acceleration, we attached a device to a pendulum and then set it to swing. Also an applied voltage caused an electrostatic force to simulate acceleration. We then measured the corresponding capacitance change of the sensor.

By plotting the capacitance versus voltage (e.g., use Lab View) curve, we saw how the accelerometer responded to a simulated acceleration.

By using the MathCAD program, we plotted the shape of the expected C-V curve, as shown in Figure 4.9.

$d := 20 \cdot 10^{-6}$ $L1 := 2000 \cdot 10^{-6}$ $\varepsilon := 1$ $S := 3000 \cdot 3600 \cdot 10^{-12}$

$b := 1700 \cdot 10^{-6}$ $L2 := 3500 \cdot 10^{-6}$ $\varepsilon 0 := 8.85 \cdot 10^{-12}$ $E := 1.7 \cdot 10^{11}$

$h := 30 \cdot 10^{-6}$ $V := -35..35$

$$S(V) := \varepsilon^2 \cdot (\varepsilon 0)^2 \cdot V^2 \cdot \frac{\left(L1^3 + 3 \cdot L1 \cdot L2^2\right) \cdot S^2}{2 \cdot E \cdot d^4 \cdot b \cdot h^3}$$

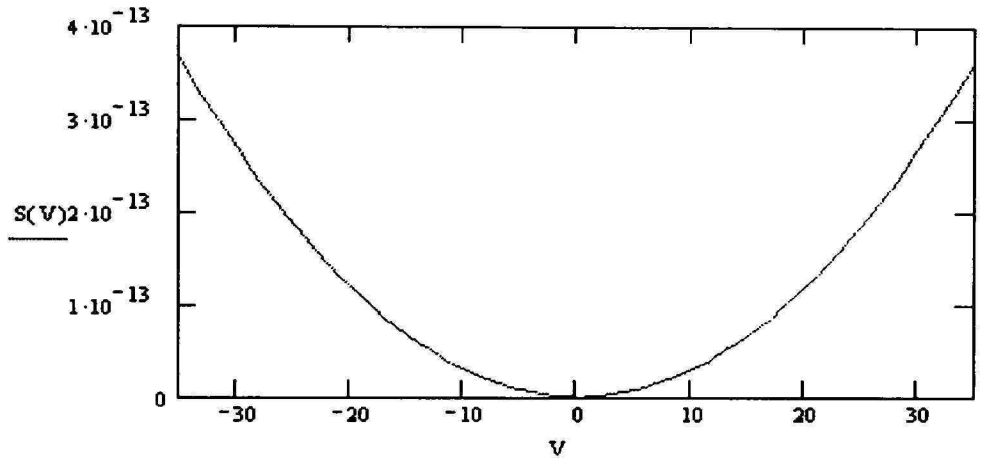


Figure 4.9. Expected C-V curve of the accelerometer

The actual measured curve is shown in Figure 4.10.

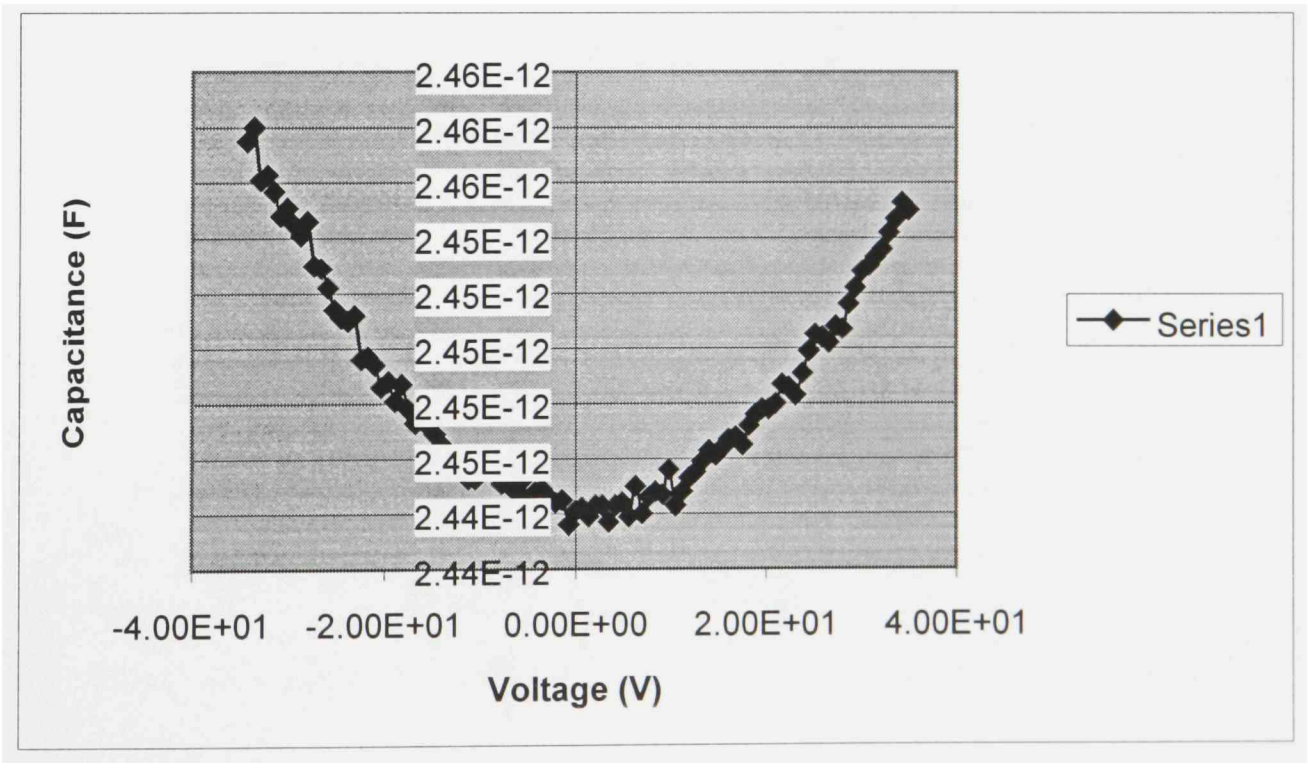


Figure 4.10. Actual C-V curve of the accelerometer

The fabricated sensor had the expected shape according to our design. It indicates our design and process flow was reasonable and successful. The measured C-V curve followed our expected curve very well. The deviation in the capacitance magnitude is due to the deviation of the capacitance gap distance during fabrication. This indicated the working principle of the sensor is correct. During the fabrication flow, all kinds of MEMS technologies were adapted. The success of this project provides useful experience for fabricating more complex devices in the future.

CHAPTER V

INVESTIGATION OF RESULTS AND DISCUSSION

5.1 Results and Discussion of Wet Etching

5.1.1 Etch rate

The etch rate of silicon in an aqueous KOH solution varies considerably with etchant temperature and concentration. The relevant experimental data are shown in Table 5.1. It is obvious that etch rate increase with an increase in temperature. Figures 5.1 and 5.2 show that in 20 wt% KOH silicon had the highest etch rate.

Table 5.1. Etch rate of silicon in aqueous KOH solutions (μm/h)

	Temperature (°C)								
%KOH	20°	30°	40°	50°	60°	70°	80°	90°	100°
10	1.49	3.2	6.7	13.3	25.2	46	82	140	233
15	1.56	3.4	7.0	14.0	26.5	49	86	147	245
20	1.57	3.4	7.1	14.0	26.7	49	86	148	246
25	1.53	3.3	6.9	13.6	25.9	47	84	144	239
30	1.44	3.1	6.5	12.8	24.4	45	79	135	225
35	1.32	2.9	5.9	11.8	22.3	41	72	124	206
40	1.17	2.5	5.3	10.5	19.9	36	64	110	184
45	1.01	2.2	4.6	9.0	17.1	31	55	95	158
50	0.84	1.8	3.8	7.5	14.2	26	46	79	131
55	0.66	1.4	3.0	5.9	11.2	21	36	62	104
60	0.50	1.1	2.2	4.4	8.4	15	27	47	78

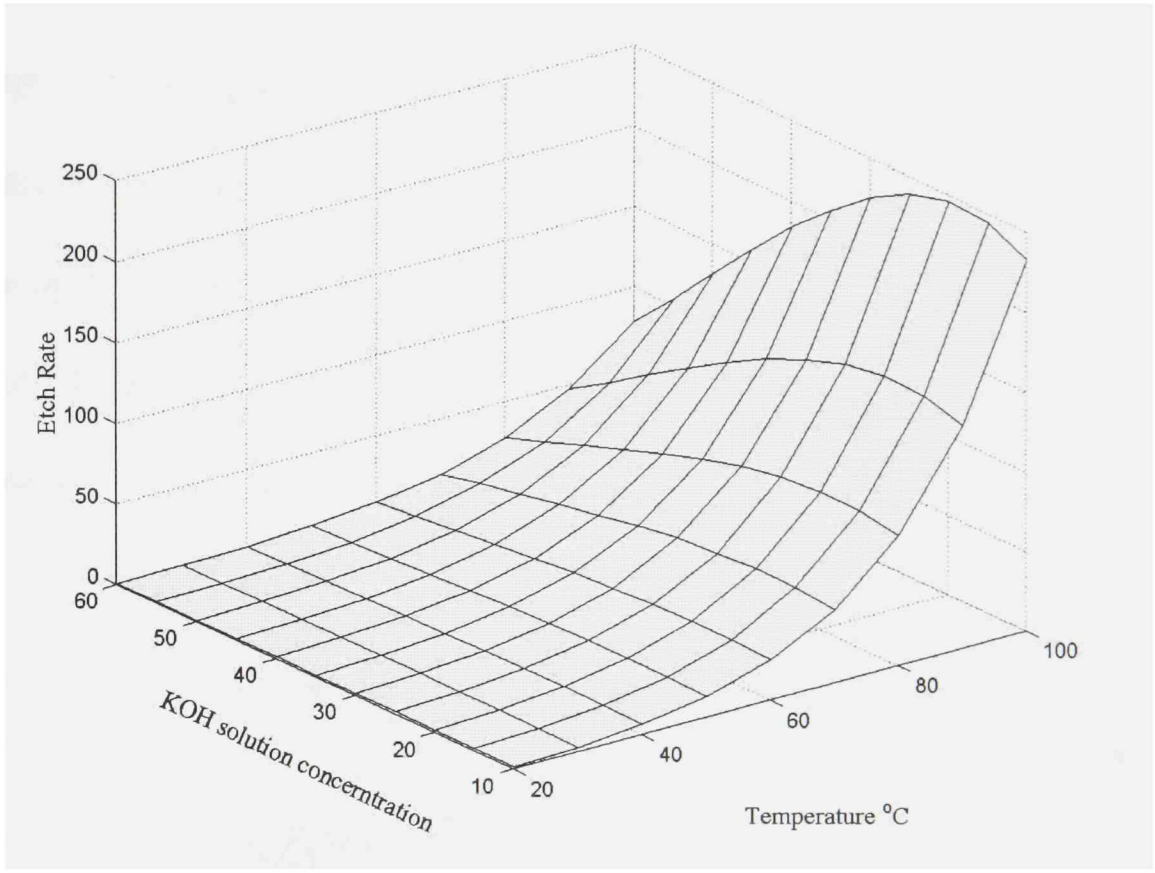


Figure 5.1. 3D plot of etch rate of silicon in KOH

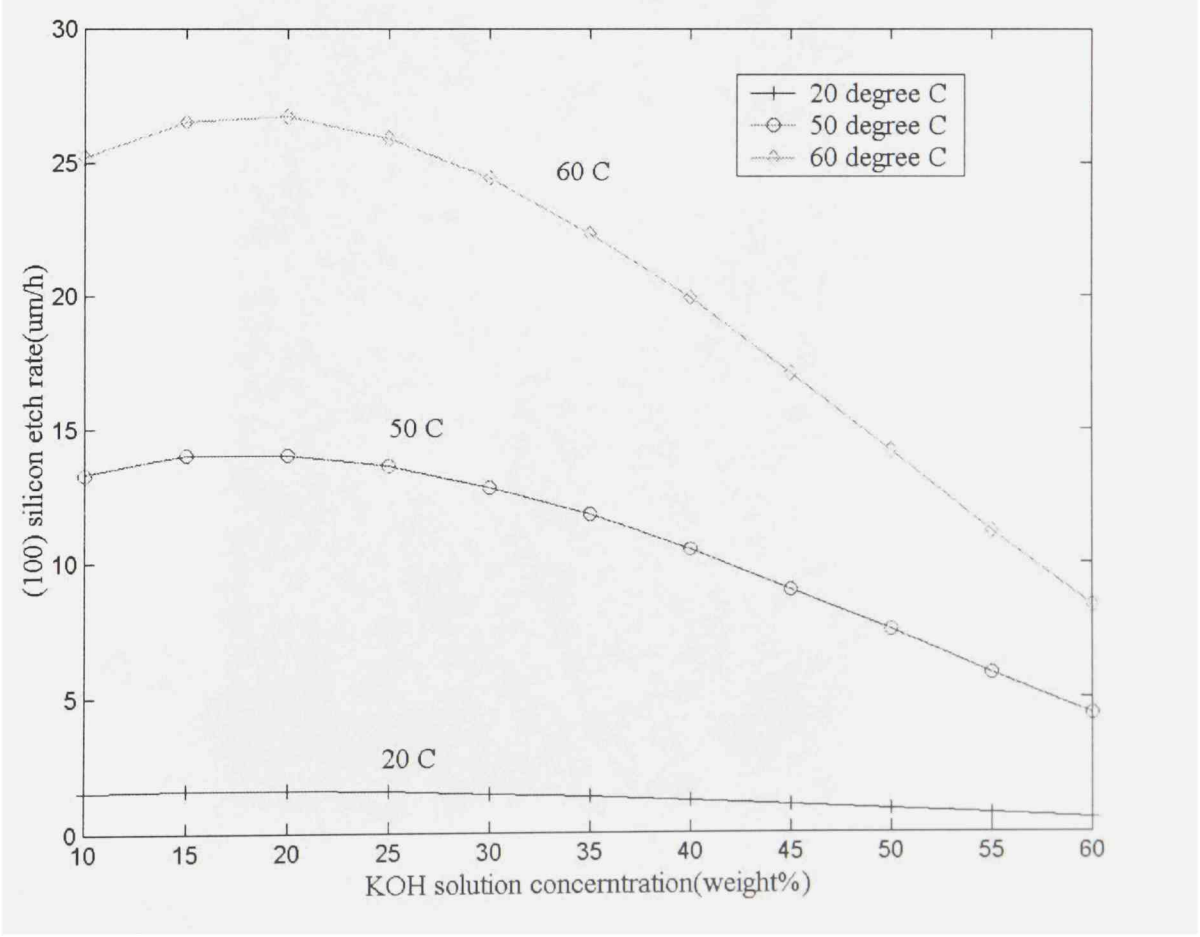


Figure 5.2. Etch rate for various temperatures and concentrations

However, in most cases, a flat sidewall and bottom were also required for an etched structure. The experiment shows that the surface roughness was dependant on the etchant concentration. Normally, when etching at low and medium KOH concentrations, the <100> surface roughed. Figure 5.3 shows the various bottom roughness of the silicon groove etched by different concentration of KOH solvent. The roughness of the etched bottom generally increases with the etch depth [23] [24]. Figures 5.4 and 5.5 show the topology of a <100> wafer after 50 wt% KOH etching. The result shows a pretty acceptable smoothness for micro-fluid channels.

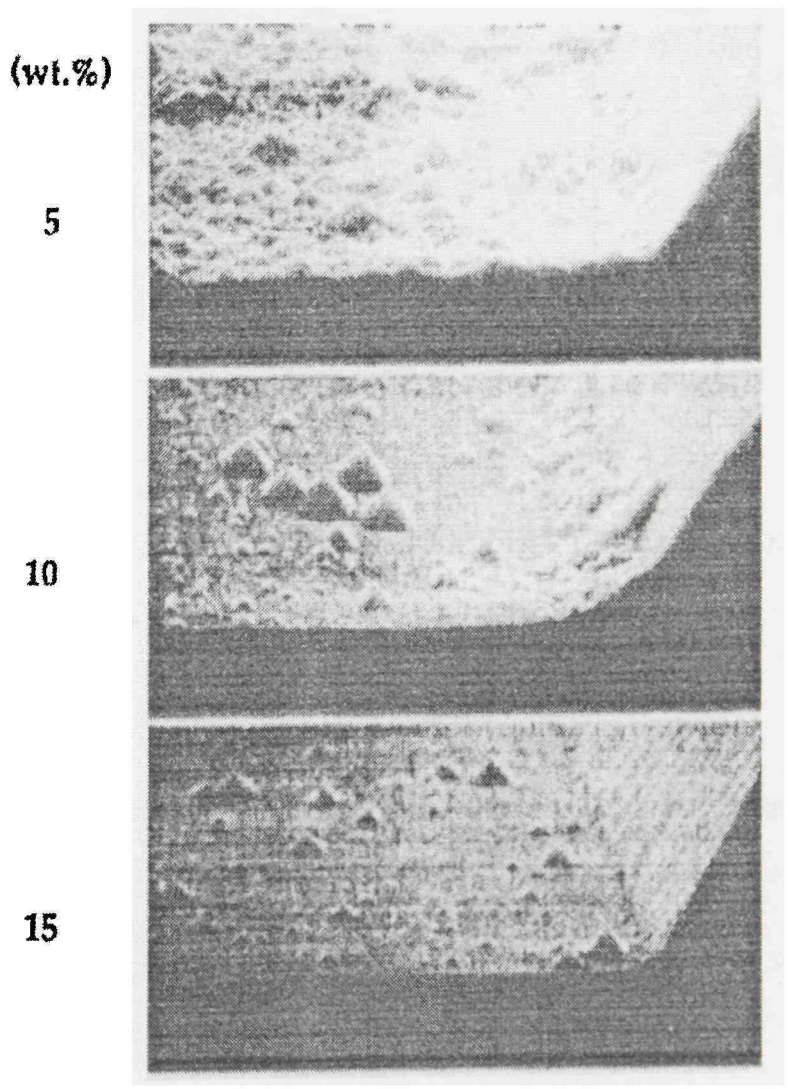
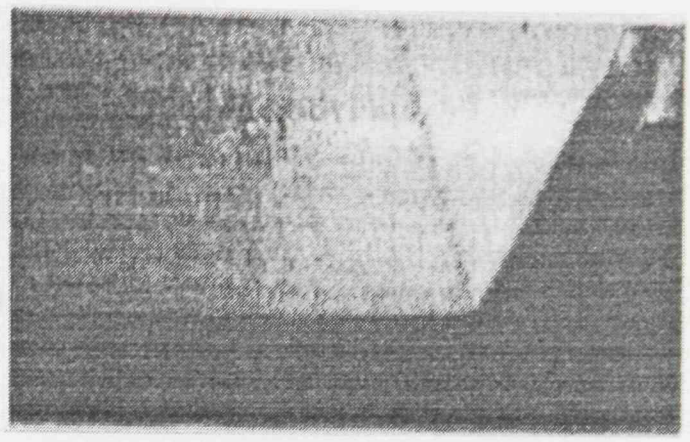


Figure 5.3 The bottom topology of etched groove of <100> Si wafer on condition of different concentration KOH etch

22



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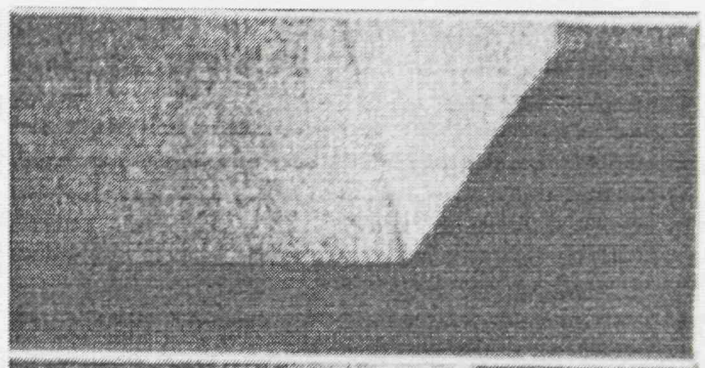

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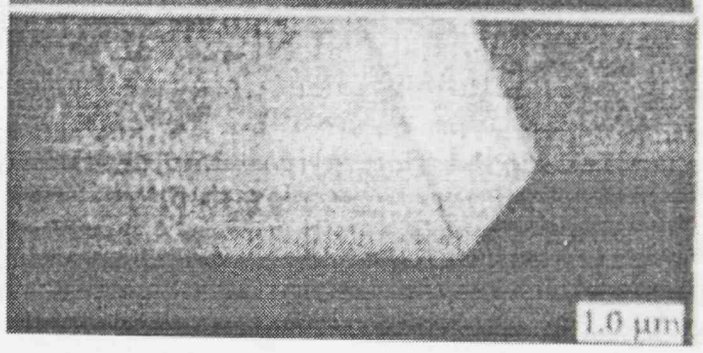


Figure 5.3 Continued.

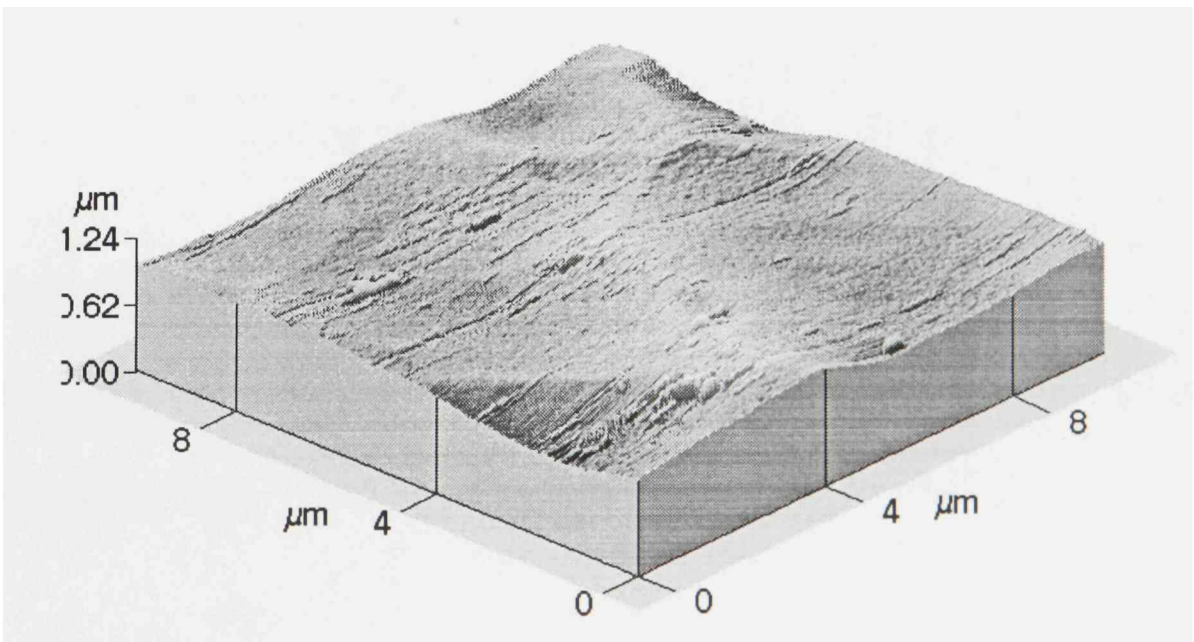
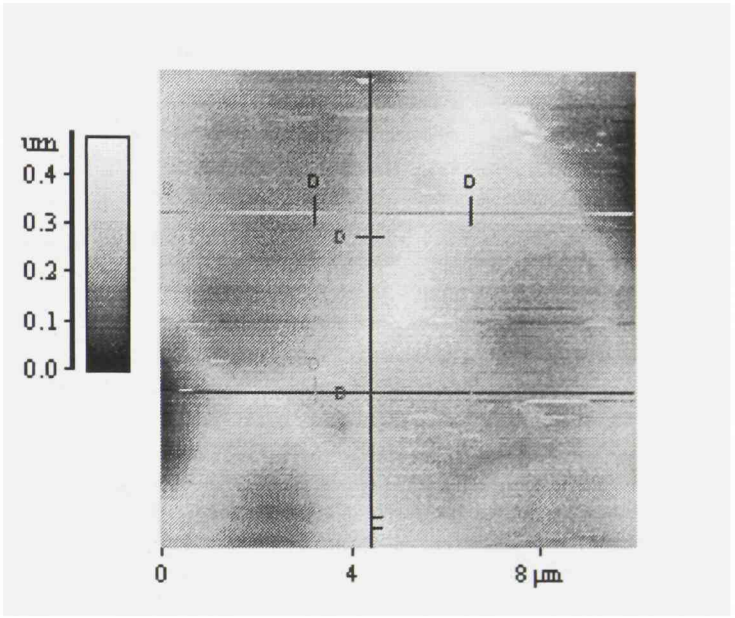


Figure 5.4. AFM image of bottom topology of 100μm etched groove of <100> Si wafer on condition of 50 wt.% KOH etch



Line	Height	Distance	Rp-v	Rms	Ave
[A]	0: 342 Å	0: 3.29 um	0.241 um	495 Å	375 Å
[B]	0: 0.147 um	0: 3.29 um	0.301 um	747 Å	636 Å
[C]	0: 275 Å	0: 3.29 um	0.214 um	472 Å	375 Å

Figure 5.5. Topology analysis of 100µm etched groove in <100> Si wafer (condition on 50 wt.% KOH etch)

5.1.2 Timed etch stop

The timed etch stop was the easiest way to stop etching. The biggest advantage was the simplicity of this operation. However, several problems arose.

1. The etch rate is influenced considerably by transport of etching agents to the wafer and by transport of etch products away from the wafer. The shape of etch container, stirring, and number of wafers etching at the same time also influenced the etch rate. The change was around ten percent from the data in Table 5.2. Therefore, the etch depth could not be determined by etch time with sufficient precision. Normally, during the last stage of etch time, it was necessary to observe the etching carefully.

Table 5.2. Deviation of etch rate of KOH etching <100> Silicon

Etch Condition	Etch rate (μm/h)	reference rate (μm/h)	Deviation (%)
33% KOH 85°C	94.2	102	7.8%
40% KOH 70°C	31.8	36	11%
50% KOH 55°C	9.4	10.8	13%

2. The thickness of wafers varied from wafer to wafer. And the thickness of a single wafer was not homogeneous. The thickness of the oxide mask was not uniform as well. Normally, the quality of surface during an etch was not very good, especially when several wafers were etched at the same time.

5.1.3 Etch Mask

The most commonly used masks for silicon etching are silicon dioxide and silicon nitride. Etch mask material should be selected by considering the availability of the process, ease of the process, and other factors. Because silicon dioxide can be grown easily by the equipment in our laboratory, and since it can be easily removed by HF, silicon dioxide was used exclusively in my experiments as a mask material.

Silicon dioxide can be thermally grown and deposited in a CVD process. The etch rate of thermally grown SiO_2 by KOH solvent is listed in Table 5.3, the etch rate ratio of KOH on silicon and silicon dioxide is shown in Figures 5.6, 5.7 and 5.8. The etch rate reached its maximum at around 35 weight percentage KOH. It was also found that the etch rate of CVD grown silicon dioxide on KOH was much faster than thermally grown SiO_2 [24]. So, thermally grown silicon dioxide was chosen as a mask.

Table 5.3. Etch rate of SiO_2 in aqueous KOH solutions (nm/h)

	Temperature (°C)								
%KOH	20°	30°	40°	50°	60°	70°	80°	90°	100°
10	0.40	1.22	3.5	9.2	23	54	123	266	551
15	0.63	1.91	5.4	14.4	36	85	193	416	862
20	0.88	2.66	7.5	20.0	50	118	268	578	1200
25	1.14	3.46	9.8	26.0	65	154	348	752	1560
30	1.42	4.32	12.2	32.5	81	193	435	940	1950
35	1.44	4.37	12.4	32.8	82	195	440	949	1970
40	1.33	4.03	11.4	30.3	76	180	406	876	1820
45	1.21	3.67	10.4	27.5	69	163	369	797	1650
50	1.08	3.28	9.3	24.6	62	146	330	713	1480
55	0.95	2.87	8.1	21.6	54	128	289	624	1290
60	0.81	2.45	6.9	18.4	46	109	246	532	1100

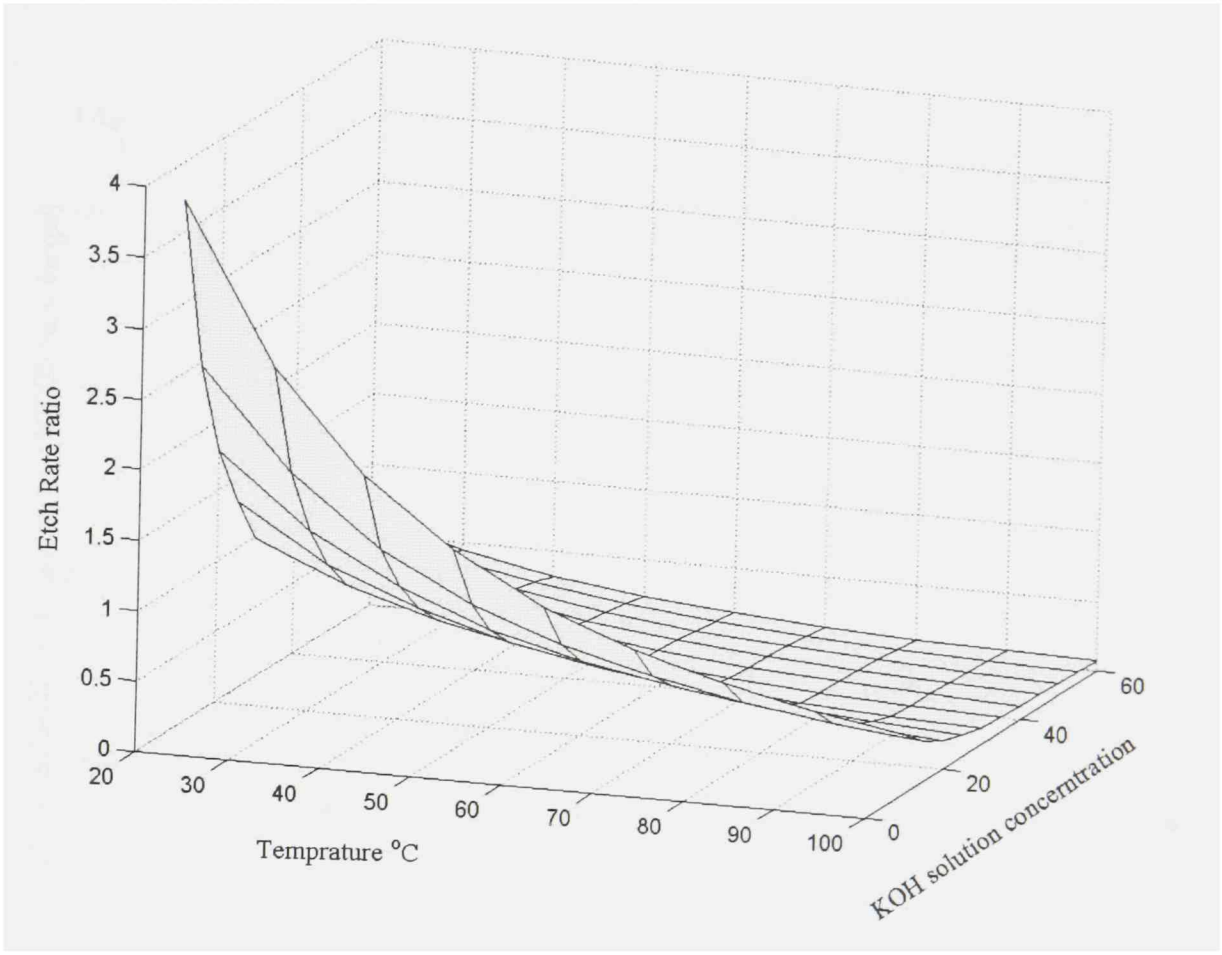


Figure 5.6. 3D plot of etch rate ratio of Si/SiO_2 in KOH

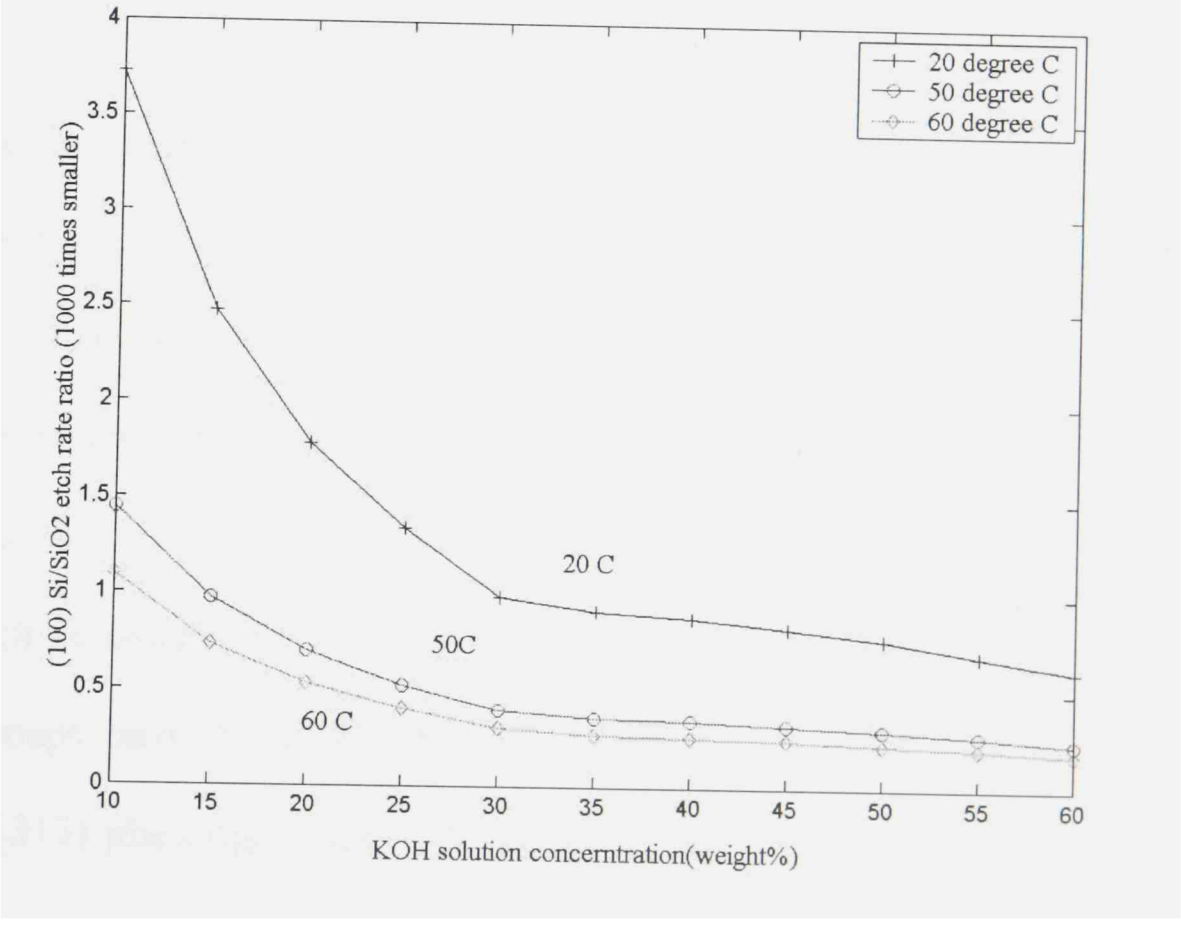


Figure 5.7. Etch ratio of Si/SiO_2 for various concentrations.

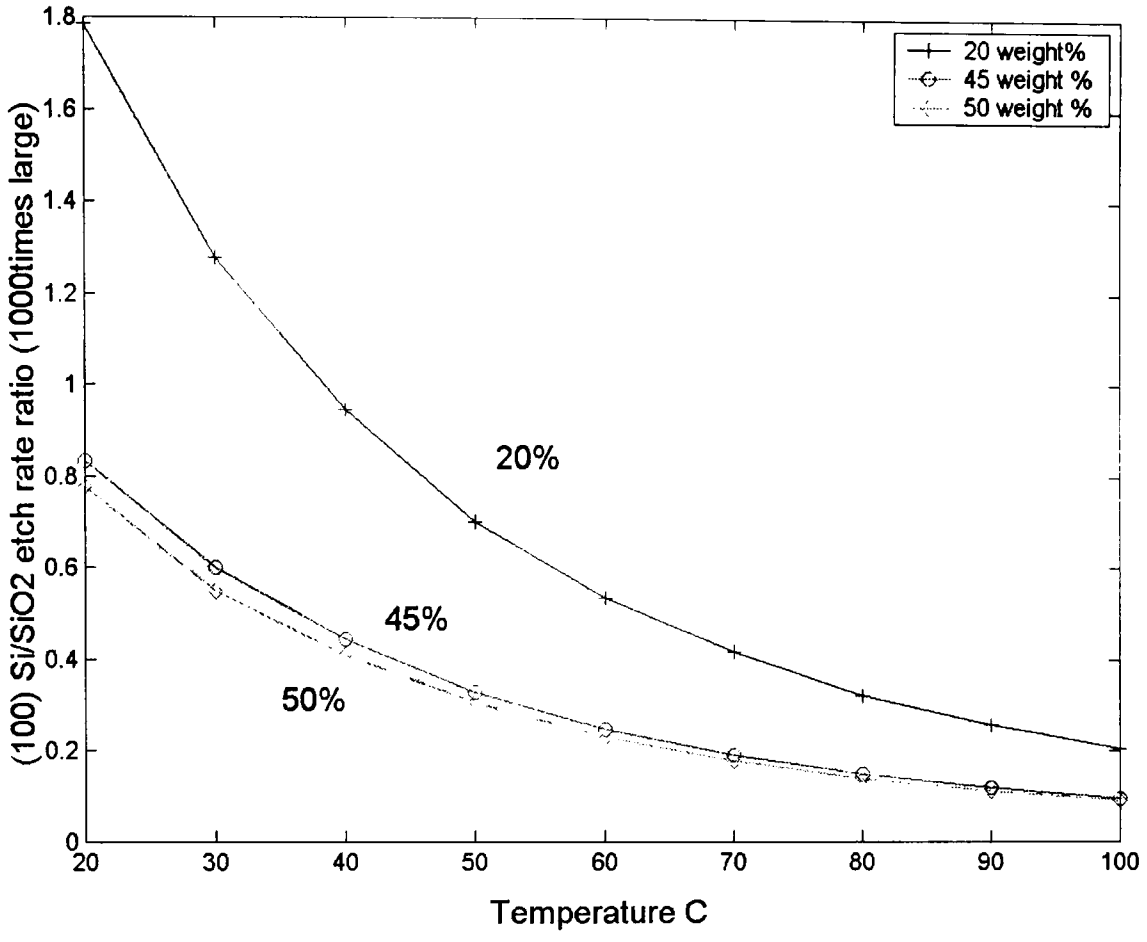


Figure 5.8. Etch ratio of Si/SiO_2 for various temperatures

5.1.4 Corner compensation

When convex corners are unavoidable, the forms of corners are dominated by the fast etching planes rather than slower etching planes like the <111> [25, 26]. The direct result is the undercutting of the corners. Compensation structure needs to be added to the mask design.

Much research has gone into determining the fast etch planes, and different research groups have found different fast-etching planes. For aqueous KOH etches, {212} and {313} planes are widely discussed [25, 26].

Two techniques are widely used for compensation. The most popular is to add compensation structure on mask. The other technique is misalignment of the mask with respect to the <110> plane by a slight angle [14].

When fast-etching planes such as {212} intersect the (001) surface at {210} orientations, Figures 5.9, 5.10 and 5.11 show the compensation principle and different compensation patterns. Figures 5.12 and 5.13 show examples of corner compensation.

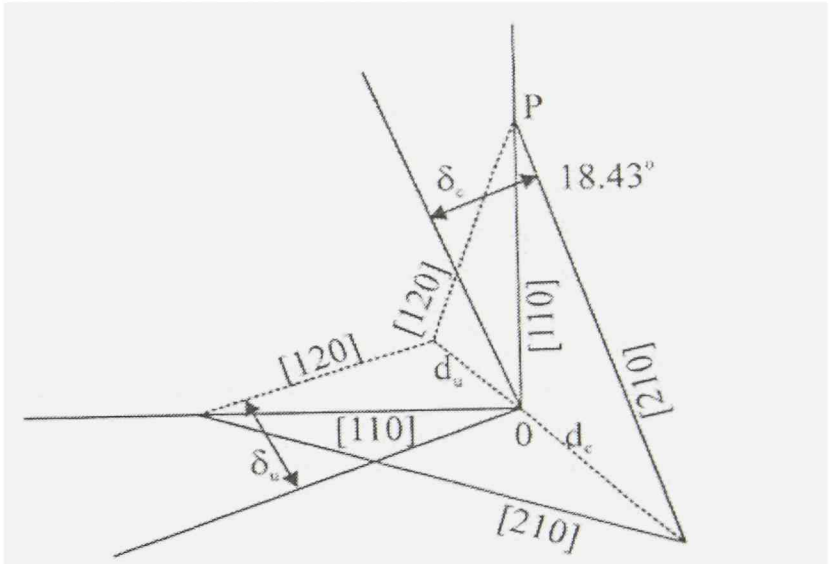


Figure 5.9. Triangle of mask compensation
(from Wu and Ko [25])

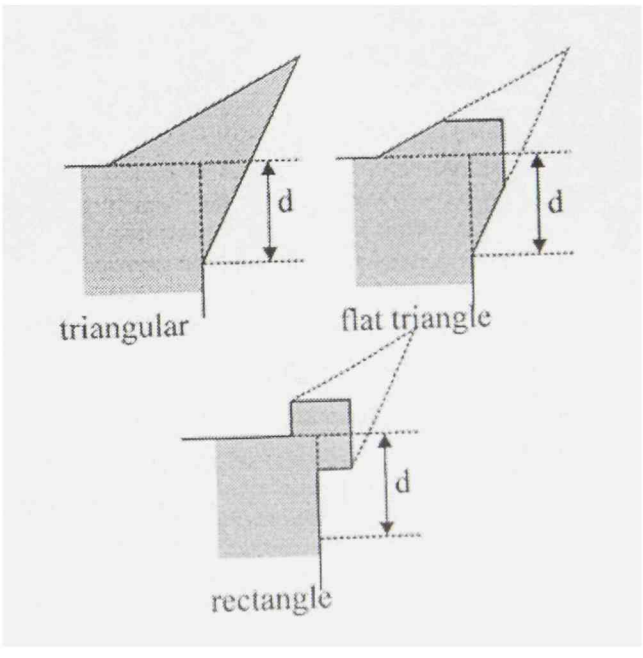


Figure 5.10. Compensation pattern (from Puers and Sansen [26])

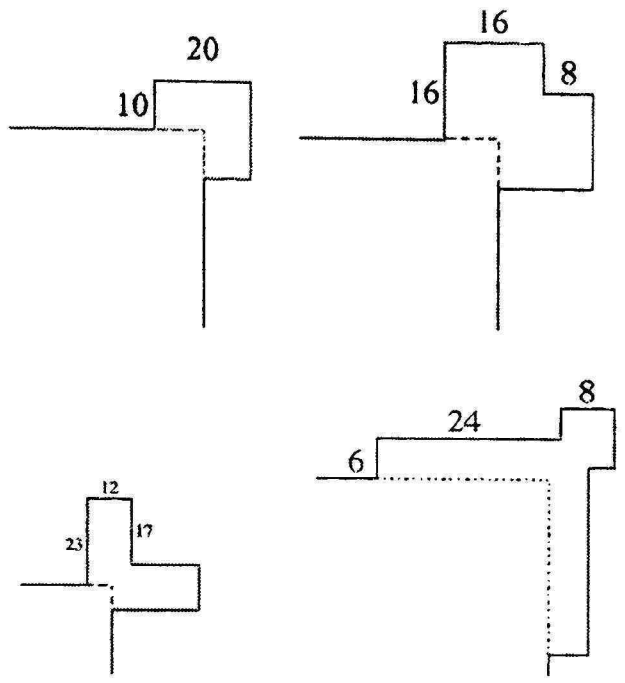
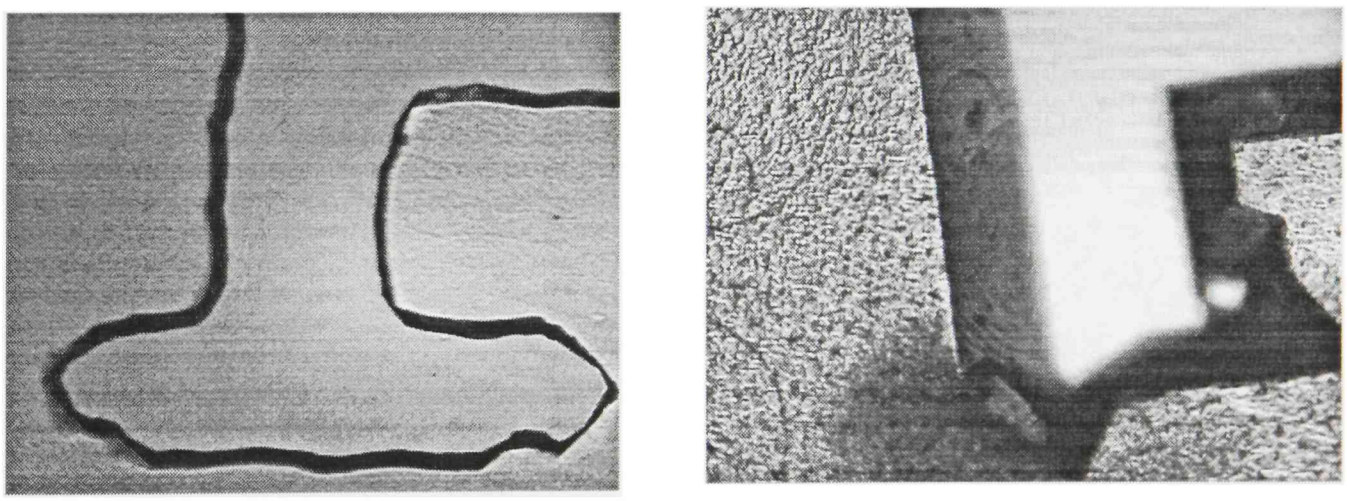


Figure 5.11. Compensation patterns attaining the same results
(from Q.A. Huang [14])



Before etching

After etching

Figure 5.12. Convex corner etch with compensation structure

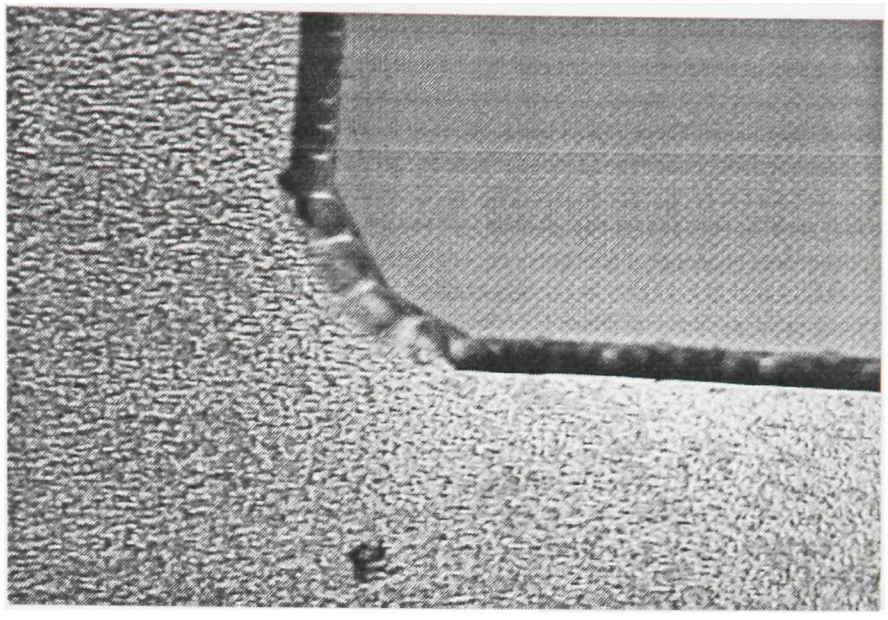


Figure 5.13. Convex corner etch without compensation structure

5.2 Results and Discussion of Bonding

5.2.1 Factors influencing direct bonding

Direct bonding depends on short ranged force such as Van der Waals forces, so the key factor for successful bonding is to keep the surfaces of two wafers as close as possible. This is influenced by the size of the particle residue on the wafer surface during bonding, the flatness of the wafers, and the roughness of the bonding surface.

5.2.1.1 Influence of the particle size. During direct bonding, wafers are deformed around particles on bonding surfaces, leaving circularly unbonded interface bubbles. Figure 5. 14 shows the formation of bubbles because of particles.

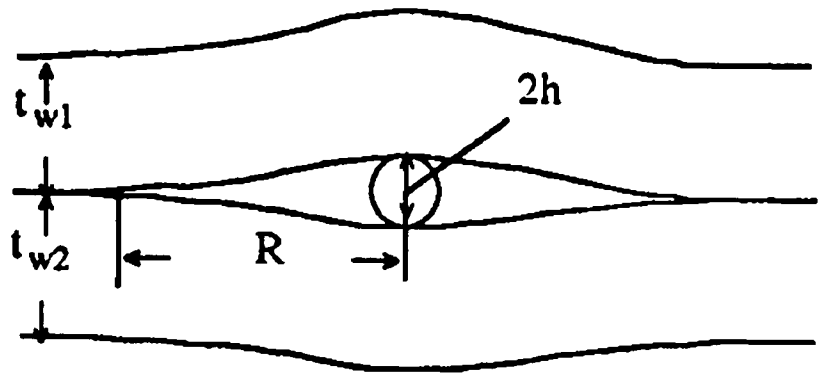


Figure 5. 14. Formation of bubbles because of particles

A formula by Q. Y Tong [21] shows that the radius of the unbonded bubbles can be calculated as:

$$R = \left[0.73Et_w^3/\gamma\right]^{1/4} h^{1/2} \tag{5.1}$$

In it, E is Young's modulus, γ is the surface energy of each wafer in the pair, t_w is the thickness of the wafer. For a 2-inch wafer with a thickness of 280 μm, a particle of about 1μm can leads to a bubble with a diameter of about 0.3 cm. This formula also shows that reduction of the wafer thickness leads to a strong reduction in unbonded area.

Q.Y. Tong also showed that if the particle size was smaller than a critical size h_c, which can be calculated by formula 5.2, then the unbonded bubble will have a much smaller radius, which can be calculated by formula 5.3:

$$h_c = 4.785(t_w\gamma/E)^{1/2} \tag{5.2}$$

$$R \approx h \tag{5.3}$$

For a typical 2-inch wafer with thickness of 280 μm, h_c is in the order of 730 Å. and the result bubble radius is also about 730 Å.

Therefore, to initiate successful direct wafer bonding, cleaning is critical to make the wafer surface free of particles. The yield will be improved greatly by successful cleaning.

5.2.1.2 Influence of the flatnesss. Though wafers are carefully polished, they are not completely flat. However, during wafer bonding, each wafer will be elastically deformed to achieve bonding. Q.Y. Tong [21] reports that a flatness variation of 1-3 μm over a 4-inch silicon wafer does not prevent wafer bonding. Bow up to 25 μm is also tolerable. Normally, the wafers used for bonding have better flatness parameters than this, so the flatness is not a big obstacle for direct boning in most cases.

Mircoroughness is also crucial in wafer bonding. It is normally characterized by a root mean square value abbreviated as R_q. Q.Y. Tong reports that a R_q value less than 5 Å is adequate for wafer bonding. During our bonding experiment, an AFM scanned image shows a R_q value about 15 Å (shown in Figures 5.15 and 5.16), and the bonding result is still good.

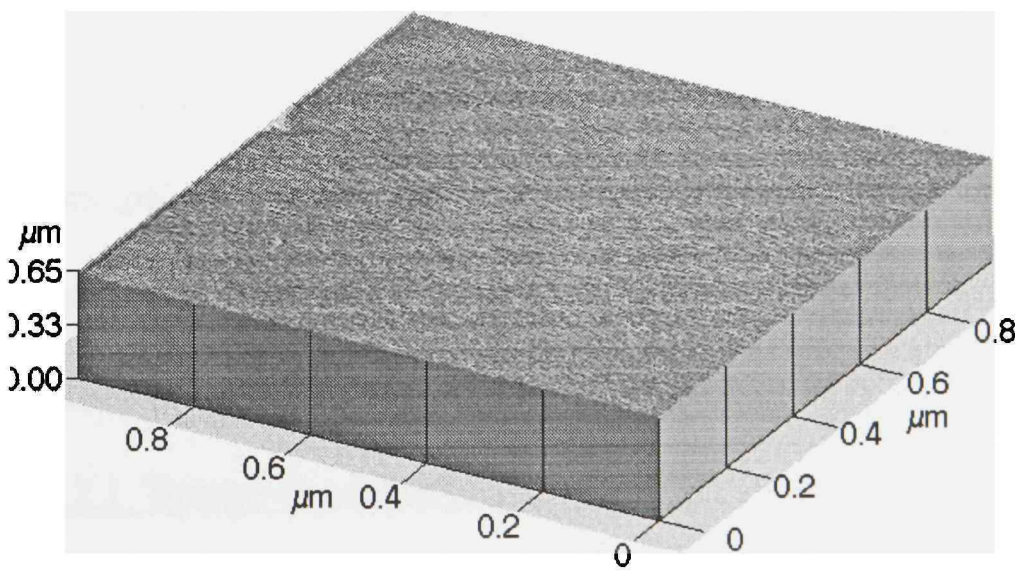
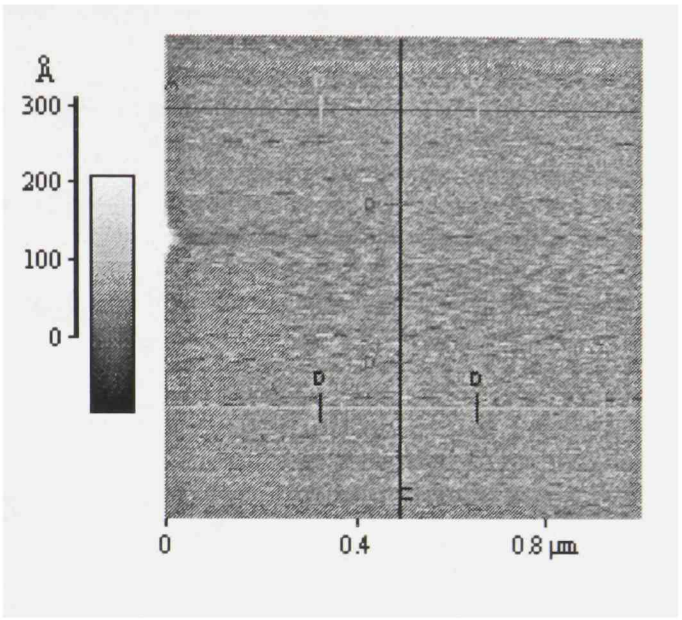


Figure 5.15. Surface Topology of bare Si wafer



Line	Height	Distance	Rp-v	Rms	Ave
[A]	0: 3.21 Å	0: 0.329 um	227 Å	15.0 Å	6.24 Å
[B]	0: 12.8 Å	0: 0.329 um	266 Å	17.7 Å	8.77 Å
[C]	0: 1.07 Å	0: 0.329 um	98.4 Å	11.6 Å	8.26 Å

Figure 5.16. Analysis of surface topology of silicon wafer

5.2.2 Factors influencing anodic bonding

Because anodic bonding is done at elevated temperatures and high voltages, these two parameters can influence the bonding results a lot.

5.2.2.1 Temperature influence. The high temperature plays two roles in anodic bonding. First, it can mobilize alkali ions inside the glass wafers, which makes it easier to

move them by an applied electrical field. Second, different expansion coefficients for silicon and most glass wafers make bonding difficult.

Many papers have been published on the critical temperature needed to mobilize ions. Normally the range is from 200°C to 500°C. Because the required temperature is inversely proportional to the applied voltage, higher temperature is tended to use for anodic bonding.

However, the second factor has been proven to be more important in anodic bonding. Because the anodic bonding is carried out between two different materials, the different thermal expansion coefficients of these materials will cause great stress in the bonded interface. It may cause the bonded pair to bow, or even crack. Therefore, the thermal expansion coefficients of the bonded materials must match in the operating temperature range.

A well accepted glass for anodic bonding is Pyrex 7740 from Corning. Figure 5.17 shows the thermal expansion coefficient of silicon and Pyrex 7740 as a function of temperature. As can be seen, above 450°C the thermal properties of the materials begin to deviate widely. Therefore, the bonding temperature should be limited to below 450°C.

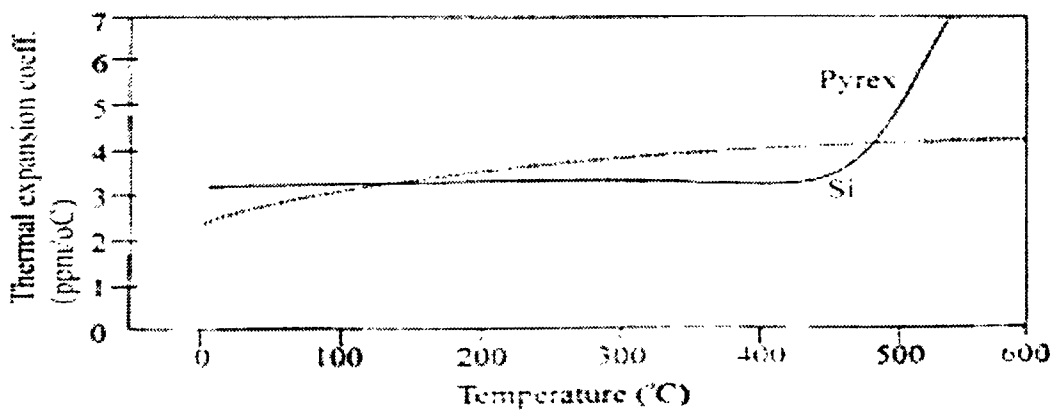


Fig 5.17. Thermal expansion coefficient of silicon and Pyrex 7740 glass from Q.A. Huang [14]

Besides Pyrex 7740, there are several other types of glass can be chosen as anodic bonding material such as Schott 3310, Soda lime #0080, and aluminosilicate #1720. Actually, as long as the thermal expansion coefficient of the chosen glass matches that of silicon. It can be used for anodic bonding. The glass used in projects mentioned in this paper is boronfloat glass from Schott. Its specification is listed in Table 5.4.

Table 5.4 Physical specification of Schott Boronfloat® glass

Coefficient of Thermal Expansion (α 20 - 300°C)	3.25 x 10^{-6}/K
Maximum Operating Temperature	500°C
Maximum Recommended Thermal Gradients< 1 hour	110K
Young's Modulus (E) @ 25°C	63 GPa
Density (ρ) @ 25°C	2.22 g/cc
Dielectric Constant (K) 1 Mhz @25°C	4.6

5.2.2.2 Voltage Influence. The high voltage makes mobile ions travel to the surface. The induced electrical field causes a strong mechanical force to push the two wafers together. To realize an even force across the surface and avoid air trapped inside, the electrical field should be spread evenly from the center to edge.

Two kinds of cathodes are usually used to apply voltage to the glass wafer surface, one is a point probe and the other is planar. The planar cathode can spread the electrical field fast and evenly, however, air is often trapped inside. The point probe applies voltage to one point and lets the electrical field spread across the wafer. It takes a much longer time to form a complete electrical field. The electrical field spreads much slower at the edge than in the center. It is also hard to find a proper probe point at a surface with arbitrary shape, especially those with a sharp point.

When the glass is conductive, the pressure induced by the electrical field is

$$P = \frac{2V^2\varepsilon_G^2}{\varepsilon_0 D_P^2}.$$

In the equation, V is the applied voltage, ε_G is the dielectric constants of the glass, and D_P is the thickness of the glass. From this formula, we can see clearly that the pressure drops quickly when the glass become thick. In that case, we normally need higher voltage to achieve good contact.

To combine the advantage of both kinds of cathodes, a layer of aluminum foil is placed on the glass wafer surface and cut into a shape that will facilitate the spread of electrical field. Figure 5.18 shows a few shapes used for that purpose, and Table 5.5 shows the bonding results with and without that aluminum foil layer.

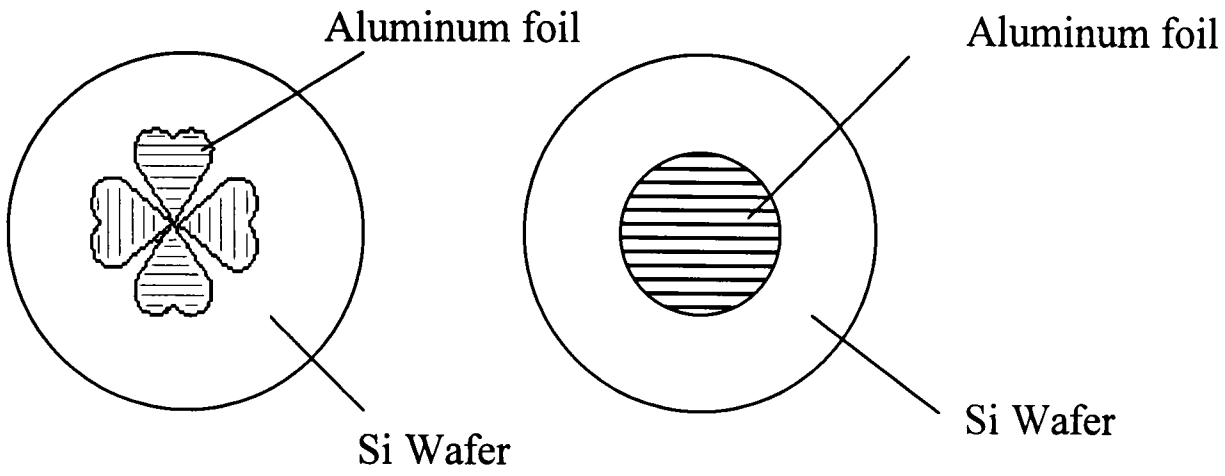


Figure 5.18. Aluminum foil used to facilitate bonding

Table 5.5 Bonding results comparison

Item	Bonding time (minutes)	Applied Voltage (V)	Void
Bonding with aluminum foil	6	800	free
Bonding without aluminum foil	10	1000	little

5.2.3 Discussion of anodic bonding system

From the above discussion, we know that anodic bonding system is done at elevated temperature and high voltage. So the bonding system is divided into two parts according to their function: heating and high voltage. Figure 5.19 shows the details of these two parts. Both parts have some alternative forms and will be discussed as following.

5.2.3.1 Heating part. the temperature range required in anodic bonding is 250-500 °C, which is within the operational range of most laboratory hot plate. Therefore, a hot plate is chosen as the heating element. There are several different types of hot plates:

analog or digital type, programmable or manual. Their principal functions are the same, with the difference between them being the ease and precision of control. However, anodic bonding processes do not require a very precise temperature, so a manual control direct heating type was chosen for the first trial. Because the heat produced by an electrical heater is proportional to the square value of the voltage applied on that element, the temperature control can be realized by adjusting the voltage, which is done by an external voltage transformer. The result is satisfactory. However, since this hot plate has no temperature gauge, the operator may need a few times of training and practice before he can control the temperature properly. A programmable and digital heater is more suitable for general operators and have the potential of automatic control.

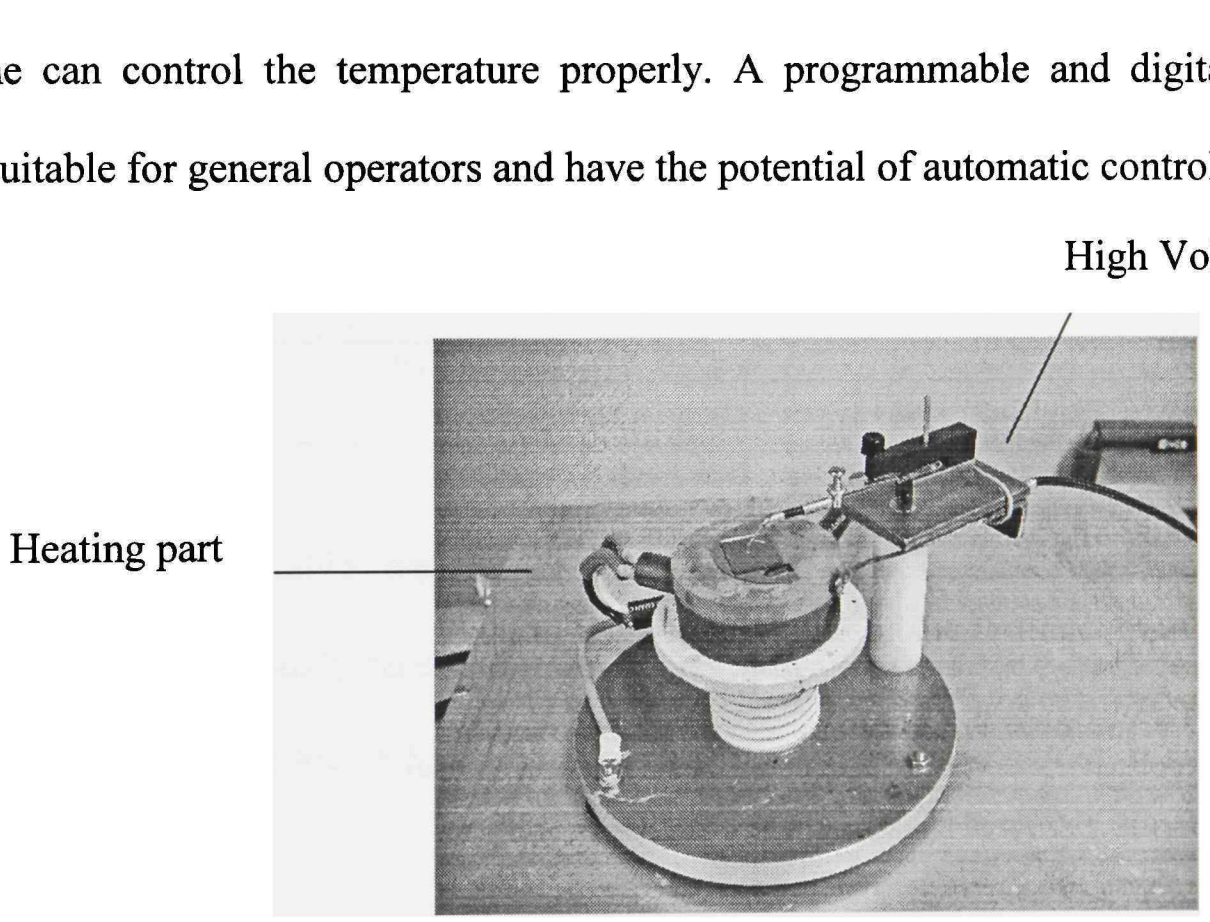


Figure 5.19. Anodic bonding platform

5.2.3.2 High voltage part. Anodic bonding needs a high voltage up to 1.5 kV DC. Almost all high voltage generators can generate higher voltages than that. However, to do anodic bonding, there are several specific requirements for the high voltage generator.

First, the voltage can be increased or decreased continuously in a short time; second, it should be equipped with a voltage meter and a current meter for better observation and control of the process parameters; third, an overload protection is needed for safety reason; finally, the polarity should be adjustable to suit different kinds of connectors.

Three types of generators are tested and their properties are combined in Table 5.6

Table 5.6. Properties of high voltage generators used for anodic bonding

Type	Voltage range (kV)	Continuous changeable	Meter	Polarity changeable
Tailor made	0~5	Yes	Voltage	No
Fluke-415B	0~3.1	No	Voltage	Yes
PS-15	0~15	Yes	Voltage / Current	Yes

From the above table, we can see that PS-15 is most suitable for anodic bonding. It can provide continuously control and good observation at the same time. Figure 5.20 shows the front panel of PS-15 high voltage generator.

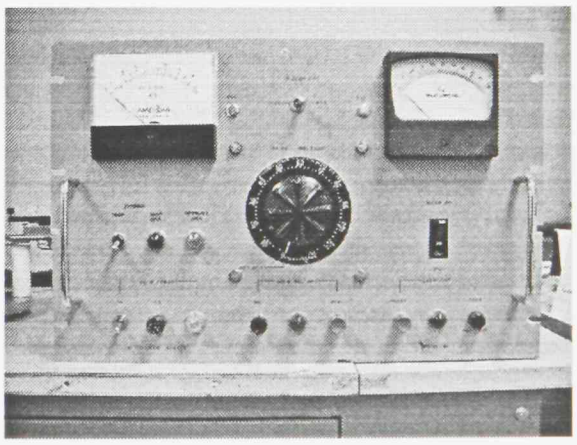


Figure 5.20. Front panel of PS-15 high Voltage generator

5.2.3.3. Other consideration. During the above discussion, we noticed that particles fall on the bonding surface will influence the yield of bonding, so one should avoid introducing particles onto clean bonding surface. The system mentioned here requires cleaning and bonding at separate locations, and the wafers need to be transported from the cleaning area to the bonding platform. Particles may collect on the cleaned wafer surfaces during transportation. A future system will try to do the two steps at the same location or even combine the two steps into one, so the bonding surface can be void free.

CHAPTER VI

CONCLUSION

MEMS (microelectromechanical systems) are an outgrowth of silicon technology. Microfabrication techniques is needed to make those micro-devices possible, Though still under development, MEMS has shown a bright prospective and many products based on micromachining technology have made it into market.

In the fall of 1999, the Sensor System Center (SSC) began its research on the design, fabrication and testing of wafer-based micro system. Based on its well equipped Maddox Lab, most process steps used for micro sensor fabrication, like oxidation, lithography, CVD, PVD, and wet etching were inherited from semiconductor processing. Some relatively new processes, like bonding have also been developed for this purpose.

The research done in this thesis includes theoretical descriptions, fabrication examples of these processes, as well as the fabrication of a bulk micromachinined accelerometer. An anodic bonding system was assembled to facilitate wafer bonding. This work provides a basis for further development and fabrication of advanced MEMS devices.

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