A VLSI OPTICAL DETECTOR ARRAY EMPLOYING HETERODYNE DETECTION

by

TEJVANSH SINGH SONI, B.S.E.E.

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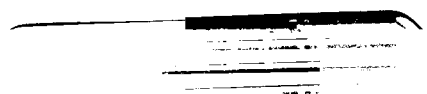

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CHAPTER 1

INTRODUCTION

1.1 Overview

The integration of image sensors with circuitry for driving the image sensor and performing on-chip signal processing is becoming increasingly popular for a multitude of signal processing applications. A high degree of on-chip signal processing helps enable miniaturization of instrument systems and simplify system interfaces.

In this work, the design of a powerful and versatile VLSI optical sensor array, with on-chip circuitry to perform temporal electronic heterodyne detection on a pixel-by-pixel basis is presented. Heterodyne detection techniques significantly enhance the dynamic range and signal to noise ratio, as compared to base-band detectors. The unavailability of heterodyne detector arrays has been a bottleneck in many image-processing systems, restricting the use of heterodyne detection techniques to scanning based systems, or systems having a single temporal output, such as acousto-optic space integrating correlators and convolvers. The need for heterodyne detector arrays in acousto-optics has been emphasized by prominent researchers in the field.[1]

The availability of a heterodyne optical detector array would find usage in numerous optical techniques employing temporal or spatio-temporal modulation. Low to moderate (<100 MHz) devices would find wide use in applications like phase shift interferometery,[2] and real time image processing.[3-5] Wide band(>100 MHz) devices

would find applications in acousto-optics and optical spatio-temporal memories based on spectral hole burning.[6-8]

Numerous designs of smart-pixel arrays and smart array detectors performing dedicated image processing operations have been proposed. The heterodyne optical detector array proposed in this work has the unique capability of performing a multitude of optical signal processing operations. The detector array can be used to extract edge related information, such as the directional gradients and Laplacian components of images. Real-time spatial filtering operations on images can also be performed using the detector array. The detector array can also be used for contour-tracking operations.[5]

The heterodyne array, while detecting high bandwidth optical signals, yields a base-band signal, which greatly reduces the burden of off-chip input/output, memory storage and digital post-processing. A technique somewhat related to our 2-D image processing scheme has been described in ref[9]. This technique, however is closely allied to digital image processing algorithms, as the image is spatially sampled, and the sampled data is sent to an analog array processor in a scheme similar to the difference equations used in conventional digital image filtering.

The MOSIS foundry fabrication facilities were used for a preliminary design of a heterodyne detector element (photodetector with the electronic detection circuitry). We used the Orbit 2.0μ N-Well process for the fabrication of our prototypes. The Orbit 2.0μ N-Well process is not optimized for the fabrication of photo-diode arrays, which was a major constraint in our design. We have, though, demonstrated proof-of-principle results regarding the feasibility of the fabrication of heterodyne detector arrays. In this work we

present a generalized architecture of the heterodyne detector array, and the test results of the individual circuit blocks. For high bandwidth(>100 MHz) applications we recommend the use of SEED(Self Electro-optic Devices) diode arrays, flip-chip bonded to the CMOS chip (containing the processing circuitry).

Real time 2-D image processing applications of the heterodyne detector array are highlighted in this work. Most of the information content in visual images resides in edges, which represent significant spatial gradients of intensity in the image. Consequently edge detection/enhancement operations are fundamental in numerous image processing applications like image segmentation, registration, object identification, boundary extraction and boundary representation.

Edge detection and enhancement operations are generally achieved by means of various digital filtering techniques, wherein the image is first sampled, digitized and then uploaded to a computer. Digital edge filters like the Sobel and Laplacian[10,11] operators are then used. These operations, though relatively simple to perform, often become a bottleneck, due to the large throughput required in real-time high resolution image processing systems. Also, the edge operators, by nature, are differential operators, and are consequently highly susceptible to noise. The noise is generally dealt with by using digital smoothing filters, which have the undesirable effect of compromising spatial resolution.

A scanning based spatio-temporal technique which acquires first and second order spatial derivatives of images is described in ref[5]. The image processing capabilities of the system are by virtue of the modulation of the illumination and the image detection systems. In this thesis, a 2-D image processing system based on the heterodyne optical

detector array is also proposed. This image processing system is an extension of the scanning based system proposed in ref[5]. This system would have the ability to realize continuously variable spatial resolution (with the maximum resolution equal to the detector spacing) and would be able to extract arbitrary spatial derivatives of an image. The ability to extract the spatial derivatives in a parallel fashion would potentially provide a high throughput/frame rate in real time image processing systems in contrast to the digital techniques. In addition, since this system does not have to rely on discrete spatial sampling of the image, it enjoys potential advantages over the digital image processing techniques in terms of noise rejection. This system would also be able to perform 2-D linear spatial filtering of the image.

1.2 Structure of Thesis

Chapter 2 gives a theoretical analysis of the 2-D scan based spatio-temporal image processing system and its extension to a parallel acquisition 2-D image processing system. Simulaton results are also presented. Chapter 3 presents the design of the heterodyne optical detector array and the processing circuitry. Chapter 4 details the Pspice simulation and experimental results obtained from our first detector array prototype. Conclusions and suggestions on further work are presented in Chapter 5.

CHAPTER 2

THEORY

We begin our discussion by presenting the theoretical analysis of the 2-D spatio-temporal image processing system presented in ref[5]. Then we present the logical extension of the concept presented in ref[5] to a parallel acquisition 2-D spatio-temporal image processing system employing a 2-D array of heterodyne optical detectors. The system design is presented next, followed by the simulation results.

2.1 2-D Scanning Based Spatio-temporal System

A block diagram representation of the system is depicted in Figure 2-1. A 2-D sinusoidal perturbation is superimposed on the normal raster motion of the scanning spot by the scanning mechanism. The instantaneous position of the scanning spot, in general, is given parametrically by the vector:

$$p(t) = \left[x(t), y(t)\right] \tag{2-1}$$

where

$$x(t) = x_0 + A_x \cos(\Omega_x t + \Phi_x)$$

and

$$y(t) = y_0 + A_y \cos(\Omega_y t + \Phi_y). \tag{2-2}$$

Here x_0 and y_0 are slowly varying time functions that represent the normal raster scan motion of the scanning spot. The target mask can be described as a 2-D intensity transmittance

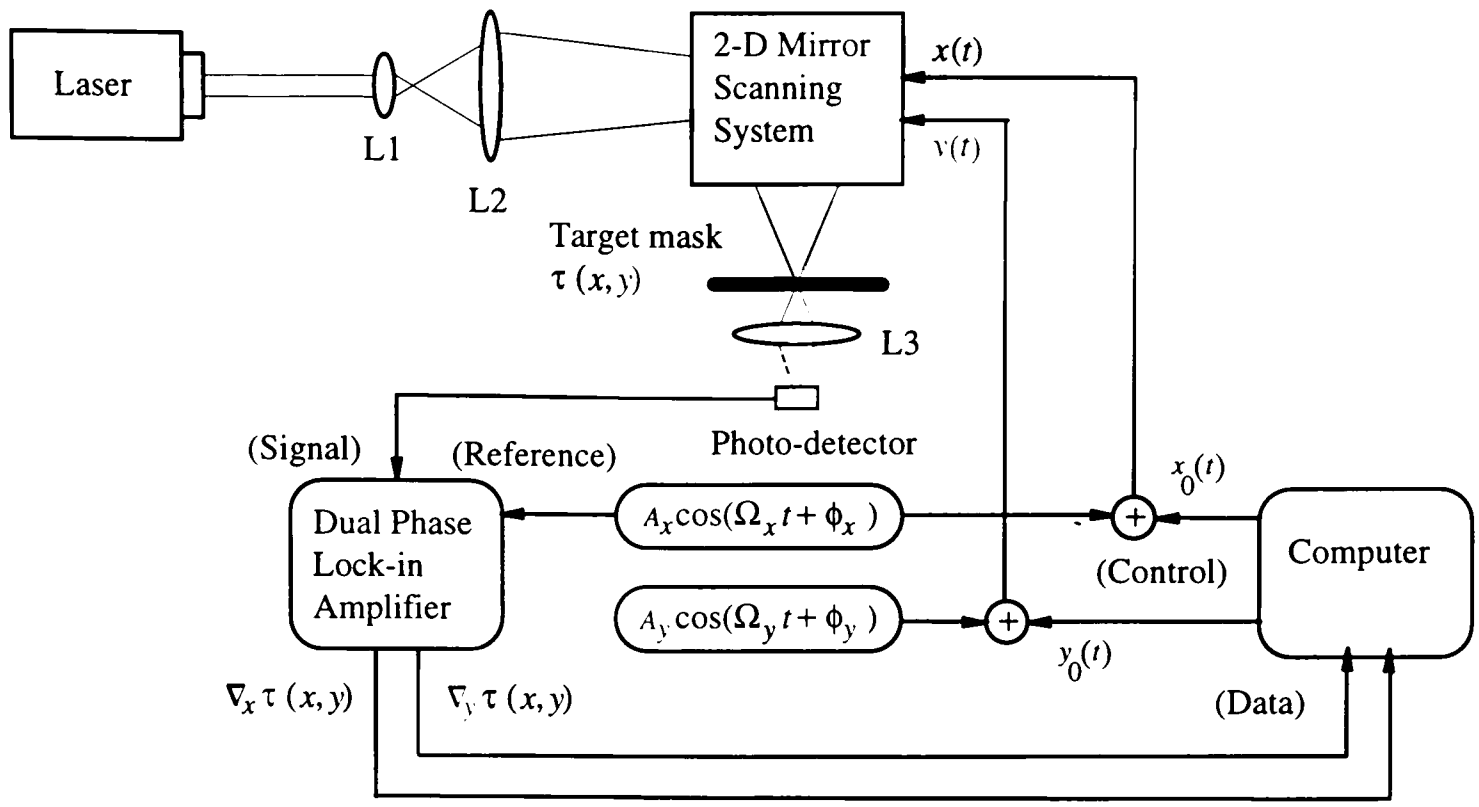


Figure 2-1. "Spatio-Temporal" Gradient Detection System

function $\tau(x,y)$. Assuming the lens collects all of the light transmitted through the target mask, the photodetector current is given by:

$$i_d(t) = K\int_{-\infty}^{+\infty}\int_{-\infty}^{+\infty}\tau(x, y)s\big[x(t), y(t)\big]dxdy, \tag{2-3}$$

where $s(x,y)$ represents the intensity profile of the scanning spot and K is the effective gain constant of the system. Assuming an infinitesimally small scanning spot, $s(x,y)$ can be approximated by a Dirac delta function. The photodetector current given in Equation (2-3) can therefore be written as:

$$i_d(t) = K\tau\big[x(t), y(t)\big]. \tag{2-4}$$

Thus we see that the photodetector current $i_d(t)$ is directly proportional to the intensity transmittance of the target mask $\tau(x,y)$ at the location $x(t)$ and $y(t)$ and constitutes a time dependent representation of the image. For finite-sized scanning spot intensity

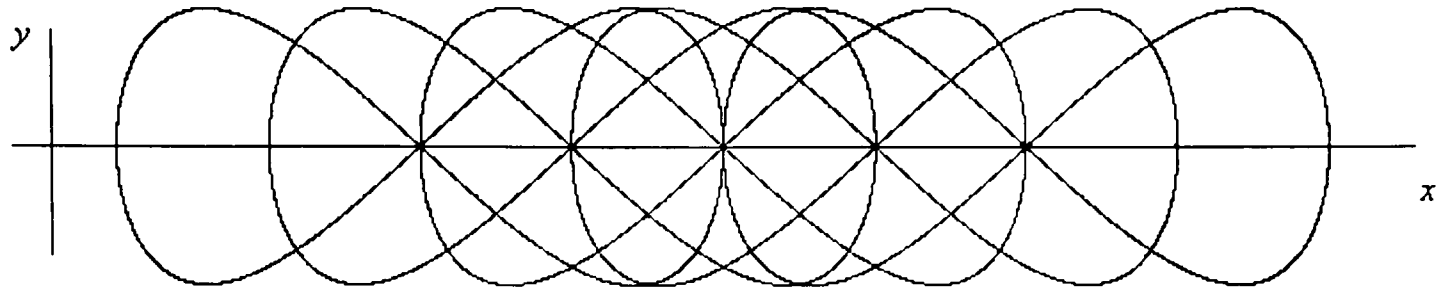


Figure 2-2. Lissajous Pattern Superimposed on Linear Raster Scan

profiles, the effect can be incorporated by modifying the intensity transmittance of the target mask to

$$\tau'(x, y) = \tau(x, y) \otimes s(x, y), \tag{2-5}$$

so that the result in Equation (2-4) is still valid. Here the symbol '⊗' represents the spatial cross-correlation operation.

The trajectory of the scanning spot is determined by the amplitudes, phase angles and frequencies selected for the sinusoidal perturbations. For heterodyne detection the perturbation frequencies for the x and y axes should be different and incommensurable. This results in a Lissajous pattern being superimposed on the normal raster scan trajectory of the scanning spot. An example is shown in Figure 2-2. The reason we want the frequencies to be incommensurable will become clear in the discussion to follow.

2.1.1 Taylor Series Analysis

If the linear raster scan motion of the scan is slow compared to the *x*-*y* sinusoidal perturbations, then x_0 and y_0 can be considered the nominal position of the scanning spot.

The intensity transmittance function of the 2-D mask can be expanded as a Taylor series about the nominal spot position (x_0,y_0) as:

$$\tau(x,y)=\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{1}{m!n!}\frac{\partial^{m+n}\tau(x_0,y_0)}{\partial x^m\partial y^n}(x-x_0)^m(y-y_0)^n. \tag{2-6}$$

By using Equation 2-4 the photodetector current can be written as:

$$i_d(t)=K\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{1}{m!n!}\frac{\partial^{m+n}\tau(x_0,y_0)}{\partial x^m\partial y^n}\left[x(t)-x_0\right]^m\left[y(t)-y_0\right]^n, \tag{2-7}$$

where K is the effective gain of the system as defined earlier. Substituting the expression for the scanning spot position from Equation (2-2) into Equation (2-7), we obtain,

$$i_d(t)=K\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{A_x^mA_y^n}{m!n!}\frac{\partial^{m+n}\tau(x_0,y_0)}{\partial x^m\partial y^n}\cos^m(\Omega_x t+\varphi_x)\cos^n(\Omega_y t+\Phi_y). \tag{2-8}$$

As is clear from Equation (2-8), for a nominal position (x_0,y_0) of the scanning spot, the photodetector current can be expressed as the summation of the partial derivatives of the 2-D intensity transmittance function of the target mask, i.e., $\tau(x,y)$, at the point (x_0,y_0). Each spatial derivative can be designated by selecting the appropriate pair of summation indices m and n. The temporal characteristics of the photodetector current suggest that judicious choice of the parameters Ω_x, Ω_y, ϕ_x and ϕ_y would ensure that the different spatial derivatives of $\tau(x,y)$ reside at unique carrier frequencies. This is the reason why we want the x and y perturbation frequencies Ω_x, Ω_y to be incommensurable. For heterodyne detection, selecting

$$\begin{aligned}&\Omega_x\neq\Omega_y\\&\Phi_x=\Phi_y=0\\&A_x=A_y=A_0,\end{aligned} \tag{2-9}$$

the photodetector current can be expressed as:

$$i_d(t) = K\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{A_0^{m+n}}{m!n!}\frac{\partial^{m+n}\tau(x_0, y_0)}{\partial x^m \partial y^n}\cos^m(\Omega_x t)\cos^n(\Omega_y t). \tag{2-10}$$

On expanding the photodetector current to third-order terms ($m+n \leq 3$) and applying appropriate trignometric identities we get,

$$\begin{aligned}
i_d(t) \propto\ & \tau(x_0, y_0) + \left\{A_0\frac{\partial}{\partial y}\tau(x_0, y_0)\cos(\Omega_y t)\right\} + \frac{A_0^2}{4}\frac{\partial^2}{\partial y^2}\tau(x_0, y_0) \\
& + \frac{A_0^2}{4}\frac{\partial^2}{\partial y^2}\tau(x_0, y_0)\cos(2\Omega_y t) + \frac{A_0^3}{8}\frac{\partial^3}{\partial y^3}\tau(x_0, y_0)\cos(\Omega_y t) \\
& + \frac{A_0^3}{24}\frac{\partial^3}{\partial y^3}\tau(x_0, y_0)\cos(3\Omega_y t) + \left\{A_0\frac{\partial}{\partial x}\tau(x_0, y_0)\cos(\Omega_x t)\right\} \\
& + \frac{A_0^2}{2}\frac{\partial^2}{\partial x\partial y}\tau(x_0, y_0) + \frac{A_0^2}{2}\frac{\partial^2}{\partial x\partial y}\tau(x_0, y_0)\cos\left[(\Omega_x + \Omega_y)t\right] \\
& + \frac{A_0^3}{4}\frac{\partial^3}{\partial x\partial y^2}\tau(x_0, y_0)\cos(\Omega_x t) + \frac{A_0^3}{8}\frac{\partial^3}{\partial x\partial y^2}\tau(x_0, y_0)\cos\left[(\Omega_x - 2\Omega_y)t\right] \\
& + \frac{A_0^3}{8}\frac{\partial^3}{\partial x\partial y^2}\tau(x_0, y_0)\cos\left[(\Omega_x + 2\Omega_y)t\right] + \frac{A_0^2}{4}\frac{\partial^2}{\partial x^2}\tau(x_0, y_0) \\
& + \frac{A_0^2}{4}\frac{\partial^2}{\partial x^2}\tau(x_0, y_0)\cos(2\Omega_x t) + \frac{A_0^3}{4}\frac{\partial^3}{\partial x^2\partial y}\tau(x_0, y_0)\cos(\Omega_y t) \\
& + \frac{A_0^3}{8}\frac{\partial^3}{\partial x^2\partial y}\tau(x_0, y_0)\cos\left[(2\Omega_x - \Omega_y)t\right] + \frac{A_0^3}{8}\frac{\partial^3}{\partial x^2\partial y}\tau(x_0, y_0)\cos\left[(2\Omega_x + \Omega_y)t\right] \\
& + \frac{A_0^3}{8}\frac{\partial^3}{\partial x^3}\tau(x_0, y_0)\cos(\Omega_x t) + \frac{A_0^3}{24}\frac{\partial^3}{\partial x^3}\tau(x_0, y_0)\cos(3\Omega_x t) + \ldots
\end{aligned} \tag{2-11}$$

The gradient components $\nabla_x\tau(x_0,y_0)$ and $\nabla_y\tau(x_0,y_0)$, indicated by the bracketed terms in Equation (2-11), reside on carrier frequencies Ω_x and Ω_y, with these components given by:

$$\nabla_y \tau(x_0, y_0) =$$
$$\left(A_0 \frac{\partial}{\partial y} \tau(x_0, y_0) + \frac{A_0^3}{4} \frac{\partial^3}{\partial x^2 \partial y} \tau(x_0, y_0) + \frac{A_0^3}{8} \frac{\partial^3}{\partial y^3} \tau(x_0, y_0) + \ldots \right) \cos(\Omega_y t)$$
$$\approx A_0 \frac{\partial}{\partial y} \tau(x_0, y_0) \cos(\Omega_y t),$$

and

$$\nabla_x \tau(x_0, y_0) =$$
$$\left(A_0 \frac{\partial}{\partial x} \tau(x_0, y_0) + \frac{A_0^3}{4} \frac{\partial^3}{\partial x \partial y^2} \tau(x_0, y_0) + \frac{A_0^3}{8} \frac{\partial^3}{\partial x^3} \tau(x_0, y_0) + \ldots \right) \cos(\Omega_x t) \qquad (2\text{-}12)$$
$$\approx A_0 \frac{\partial}{\partial x} \tau(x_0, y_0) \cos(\Omega_x t).$$

The above approximations are valid if the magnitude of the sinusoidal perturbations, i.e., A_0 in this case, is less than the smallest feature size in the 2-D intensity transmittance function. The directional gradients can be easily detected by band-pass filters/detectors tuned to the base frequencies Ω_x and Ω_y. In general, we observe that the spatial derivatives reside at two unique frequencies according to the formula:

$$\frac{\partial^{m+n}}{\partial x^m \partial y^n} \tau(x, y) \Rightarrow \cos\left[(m\Omega_x \pm n\Omega_y) t \right]. \qquad (2\text{-}13)$$

Equation (2-13) shows that any specific frequency in the photodetector signal will contain the information of several different spatial derivatives and may lie in close proximity to other frequency components of the photodetector current output, which in turn might contain derivative information of higher orders. Therefore, to successfully extract the desired order of the spatial derivative, the frequencies Ω_x and Ω_y must be incommensurable and judiciously selected to ensure the desired frequency component can be extracted by the detecting circuitry, without any aliasing effects.

2.1.2 Fourier Analysis

The intensity transmittance $\tau(x,y)$ of the mask can be written as a (2-D spatial) inverse Fourier transform as:

$$T(f_x, f_y) = \int_{-\infty}^{+\infty}\int \tau(x, y)\exp\left[-j2\pi(f_x x + f_y y)\right]dxdy, \tag{2-14}$$

where $T(f_x,f_y)$ is the 2-D spatial Fourier transform of $\tau(x,y)$. Likewise the transmittance of the mask can be expressed as the inverse Fourier transform:

$$\tau(x, y) = \int_{-\infty}^{+\infty}\int T(f_x, f_y)\exp\left[j2\pi(f_x x + f_y y)\right]df_x df_y. \tag{2-15}$$

From Equation (2-4), the photodetector current can be written as:

$$i_d(t) = K\int_{-\infty}^{+\infty}\int T(f_x, f_y)\exp\left\{j2\pi\left[f_x x(t) + f_y y(t)\right]\right\}df_x df_y. \tag{2-16}$$

Using Equations (2-2), the signal can be expressed as:

$$i_d(t) = K\int_{-\infty}^{+\infty}\int T(f_x, f_y)\exp\left[j2\pi(f_x x_o + f_y y_o)\right]\exp\left[j2\pi f_x A_x \cos(\Omega_x t + \Phi_x)\right]$$

$$\times\exp\left[j2\pi f_y A_y \cos(\Omega_y t + \Phi_y)\right]df_x df_y. \tag{2-17}$$

We observe that the expression for the photodetector current takes the general form of a tone modulated FM signal. To make this relationship more explicit let $m_{fx}=A_x 2\pi f_x$ and $m_{fy}=A_y 2\pi f_y$. Equation (2-17) can now be written as:

$$i_d(t) = K\int_{-\infty}^{+\infty}\int T(f_x, f_y)\exp\left[j2\pi(f_x x_o + f_y y_o)\right]\exp\left[jm_{fx} \cos(\Omega_x t + \Phi_x)\right]$$

$$\times\exp\left[jm_{fy} \cos(\Omega_y t + \Phi_y)\right]df_x df_y, \tag{2-18}$$

where m_{fx} and m_{fy} are the indices of modulation. Note that the indices of modulation are directly proportional to the amplitude of the sinusoidal perturbations. Expanding the time

varying exponential terms under the integral, into complex Fourier series representations,[12,13] Equation (2-18) may be written as:

$$i_d(t) = K\int_{-\infty}^{+\infty}\int T(f_x, f_y)\exp\left[j2\pi(f_x x_o + f_y y_o)\right]\times \sum_{m=-\infty}^{+\infty} j^m J_m(m_{fx})\exp\left[jm(\Omega_x t + \Phi_x)\right]$$

$$\times \sum_{n=-\infty}^{+\infty} j^n J_n(m_{fy})\exp\left[jn(\Omega_y t + \Phi_y)\right]df_x df_y. \qquad (2\text{-}19)$$

where $J_m(m_{fx})$ and $J_n(m_{fy})$ are Bessel functions of the first kind, of order m and n, respectively. By pairing the $\pm m$ and $\pm n$ terms, using Euler's identities, applying the first term of the series approximation,[14]

$$J_m(m_{fx}) = \frac{m_{fx}^m}{2^m m!}\left(1 - \frac{m_{fx}^2}{2^2(m+1)} + \ldots\right) \qquad (2\text{-}20)$$

and distributing the integration throughout the expression, the photodetector current is approximated by:

$$i_d(t) \approx K\int_{-\infty}^{\infty}\int T(f_x, f_y)\exp\left[j2\pi(f_x x_o + f_y y_o)\right]df_x df_y$$

$$+ 2K\sum_{n=1}^{\infty}\frac{A_y^n}{2^n n!}\cos\left[n(\Omega_y t + \Phi_y)\right]\times\int_{-\infty}^{\infty}\int (j2\pi f_y)^n T(f_x, f_y)\exp\left[j2\pi(f_x x_o + f_y y_o)\right]df_x df_y$$

$$+ 2K\sum_{m=1}^{\infty}\frac{A_x^m}{2^m m!}\cos\left[m(\Omega_x t + \Phi_x)\right]\times\int_{-\infty}^{\infty}\int (j2\pi f_x)^m T(f_x, f_y)\exp\left[j2\pi(f_x x_o + f_y y_o)\right]df_x df_y$$

$$+ 2K\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\frac{A_x^m}{2^m m!}\frac{A_y^n}{2^n n!}\left\{\cos\left[m(\Omega_x t + \Phi_x) - n(\Omega_y t + \Phi_y)\right] + \cos\left[m(\Omega_x t + \Phi_x) + n(\Omega_y t + \Phi_y)\right]\right\}$$

$$\times\int_{-\infty}^{\infty}\int (j2\pi f_x)^m (j2\pi f_y)^n T(f_x, f_y)\exp\left[j2\pi(f_x x_o + f_y y_o)\right]df_x df_y, \qquad (2\text{-}21)$$

where we have substituted $A_x 2\pi f_x$ for m_{fx} and $A_y 2\pi f_y$ for m_{fy}. By recalling the relationship between the Fourier Transform and the derivative of a function,

$$\frac{\partial^{m+n}\tau(x,y)}{\partial x^m \partial y^n} = \int_{-\infty}^{\infty}\int (j2\pi f_x)^m (j2\pi f_y)^n T(f_x, f_y)\exp\left[j2\pi(f_x x_o + f_y y_o)\right] df_x df_y, \tag{2-22}$$

making use of the relation in Equation (2-22), the photodetector current given in Equation (2-21) can be written as:

$$\begin{aligned} i_d(t) \approx K\tau(x_0, y_o) &+ 2K\sum_{n=1}^{\infty}\frac{A_y^n}{2^n n!}\cos\left[n(\Omega_y t + \Phi_y)\right]\frac{\partial^n}{\partial y^n}\tau(x_o, y_o) \\ &+ 2K\sum_{m=1}^{\infty}\frac{A_x^m}{2^m m!}\cos\left[m(\Omega_x t + \Phi_x)\right]\frac{\partial^m}{\partial x^m}\tau(x_o, y_o) \\ &+ 2K\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\frac{A_x^m}{2^m m!}\frac{A_y^n}{2^n n!}\times\left\{\cos\left[(m\Omega_x + n\Omega_y)t + (m\Phi_x + n\Phi_y)\right]\right. \\ &\left. + \cos\left[(m\Omega_x - n\Omega_y)t + (m\Phi_x - n\Phi_y)\right]\right\}\times\frac{\partial^{m+n}}{\partial x^m \partial y^n}\tau(x_o, y_o). \end{aligned} \tag{2-23}$$

This result is in agreement with the relation derived in Equation (2-11). Provided Ω_x and Ω_y are incommensurable, it is evident from the above expression that each partial derivative of the mask intensity transmittance $\tau(x,y)$ at the nominal scanning spot location (x_o,y_o) resides on a unique carrier frequency in the detector signal, and the mixed partial derivatives, i.e., $m,n\neq 0$, reside on two frequencies (a sum and a difference frequency).

The previous assumption that the Bessel functions can be approximated by the first term of their Taylor series expansions(Equation 2-20), is valid provided that

Figure 2-3. Binary Mask of "Texas"

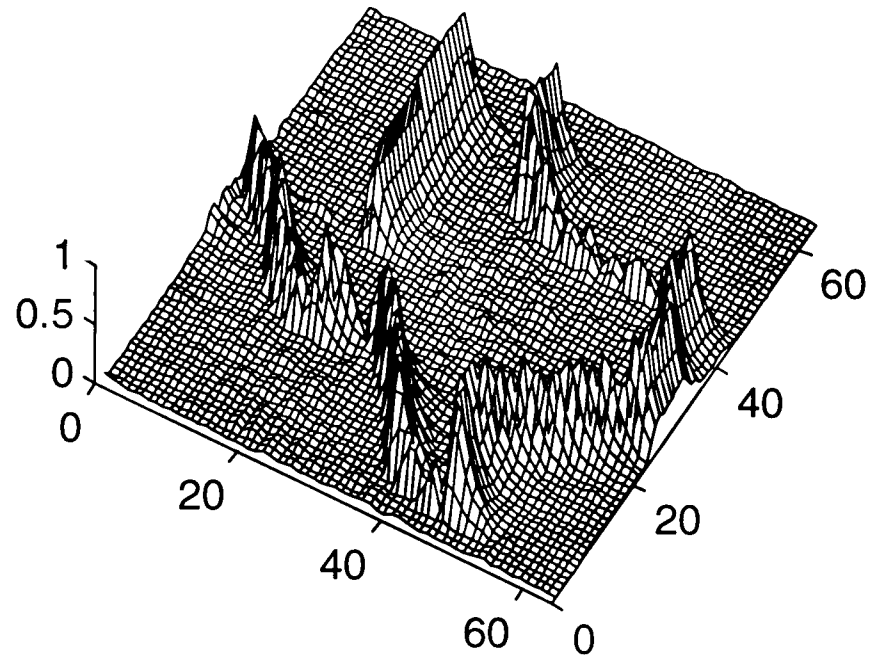


Figure 2-4. Distribution of $|\partial\tau(x,y)/\partial x|$

$$\frac{m_{fx}^2}{4(m+1)} << 1 \text{ or } (A_x 2\pi f_x)^2 << 4(m+1). \tag{2-24}$$

This condition can also be expressed as:

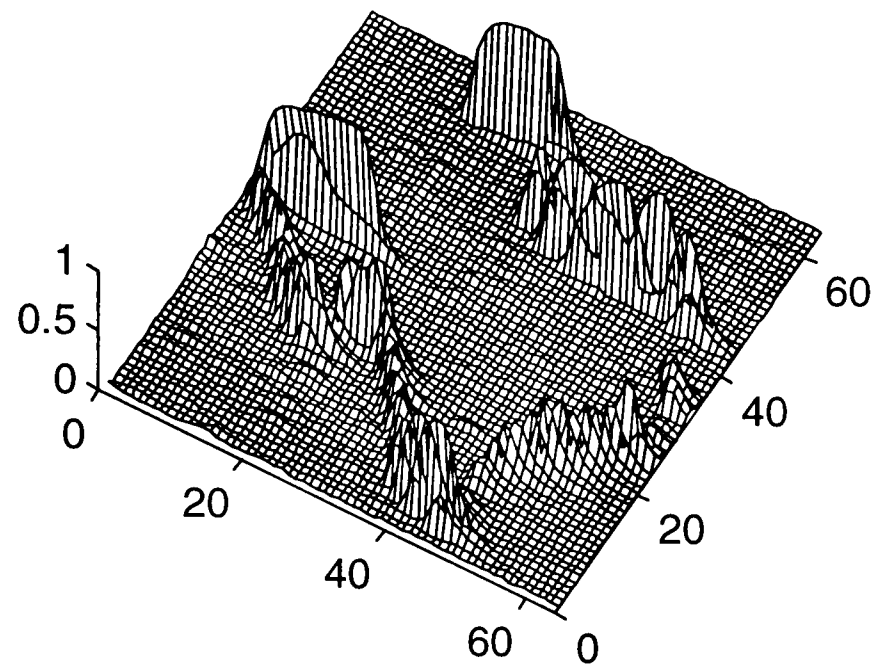


Figure 2-5. Distribution of $|\partial\tau(x,y)/\partial y|$

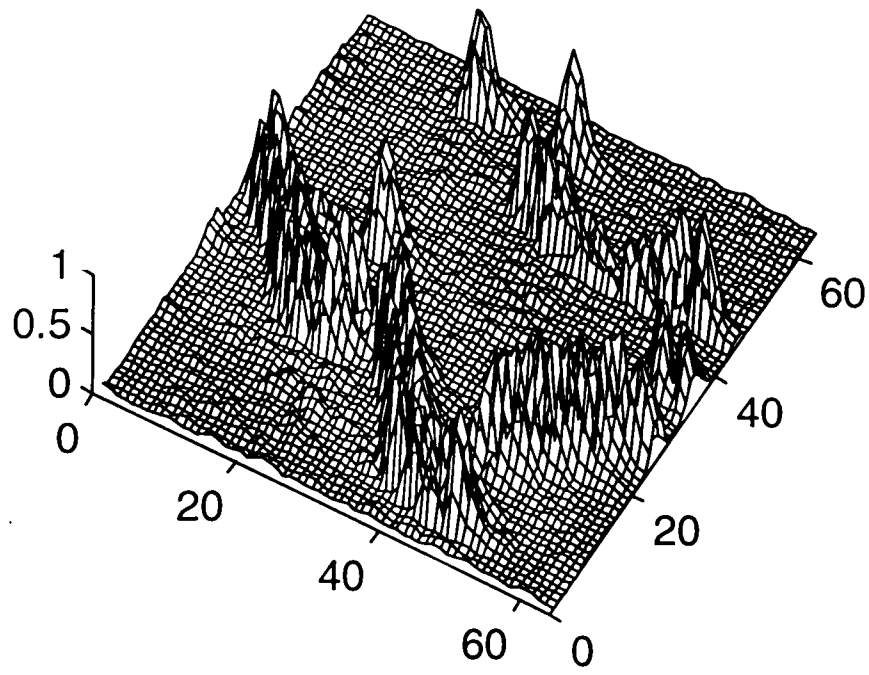


Figure 2-6. Distribution of $|\partial^2\tau(x,y)/\partial x\partial y|$

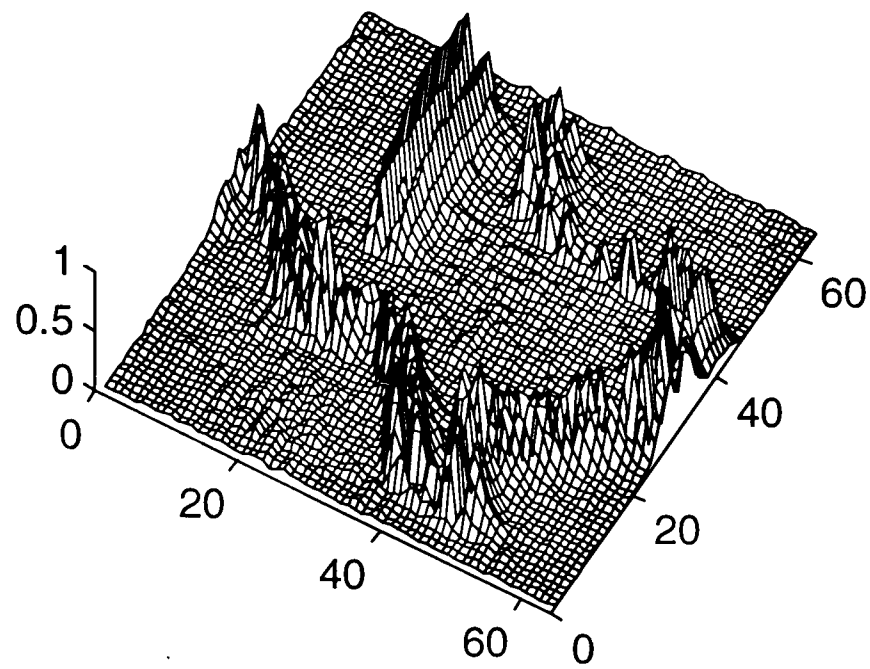


Figure 2-7. Distribution of $|\partial^2\tau(x,y)/\partial x^2|$

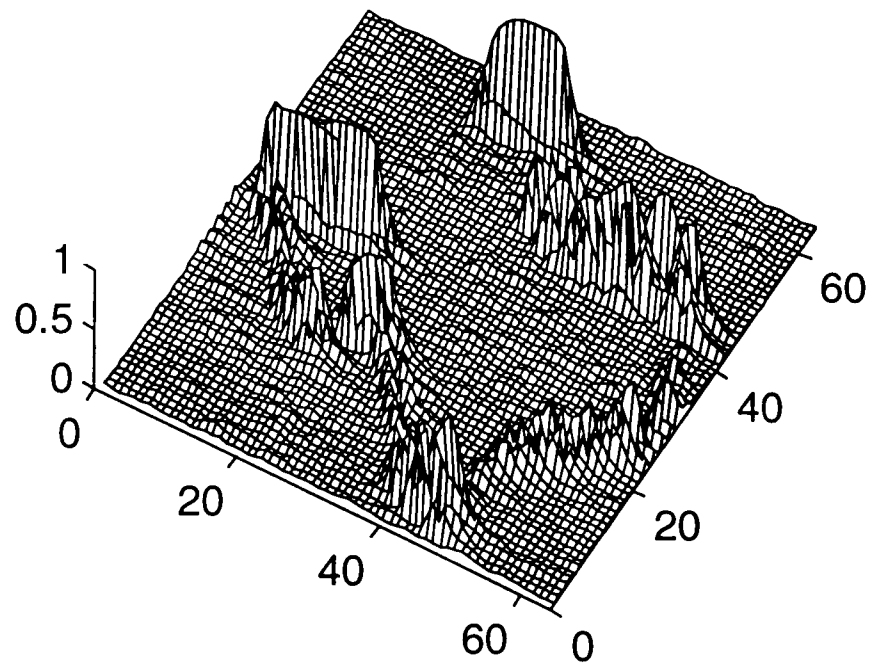


Figure 2-8. Distribution of $|\partial^2\tau(x,y)/\partial y^2|$

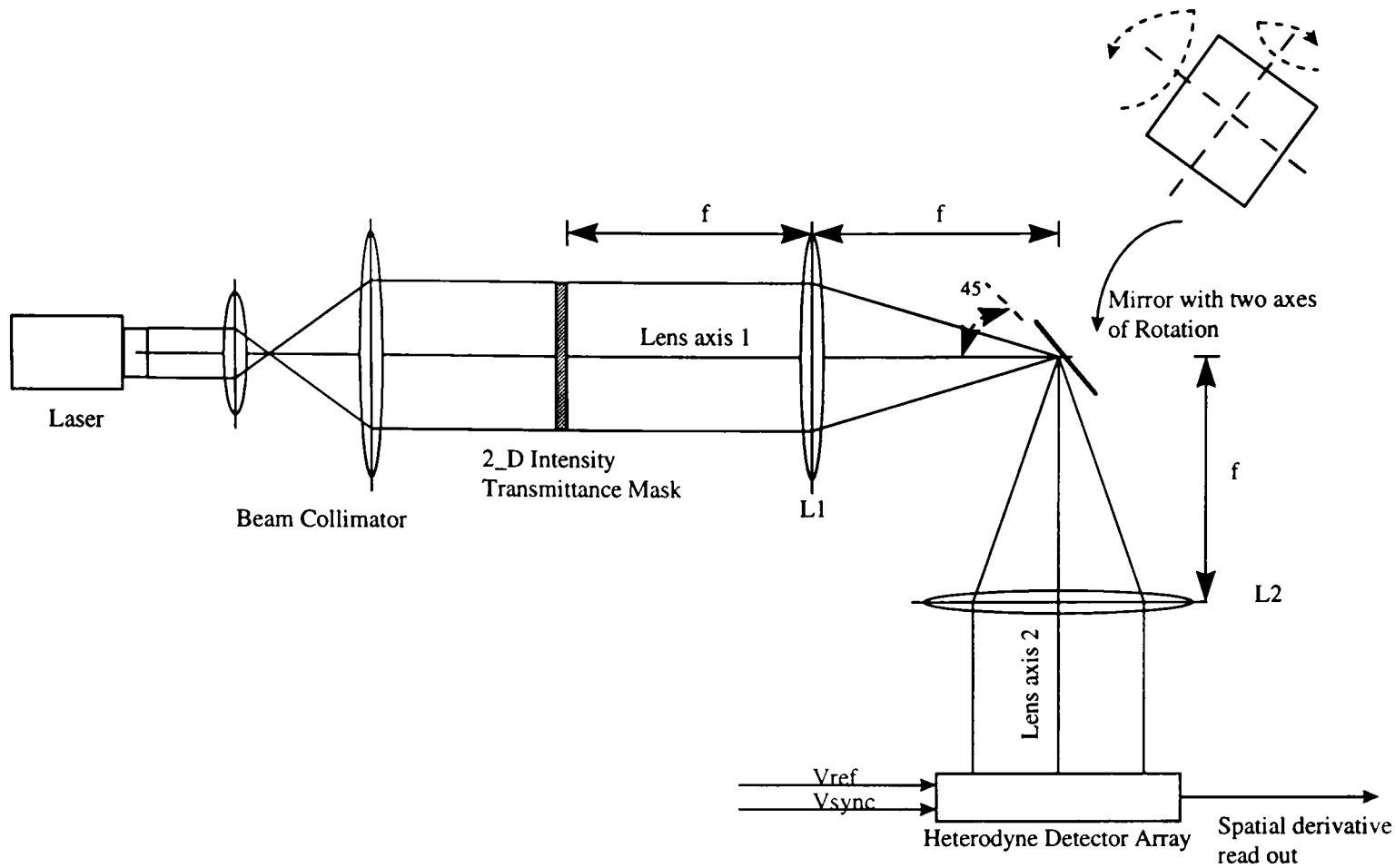


Figure 2-9. Spatial-Derivative Extraction Using the Heterodyne Detection Array

$$A_x < \frac{\sqrt{m+1}}{\pi}\delta_x \text{ and } A_y < \frac{\sqrt{n+1}}{\pi}\delta_y, \tag{2-25}$$

where $\delta_x=1/B_x$ and $\delta_y=1/B_y$ are the minimum resolvable features of the image in the X and Y extents respectively, and B_x, B_y represent the X and Y spatial bandwidths of the image.

Some of the proof-of-principle results presented in ref[5] are given below for the sake of completeness of discussion. First-order (Figures 2-4, 2-5) and second-order (Figures 2-6, 2-7 and 2-8) spatial derivatives of a mask (Figure 2-3), which comprised a binary image of the map of Texas, were successfully extracted using this technique. The system was configured to detect the first derivative with respect to x ($\partial\tau/\partial x$) by setting $\Omega_{ref} = \Omega_x$. The vertical edges are emphasized, there is no response to the horizontal edges

and a reduced response to the oblique edges is seen, as expected. The first derivative with respect to y ($\partial\tau/\partial y$) was extracted by choosing $\Omega_{ref} = \Omega_x$. This time the result highlights the horizontal edges, with no response to the vertical edges and a reduced response to the slant edges. A second-order joint spatial derivative ($\partial^2\tau/\partial x\partial y$) was extracted, with $\Omega_{ref} = (\Omega_x+\Omega_y)$. The result emphasizes the oblique edges, with no response to the horizontal or the vertical edges. This also vindicates our claim that the system can extract arbitrary order spatial derivatives. Second-order derivatives with respect to x and y ($\partial^2\tau/\partial x^2$, $\partial^2\tau/\partial y^2$) were also extracted by setting Ω_{ref} equal to $2\Omega_x$ and $2\Omega_y$, respectively, and the results are given in Figures 2-7 and 2-8.

2.2 Spatial Derivative Extraction using a 2-D Heterodyne Detector Array

The scheme of extraction for the spatial derivatives of a 2-D intensity transmittance mask using a heterodyne detector array is depicted in Figure 2-9. A collimated beam of light is projected onto the mask. The mask is placed in the front focal plane of the double convex lens. The Fourier transform of the mask appears in the back focal plane of the lens, where a rotating mirror, capable of rotation about two normal axes is placed. A possible arrangement for rotating the mirror is presented in Figure 2-11. In the steady state, the mirror is aligned at an angle of 45° with the lens axes. By electing to place the mirror in the back focal plane, we can use a small size, hence low mass mirror, and can therefore use higher perturbation frequencies for the mirror. The second double-convex lens does a second Fourier transform, and the inverted image of the mask falls on the heterodyne detector array. The mirror is made to oscillate about its two axes of

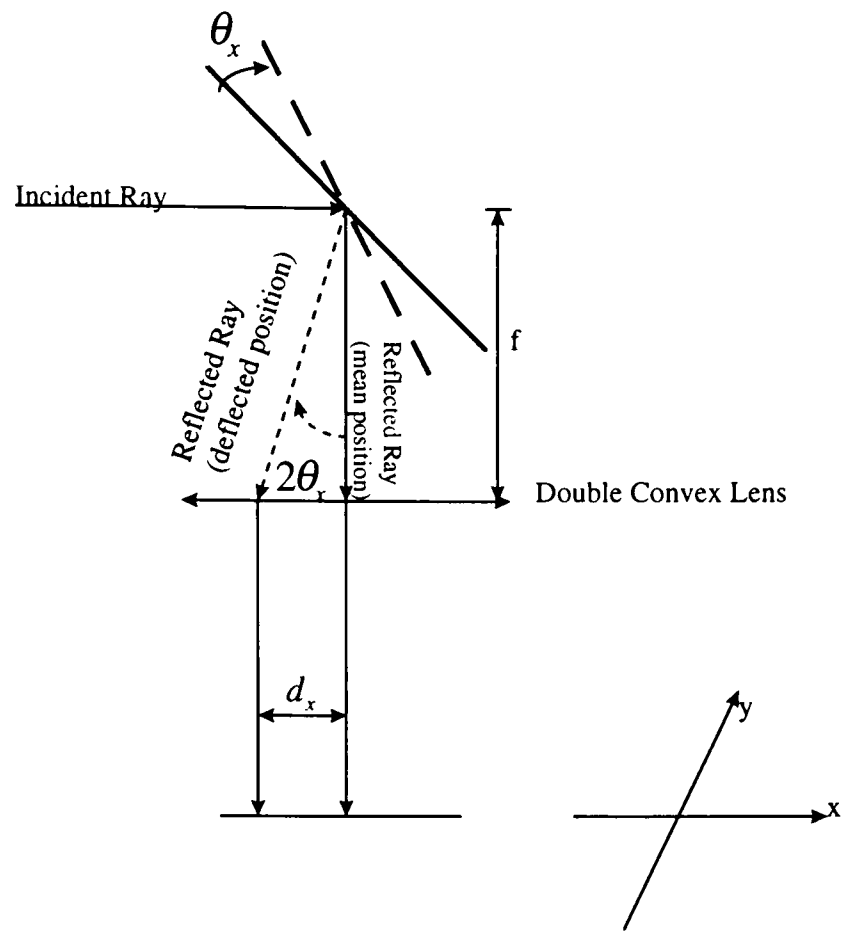


Figure 2-10. Ray Tracing for Mean and Displaced Positions of the Mirror

rotation, as a result of which the heterodyne detector array sees a laterally displaced image of the mask, sinusoidally perturbed, along the x and y axes. The relationship between the mirror rotation and the x and y perturbation of the mask image, as seen by the detector array can be very easily established. In Figure 2-10, we show two different positions of the mirror. A sample ray has been traced for two different positions of the mirror. For a small rotation θ_x of the mirror, the lateral displacement along the x-axis, as seen in the plane of the detector array is given by:

$$d_x = f(2\theta_x). \tag{2-26}$$

If the mirror is rotated sinusoidally, i.e.,

$$\theta_x = \frac{A_x}{2f}\cos(\Omega_x t + \Phi_x), \tag{2-27}$$

then

$$d_x = A_x \cos(\Omega_x t + \Phi_x). \tag{2-28}$$

Similar results can be obtained for displacement along the *y*-axis, giving

$$d_y = A_y \cos(\Omega_y t + \Phi_y). \tag{2-29}$$

It is easy to visualize from the above discussion that the image seen by the heterodyne detector array is actually vibrating along the x and y axes with the x and y displacements being given by Equations (2-28) and (2-29), respectively. Ignoring the inversion of the image due to the imaging system in Figure 2-4 a point (x_o,y_o) in the plane of the mask (object-plane) is mapped to a point (x_o,y_o) in the detector-plane (image-plane), where we have assumed an imaging system with unity magnification.

Let us assume that the mirror is stationary and (x_o,y_o) corresponds to the nominal position of a detector element. The image coordinates seen by the detector element due to the sinusoidal perturbation of the image are:

$$\left[x_i(t), y_i(t)\right] = \left[(x_o + A_x \cos(\Omega_x t + \Phi_x)), (y_o + A_y \cos(\Omega_y t + \Phi_y))\right], \tag{2-30}$$

where the subscript '*i*' has been used to denote the image plane. The detector current can thus be obtained from Equation (2-4) as:

$$\begin{aligned} i_{d_i}^{(0,0)}(t) &= K\tau\left[x_i(t), y_i(t)\right] \\ &= K\tau\left[(x_o + A_x \cos(\Omega_x t + \Phi_x)), (y_o + A_y \cos(\Omega_y t + \Phi_y))\right]. \end{aligned} \tag{2-31}$$

The superscript in the above equation indicates the coordinate of a particular detector element. Since we are assuming a unity magnification imaging system, a point (x_p,y_q) on

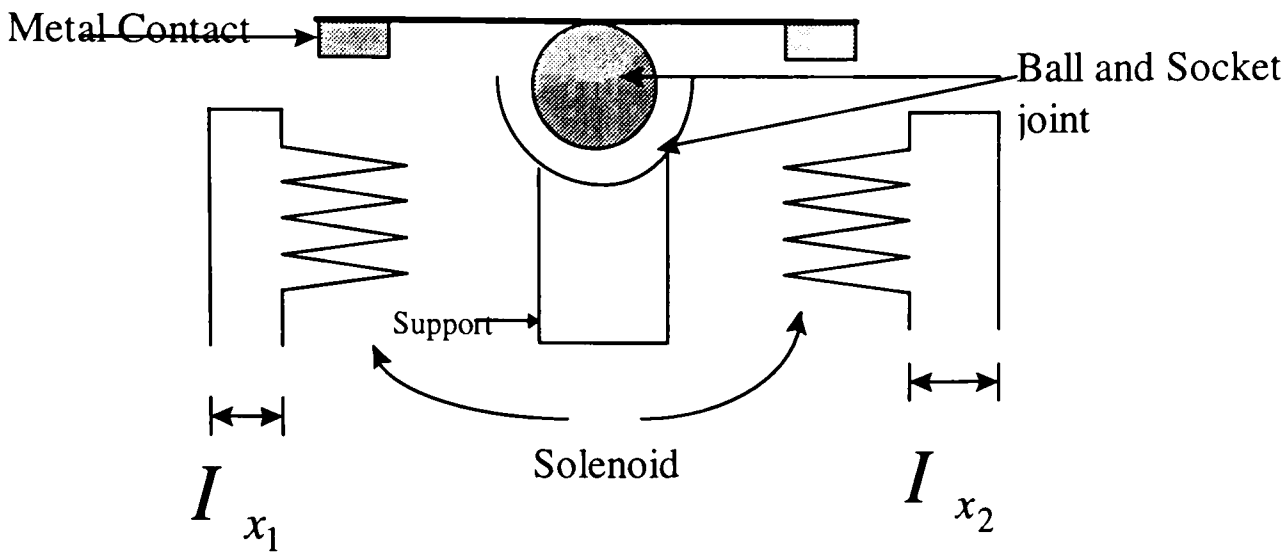


Figure 2-11. Cross-section of the Mirror Rotating System

the mask is mapped to a point (x_p,y_q) in the detector plane. Thus to generalize Equation (2-31), for a detector (p,q), the detector current can be written as:

$$i_{d_i}^{(p,q)}(t) = K\tau\Big[(x_p + A_x\cos(\Omega_x t + \Phi_x)),(y_q + A_y\cos(\Omega_y t + \Phi_y))\Big]. \qquad (2\text{-}32)$$

Following the analysis presented in Equations (2-6) through (2-10), the expression for the photodetector current for the (p,q) photo-diode can be written as:

$$i_{d_i}^{(p,q)}(t) = K\sum_{m=0}^{\infty}\sum_{n=0}^{\infty}\frac{A_0^{m+n}}{m!n!}\frac{\partial^{m+n}\tau(x_p,y_q)}{\partial x^m\partial y^n}\cos^m(\Omega_x t)\cos^n(\Omega_y t). \qquad (2\text{-}33)$$

The photodetector current from each detector element (p,q) is a summation of the spatial-partial derivatives at the mask (2-D intensity transmittance function) coordinates (x_p,y_q). This leads to a parallel extraction of the spatial-partial derivatives.

2.2.1 Resolution Constraints

The spatial resolution of the modified system is equal to the separation between the detector elements. Figure 2-12 shows a part of the 2-D detector array where the

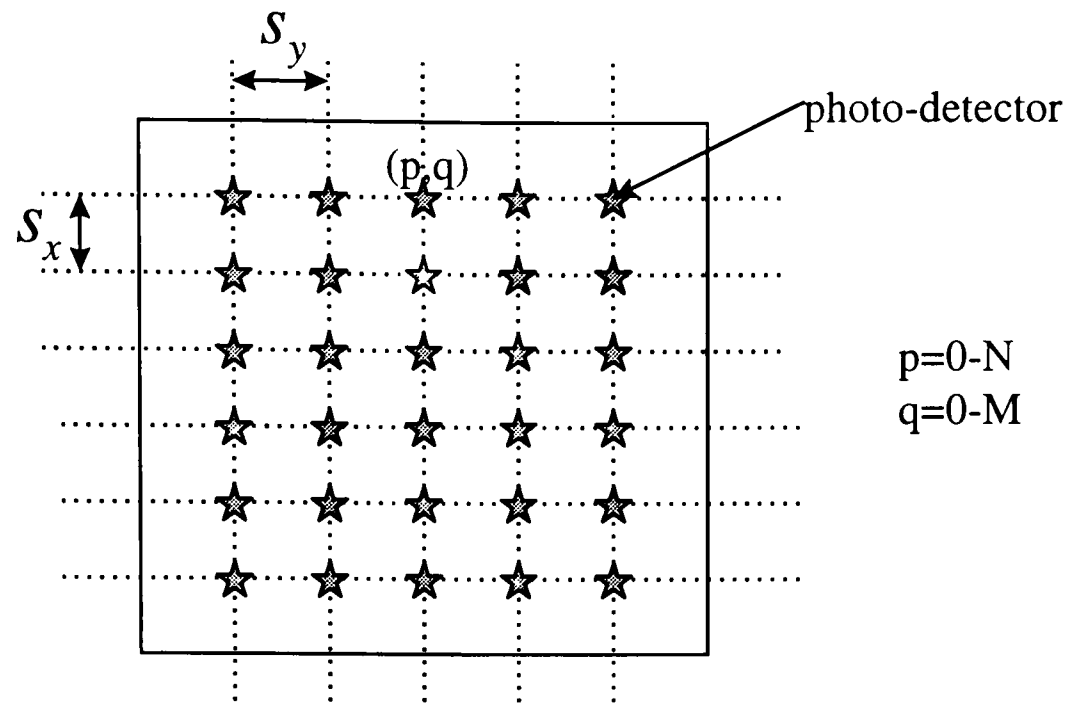


Figure 2-12. Symbolic Representation of the Heterodyne Detector Array

spacing between the detector elements is highlighted. Heuristic observation shows that the maximum spatial-resolution of the detector-array is

$$(\Delta_x)_{\max} = s_x$$
$$(\Delta_y)_{\max} = s_y. \tag{2-34}$$

The maximum perturbation amplitude should generally not exceed half the detector spacing, as this might result in cross-talk between adjacent detector elements. This condition can be expressed as:

$$A_x \le \frac{s_x}{2}; \text{ and}$$

$$A_x \le \frac{s_x}{2}. \tag{2-35}$$

VLSI constraints do not allow the size of the detector array (i.e., the number of detector elements) to be very large, which might lead to poor resolution. This problem

can be circumvented by projecting blocks of the mask onto the detector array, by an appropriate modification in the imaging system, with the tradeoff that it introduces some semblance of serial processing. This also gives us the flexibility to vary spatial resolution, within the limiting constraints specified in Equation (2-34).

The extraction of a particular spatial derivative from the photodetector current, involves mixing the photodetector current with the carrier frequency and subsequently low-pass filtering the signal. By designing a low-pass filter with a finite bandwidth, we can have the flexibility of projecting several frames of an image continuously, and thus extract the varying spatial derivatives at a point in the image. We will elaborate on this aspect when we present the design of the heterodyne detection circuitry in Chapter 4.

2.2.2 System Simulation

The verification of the results presented in Equation (2-33) was done by simulating the system in MATLAB™. We first used a 1-D spatial intensity function, a pulse with sigmoid edges. The use of a pulse with sigmoid edges, better emulates a real time situation.

2.2.2.1 1-D Simulation

The 1-D intensity function used is given below:

$$\tau(x) = \left\{ \frac{1}{1+\exp\left[-k(x+\frac{a}{2})\right]} - \frac{1}{1+\exp\left[-k(x-\frac{a}{2})\right]} \right\}, \qquad (2\text{-}36)$$

where 'k' controls the steepness of the edge, and a is the width of the edge. The above intensity function may be recognized as a pulse with exponential rise and fall, and width 'a'. The theoretically calculated derivative for the intensity function is given by:

$$\frac{\partial \tau}{\partial x} = \frac{k \exp\left[-k(x+\frac{a}{2})\right]}{\left\{1+\exp\left[-k(x+\frac{a}{2})\right]\right\}^2} - \frac{k \exp\left[-k(x-\frac{a}{2})\right]}{\left\{1+\exp\left[-k(x-\frac{a}{2})\right]\right\}^2}. \qquad (2\text{-}37)$$

The code for the simulation is listed in Appendix C. For simulation purposes, the pulse width, 'a' was selected as unity and 'k' was chosen to be '20'. The results of the simulation are given in Figure 2-13. The figure shows a plot of the intensity function and the normalized plots of the theoretical calculated first order derivative ($\partial\tau/\partial$x), and the normalized plot of the derivative obtained from the simulation. The theoretical and the simulation results are in close agreement, except for a DC offset for the region with constant intensity. This is probably due to the small offset in the derivative due to the error components specified in Equations (2-12).

2.2.2.2 2-D Simulation

We also tried to simulate the spatio-temporal heterodyne detector system for a 2-D intensity function, which is basically a (2×2) checker-board pattern. Again the edges are defined by exponentials. The intensity function is given by:

$$\tau(x, y) = \left\{\frac{1}{1+\exp[-k(x+1)]} - \frac{1}{1+\exp[-kx]}\right\}\left\{\frac{1}{1+\exp[-ky]} - \frac{1}{1+\exp[-k(y-1)]}\right\}$$

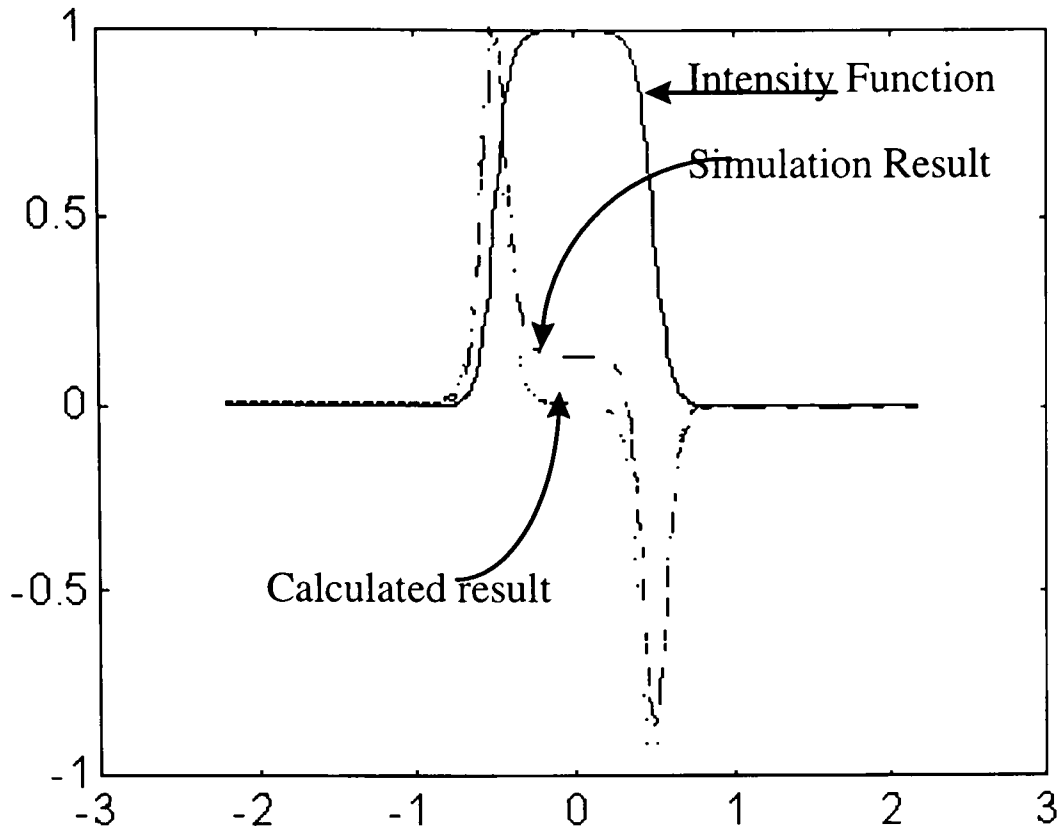


Figure 2-13. Distribution of $|\partial\tau(x)/\partial x|$

$$+\left\{\frac{1}{1+\exp[-kx]}-\frac{1}{1+\exp[-k(x-1)]}\right\}\left\{\frac{1}{1+\exp[-k(y+1)]}-\frac{1}{1+\exp[-ky]}\right\}. \qquad (2\text{-}38)$$

The code for the simulation is listed in Appendix C. The results of the simulation are presented in Figures 2-14, 2-15 and 2-16. Figure 2-14 gives the 2-D intensity function used for the simulation. Figure 2-15 gives the distribution of the derivative with respect to x, i.e., $\partial\tau(x,y)/\partial x$ with $\Omega_{ref}=\Omega_x$. Figure 2-16 is the distribution of derivative with respect to y, i.e., $\partial\tau(x,y)/\partial y$, with $\Omega_{ref}=\Omega_y$.

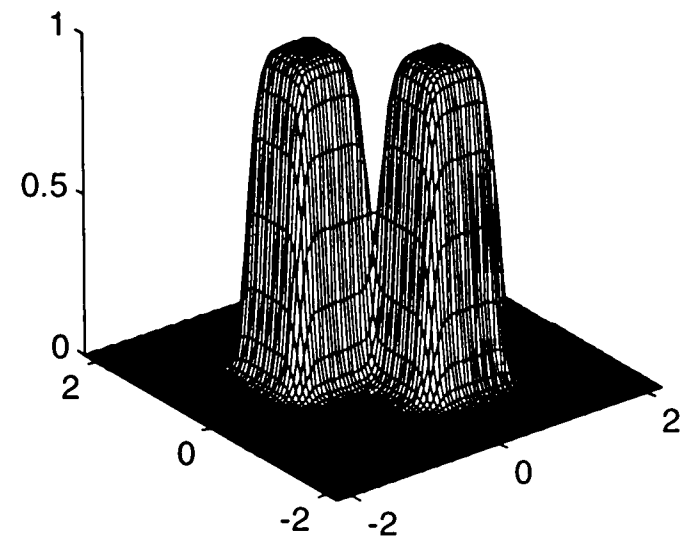


Figure 2-14. 2-D Spatial Intensity Function: "2×2 Checker-board"

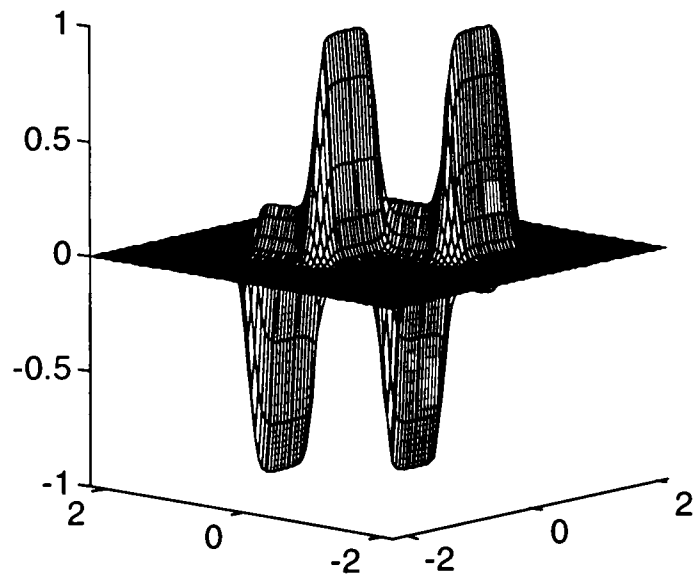


Figure 2-15. Distribution of $\partial\tau(x,y)/\partial x$

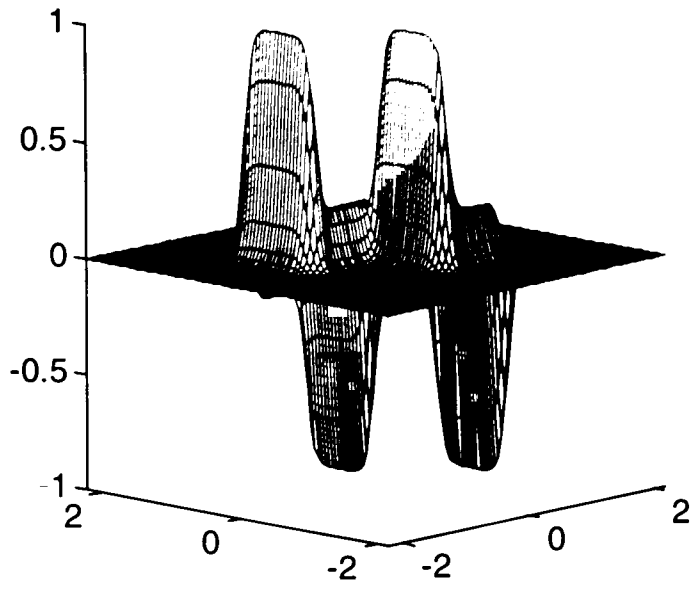


Figure 2-16. Distribution of $\partial\pi(x,y)/\partial y$

2.2.3 General Applications of the Heterodyne Detector Array

We conclude this Chapter by presenting a set of possible applications of the heterodyne detector array, using the imaging system described. The information is presented in a tabular fashion.

Table 2-1. Applications of 2-D Heterodyne Detector Array.

Desired Operation	**Parameters**
Directional Gradients: $\nabla_x t(x,y) \rightarrow$ $\nabla_y t(x,y) \rightarrow$	$x(t)=A_o\cos(\Omega_x t)$, $y(t)=A_o\cos(\Omega_y t)$, $\Omega_x \neq \Omega_y$ $V_{ref}(t) = \cos(\Omega_x t)$ $V_{ref}(t) = \cos(\Omega_y t)$
Laplacian Components: $\nabla_{xx} t(x,y) \rightarrow$ $\nabla_{yy} t(x,y) \rightarrow$	$x(t)=A_o\cos(\Omega_x t)$, $y(t)=A_o\cos(\Omega_y t)$, $\Omega_x \neq \Omega_y$ $V_{ref}(t) = \cos(2\Omega_x t)$ $V_{ref}(t) = \cos(2\Omega_y t)$
Arbitrary Derivatives: $(n,m) \geq 0$ (including fractional derivatives) $\nabla_{(mx)(ny)} t(x,y) \rightarrow$	$x(t)=A_o\cos(\Omega_x t)$, $y(t)=A_o\cos(\Omega_y t)$, $\Omega_x \neq \Omega_y$ $V_{ref}(t) = \cos[(m\Omega_x + n\Omega_y)t]$
Simple Image Acquisition: $t(x,y) \rightarrow$	$x(t) = y(t) = 0$ $V_{ref}(t) = 1$
Generalized linear filtering(tight spiral trajectory): $h(x,y) * t(x,y) \rightarrow$	$x(t)=a\sqrt{t}\cos(b\sqrt{t})$, $y(t)=a\sqrt{t}\sin(b\sqrt{t})$, $a \ll b$ $V_{ref}(t) = h[x(t),y(t)]$

CHAPTER 3

CIRCUIT DESIGN

The theoretical analysis of a 2-D spatial derivative extraction system using a heterodyne detector array, along with the system simulation results for 1-D and 2-D sample intensity function inputs, were discussed in Chapter 2. In this chapter, we first present the VLSI architecture of the 2-D heterodyne detector array. Then we present the detailed circuit level design of the individual blocks. We conclude the chapter by discussing some of the layout considerations for the individual circuit blocks. The layout diagrams of the different circuit blocks are also presented in this chapter.

3.1 VLSI Architecture of the Heterodyne Detector Array

One possible architecture for the heterodyne detector array is depicted in Figure 3-1. A heterodyne detector element essentially consists of a photodetector, an op-amp buffer, mixer and a low-pass filter. We first present a simple analysis of the working of a single heterodyne detector element. The photodetector signal, in general can be represented by

$$i_d^{(p,q)}(t) = a_o \cos(\Omega_o t) + a_1 \cos(\Omega_1 t) + a_2 \cos(\Omega_2 t) + \ldots, \tag{3-1}$$

where a_0, a_1, a_2 represent the low bandwidth derivative information, riding on carrier frequencies Ω_0, Ω_1 and Ω_2, respectively. If the op-amp buffer has a gain 'K(V/A)', the output of the buffer is given by:

$$V_o^{(p,q)}(t) = K\left[a_0 \cos(\Omega_0 t) + a_1 \cos(\Omega_1 t) + a_2 \cos(\Omega_2 t) + \ldots\right]. \tag{3-2}$$

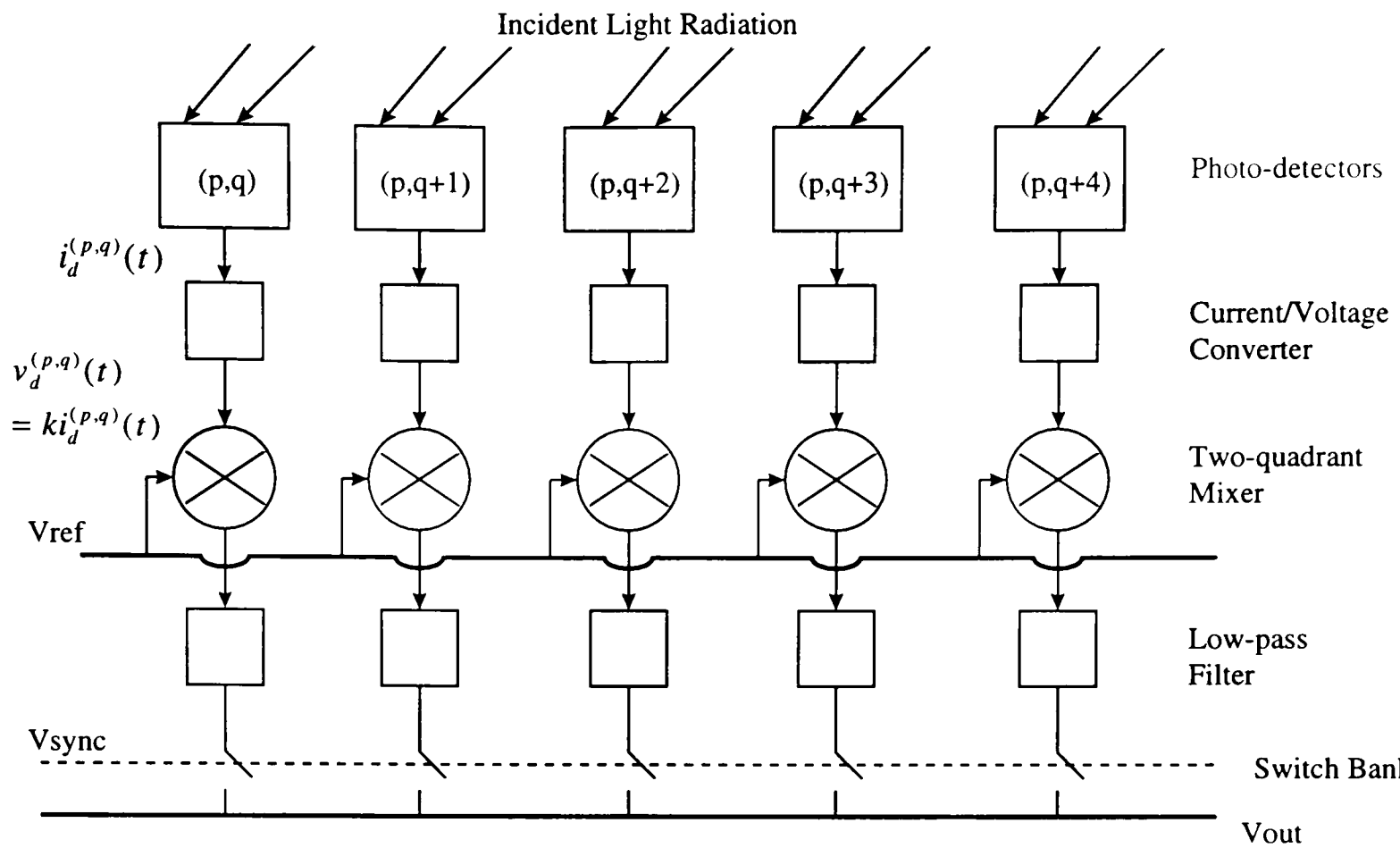


Figure 3-1. Block Diagram Representation of the Heterodyne Detector Array

To extract the derivative component corresponding to a_0, the reference frequency is selected as:

$$\Omega_{ref} = \Omega_0, \tag{3-3}$$

with

$$V_{ref}^{(p,q)} = (2/K)\cos(\Omega_0 t). \tag{3-4}$$

The output of the mixer can therefore be written as:

$$V_m^{(p,q)}(t) = \left[\frac{2}{K}\cos(\Omega_0 t)\right]\left\{K\left[a_0\cos(\Omega_0 t) + a_1\cos(\Omega_1 t) + a_2\cos(\Omega_2 t)\right]\right\}$$

$$
\begin{aligned}
&= 2a_0\cos(\Omega_0 t)\cos(\Omega_0 t) + 2a_1\cos(\Omega_0 t)\cos(\Omega_1 t) + 2a_2\cos(\Omega_0 t)\cos(\Omega_2 t) \\
&= \underline{a_0\left\{\cos\left[(\Omega_0+\Omega_0)t\right]+1\right\}} + a_1\left\{\cos\left[(\Omega_1+\Omega_0)t\right]+\cos\left[(\Omega_1-\Omega_0)t\right]\right\} \\
&+ a_2\left\{\cos\left[(\Omega_2+\Omega_0)t\right]+\cos\left[(\Omega_2-\Omega_0)t\right]\right\} \qquad (3\text{-}5) \\
&= a_0 + a_0\cos(2\Omega_0 t) + a_1\left\{\cos\left[(\Omega_1+\Omega_0)t\right]+\cos\left[(\Omega_1-\Omega_0)t\right]\right\} \\
&+ a_2\left\{\cos\left[(\Omega_2+\Omega_0)t\right]+\cos\left[(\Omega_2-\Omega_0)t\right]\right\}
\end{aligned}
$$

As is clear from Equation (3-4), the derivative component a_0, can be extracted by low-pass filtering the mixer output provided the cut-off frequency of the low-pass filter is greater than the bandwidth of a_0 and less than ($|\Omega_{ref} - \Omega_i|$), i = 1,2.

3.2 Op-amp Design

In this section we provide a detailed discussion of the design of a three stage op-amp. A general block diagram of a typical op-amp implementation is given in Figure 3-2. It typically consists of three blocks[15]:

1. Differential input pair: The input differential pair is ideally designed to provide a high input impedance, a large CMRR (Common Mode Rejection Ratio) and PSRR (Power Supply Rejection Ratio), a low offset voltage, low noise and high gain.
2. The second stage may perform one or more of the following functions:
   a. Level Shifting: This is needed to compensate for the dc voltage change occurring in the input stage, and thus to assure the appropriate dc bias for the following stages.
   b. Added Gain: In most cases the gain provided by the input stage is not sufficient, and additional amplification is required.

c. Differential to single-ended conversion: In some circuits, the input stage has a differential output, and the conversion to single-ended signals is done in a subsequent stage.

3. Output Buffer: It provides the low output impedance and larger output current needed to drive the load of the op-amp. It normally does not contribute to the voltage gain.

3.2.1 Performance Metrics

We list below some of the commonly used performance metrics[16,17,18] for an op-amp design before going into the detailed circuit design of the op-amp.

- DC gain is the low frequency gain of the amplifier and usually characterizes the accuracy of the amplifier.
- Unity gain bandwidth is the frequency at which the open-loop gain of the amplifier becomes unity or 0 dB.
- Phase margin is defined as the phase shift of the amplifier at the unity gain bandwidth.
- Slew rate is the rate of change of the output for a large input step signal.
- Settling time is the amount of time required by the amplifier to settle within a predetermined tolerance (typically 0.1 percent) of the final value of the output step response.
- Input common mode range is the range of input voltages over which the operational amplifier can still operate properly, i.e., all the input transistors are in the saturation region.

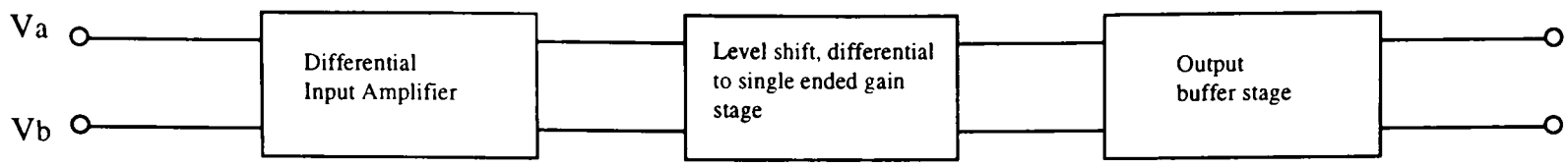


Figure 3-2. Block Diagram for a Practical Op-amp.

- Output voltage swing is the voltage range over which all the transistors in the output stage are biased in the saturation region.
- Power supply rejection ratio is defined as the ratio of the differential gain to the gain from the variation in the power supplies(ratio of the output voltage and the power supply small signal input), with the differential inputs set to zero.
- Common mode rejection ratio is defined as the ratio of the differential gain to the common mode gain.

3.2.2 Op-amp Design Specifications

The design specifications for the op-amp are given below:

Low frequency gain	$A_0 \geq 70$ dB,
Unity-gain frequency	$f_0 \geq 2$ MHz,
Slew rate	$S_r \geq 4$ V / μs,
Common-mode rejection ratio	CMRR ≥ 80 dB,
Phase margin	φM > 60°,
Load impedance	$C_L = 10$ pF,
dc supply voltages	$V_{DD} = -V_{SS} = 5$V.

The design specifications selected are quite general and suitable for a wide variety of applications, especially for buffering circuits and switched capacitor filter applications. Here, we will like to make a general comment on the slew rate specification. The maximum rate of change for a sinusoidal input voltage with amplitude A_o and frequency f_o is given by $\Omega_0 A_o$ ($\Omega_o=2\pi f_o$). .For the frequency range of interest in our design, a slew rate of 4V/μs is adequate. For a specific design application and frequency range of the heterodyne detection array, the op-amp design can still be tailored, to save some silicon area.

3.2.3 Op-amp Circuit Design

The circuit diagram of the op-amp is given in Figure 3-3. The compensation capacitance C_c is generally chosen to be equal to the load capacitance C_L; therefore,

$$C_c = C_L = 10pF\,. \tag{3-6}$$

For an adequate phase margin φM, the frequency of the second pole s_{p2} of the open loop gain should be sufficiently higher than ω_0, the unity-gain (angular) frequency. It can be shown that selecting $|s_{p2}| = 3\omega_0$ gives a phase margin greater than 60°. The value of s_{p2} can be found from the small-signal equivalent circuit of the op-amp of Figure 3-3, shown in Figure 3-4. Assuming C_A (parasitic capacitance at the output of the differential amplifier) $<< C_L = C_c$ and $g_{m6} >> g_{d7}$,

$$s_{p2} = \frac{-g_{m6}C_c}{C_A(C_L+C_c)+C_LC_c} \cong -\frac{g_{m6}}{C_L}\,. \tag{3-7}$$

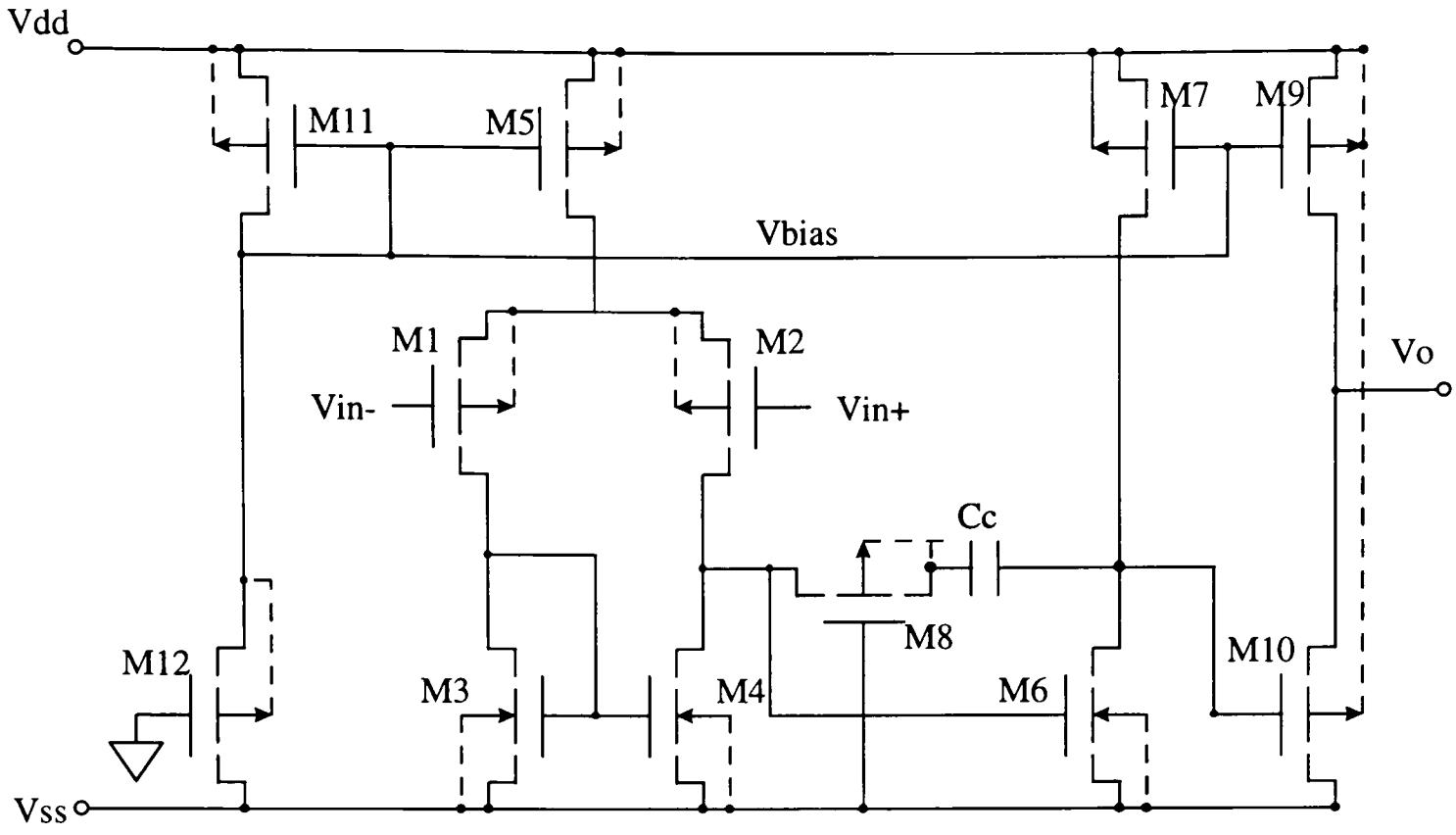


Figure 3-3. Op-amp Circuit Diagram

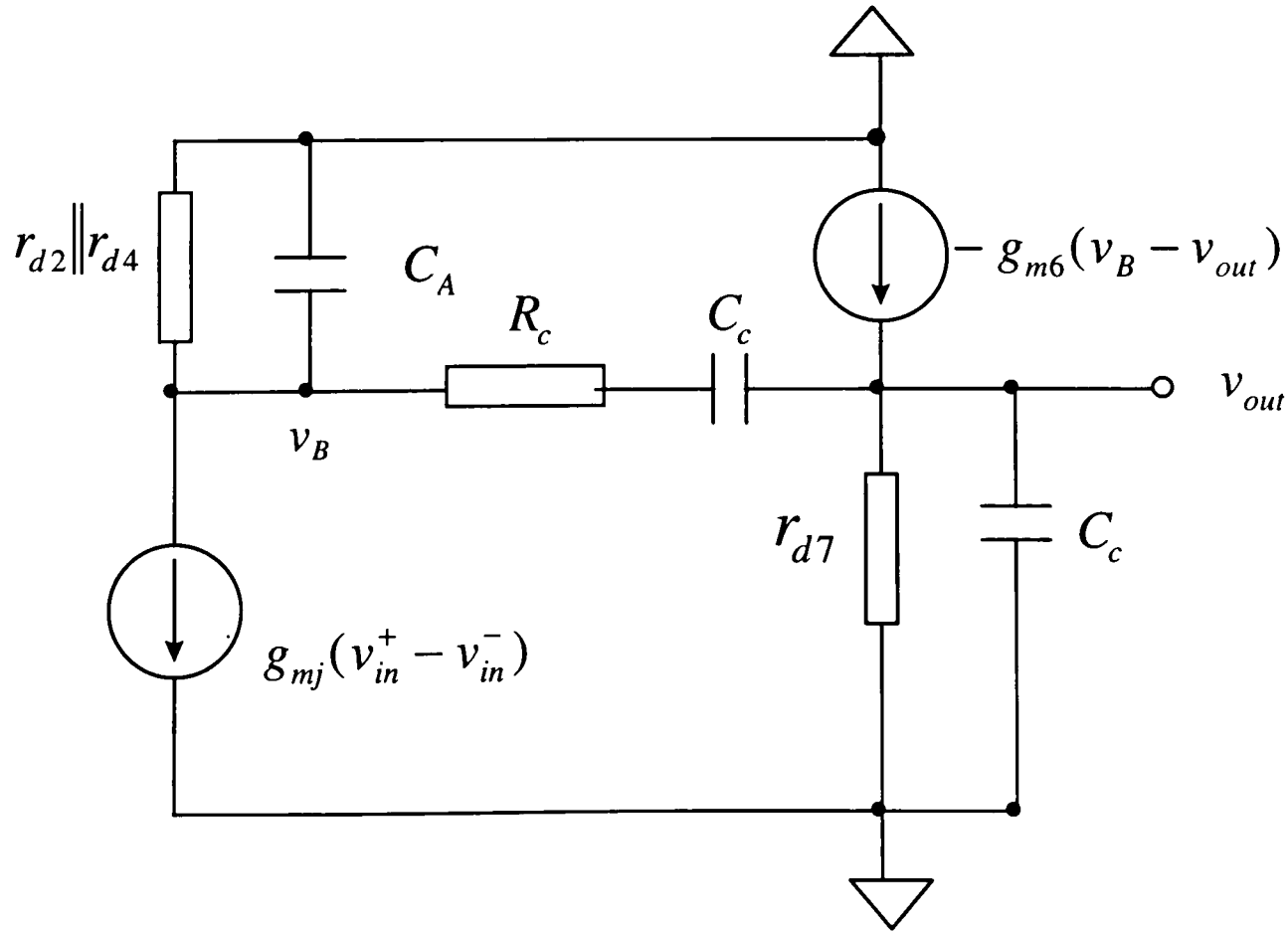


Figure 3-4. Small Signal Equivalent of the Op-amp
(excluding the output buffer stage)

Therefore

$$\left|s_{p2}\right| = \frac{g_{m6}}{C_L} = 3\omega_0 = 3\frac{g_{mi}}{C_c} \tag{3-8}$$

is the design equation. This gives

$$\begin{aligned} g_{m6} &= 3g_{mi} = 377\frac{\mu A}{V} \\ \therefore\ g_{mi} &= 125.7\frac{\mu A}{V}. \end{aligned} \tag{3-9}$$

The specified slew rate requires that the bias current of the input stage specify

$$I_0 = S_r C_c \geq 4\times 10^6 \times 10^{-11} = 40\mu A\,. \tag{3-10}$$

We can thus choose I_0 = 40 μA. The negative-going slew-rate limitation due to the use of M_7 as a current source can be expressed as:

$$S_{r0} \leq \frac{I_{bias}}{C_L}. \tag{3-11}$$

To make this effect small, we can set

$$S_{r0} = 2.5S_r = 10V/\mu s. \tag{3-12}$$

Then,

$$I_{bias} = C_L S_{r0} = 10^{-11}\times 10^7 = 100\mu A. \tag{3-13}$$

To avoid systematic offset voltage, the condition

$$\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{I_0/2}{I_{bias}} = \frac{1}{5} \tag{3-14}$$

must hold. The transconductance for the loads can be calculated as:

$$g_{m1} = g_{m3} = g_{m4} = \sqrt{\frac{(W/L)_3 \, I_0/2}{(W/L)_6 \, I_{bias}}} g_{m6} = \frac{I_0/2}{I_{bias}} g_{m6} = \frac{g_{m6}}{5} \cong 75.4\,\mu A/V\,. \qquad (3\text{-}15)$$

Next, the channel resistance R_c of M_8 is determined, so as to place the zero s_z of the op-amp transfer function at a convenient location. This can be easily determined from the small signal equivalent circuit given in Figure 3-4 and is given by:

$$s_z = \frac{-1}{(R_c - 1/g_{m6})C_c}, \qquad (3\text{-}16)$$

and hence the required resistance is related to the desired zero location s_z by the formula:

$$R_c = \frac{1}{|s_z|C_c} + \frac{1}{g_{m6}}. \qquad (3\text{-}17)$$

There exist two different strategies for choosing s_z. One possibility is to use $s_z = s_{p2}$; another is to shift s_z to infinity. For the second case, we have

$$R_c = \frac{1}{g_{m6}} \cong 2.65k\Omega\,. \qquad (3\text{-}18)$$

Note that M_8 is in the linear region since its gate is at V_{SS} and its drain-source potential is zero. The channel resistance R_c in the linear region is given by:

$$\frac{1}{R_c} = \left|\frac{\partial i_d}{\partial v_d}\right| = k_p \left(\frac{W}{L}\right)_8 \left|v_{gs8} - v_{Tp}\right|. \qquad (3\text{-}19)$$

Next, the design of the current sources M_5 and M_7 will be considered. The aspect ratios W/L of these transistors should not be too small, since for the given values of the currents I_0 and I_{bias}, the $(v_{gs}\text{-}v_T)$ drop across these transistors would be large, which would effectively reduce the input and output voltage swing (to a value such that M_5 and M_7 are always in saturation) and hence the dynamic range of the op-amp. Assuming an excess

gate to source voltage of 0.5, i.e., v_{gs}-v_T = 0.5, the aspect ratios for the transistors M_5 and M_7 can be calculated from the following relations:

$$\left(\frac{W}{L}\right)_5 = \frac{2I_0}{k_p\left(v_{gs5} - v_T\right)^2} \text{ and}$$

$$\left(\frac{W}{L}\right)_7 = \frac{2I_{bias}}{k_p\left(v_{gs7} - v_T\right)^2} . \tag{3-20}$$

The aspect ratios of transistors M_1-M_4 and M_6 can be calculated from their transconductances as given below:

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \frac{g_{mi}^2}{2K_p\left(I_0/2\right)} \tag{3-21}$$

and

$$\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \frac{g_{ml}^2}{2K_n\left(I_0/2\right)} . \tag{3-22}$$

From Equation (3-14), we have:

$$\left(\frac{W}{L}\right)_6 = 5\left(\frac{W}{L}\right)_3 . \tag{3-23}$$

The transistors M_5 and M_7 were dimensioned such that:

$$v_{gs5} = v_{gs7} = v_{Tp} - 0.5 , \tag{3-24}$$

therefore,

$$v_{bias} = V_{DD} + v_{gs5} . \tag{3-25}$$

The sizing of the biasing transistors M_{11} and M_{12} is rather trivial and can be done by assuming the transistors to be operating in the saturation mode and then equating their

drain currents. In determining the aspect ratios of the different transistors the process parameters of the Orbit 2.0μ N-well process were used. The Orbit 2.0μ N-well process is offered by the MOSIS foundry and is specifically optimized for analog design The process parameters for Pspice® (level 2 model) simulations are listed in Appendix B. The aspect ratios of the different transistors in the op-amp circuit of Figure 3-3 are given below in a tabular fashion:

Table 3-1. Transistor Aspect Ratios for the Op-amp.

$(W/L)_1$	216/10	$(W/L)_5$	175/10	$(W/L)_9$	685/5
$(W/L)_2$	216/10	$(W/L)_6$	105/10	$(W/L)_{10}$	984/5
$(W/L)_3$	21/10	$(W/L)_7$	437/10	$(W/L)_{11}$	90/10
$(W/L)_4$	21/10	$(W/L)_8$	389/10	$(W/L)_{12}$	25/100

3.3 Four-Quadrant Gilbert Cell Mixer/Multiplier

The design of the four quadrant multiplier was implemented as a basic Gilbert cell with active attenuators at the two differential inputs as proposed in ref[19]. The use of active attenuators enhances the dynamic range of the input signal and assures a linear response of the multiplier cell over the entire input range.

3.3.1 Principle of Operation

A block diagram of the multiplier is shown in Figure 3-5. Differential active attenuators used at the input to the Gilbert cell increase the dynamic range of the input

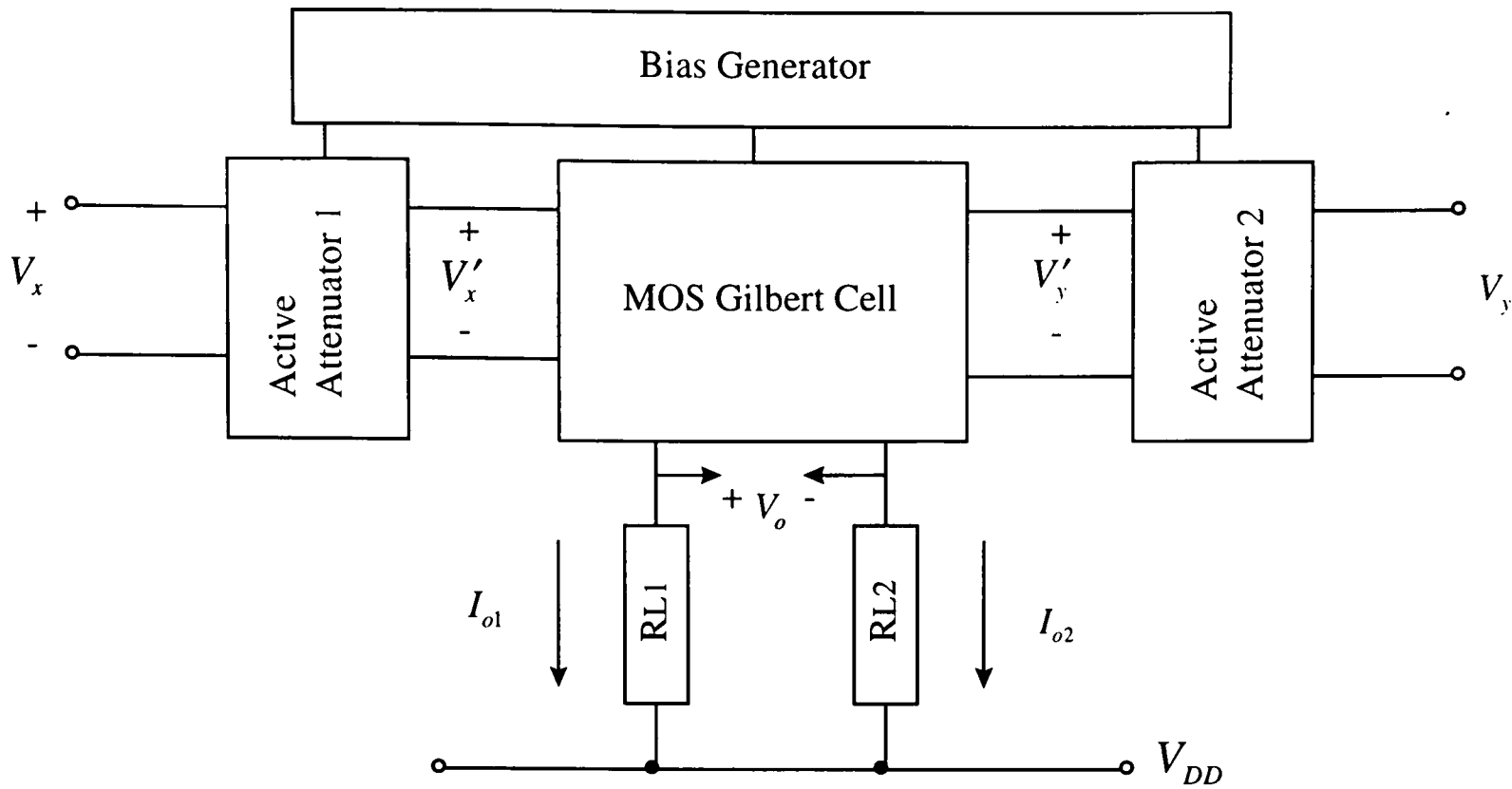


Figure 3-5. Block Diagram of CMOS Multiplier Cell

signal. The output of the multiplier is a differential output current. A differential output voltage can be obtained by two resistors referenced to V_{DD}. A brief description of each of the blocks is given below:

3.3.1.1 MOS Gilbert Cell

The MOS version of the Gilbert multiplier cell[19,20] is shown in Figure 3-6. We assume that all the transistors in Figure 3-6 are biased in the saturation region, and that they obey the ideal square law-equation, i.e.,

$$i_{ds} \propto \left(v_{gs} - v_T\right)^2. \tag{3-26}$$

Further the transistors are matched so that the transconductance parameters have the following relations:

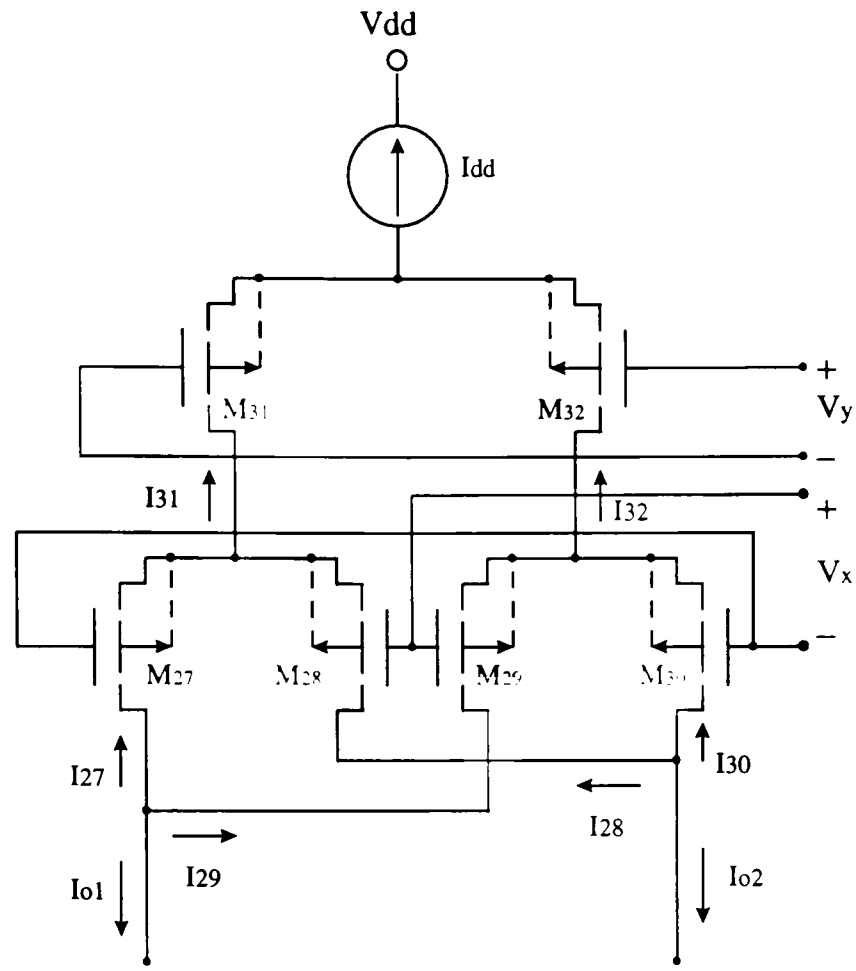


Figure 3-6. MOS version of Gilbert Cell

$$K_{27} = K_{28} = K_{29} = K_{30} = K_a \tag{3-27}$$

and

$$K_{31} = K_{32} = K_b . \tag{3-28}$$

Defining the output currents $I_{o1} = -(I_{27} + I_{29})$ and $I_{o2} = -(I_{28} + I_{30})$, it can be easily shown that the output differential current $I_{od} = I_{o1} - I_{o2}$ is given by:

$$I_{od} = \sqrt{2K_a}V_{x'}\left[\sqrt{I_{31}}\sqrt{1-\frac{K_a V_{x'}^2}{2I_{31}}} - \sqrt{I_{32}}\sqrt{1-\frac{K_a V_{x'}^2}{2I_{32}}}\right]. \tag{3-29}$$

If

$$\frac{K_a V_{x'}^2}{2I_{31}} \langle\langle 1 \tag{3-30 a}$$

and

$$\frac{K_a V_{x'}^2}{2I_{32}} \langle\langle 1, \tag{3-30 b}$$

it follows that I_{od} depends linearly on $V_{x'}$ and is given by the expression:

$$I_{od} \cong \sqrt{2K_a}\left(\sqrt{I_{31}} - \sqrt{I_{32}}\right)V_{x'}. \tag{3-31}$$

It can also be shown that I_{31} and I_{32} are dependent on the voltage $V_{y'}$ as indicated by the expression:

$$V_{y'} = \frac{1}{\sqrt{K_b}}\left(\sqrt{I_{31}} - \sqrt{I_{32}}\right). \tag{3-32}$$

Substituting Equation(3-32) into Equation(3-31), it follows that

$$I_{od} = \sqrt{2K_a K_b}V_{x'}V_{y'}. \tag{3-33}$$

This is the characteristic of an ideal analog multiplier. Practically, since I_{31} and I_{32}, both depend on $V_{y'}$ and I_{dd}, both $V_{x'}$ and $V_{y'}$ should be kept small to maintain good linearity. Therefore adding attenuators to the two input signals helps to increase the dynamic range of the input signals and maintains good linearity of the multiplier over the whole input range.

3.3.1.2 Active Attenuator

A simple active attenuator[21] is shown in Figure 3-7(a). The transistor M_1 is assumed to be operating in the ohmic region and M_2 is assumed to be operating in the saturation region. The output voltage of the active attenuator is given by the expression:

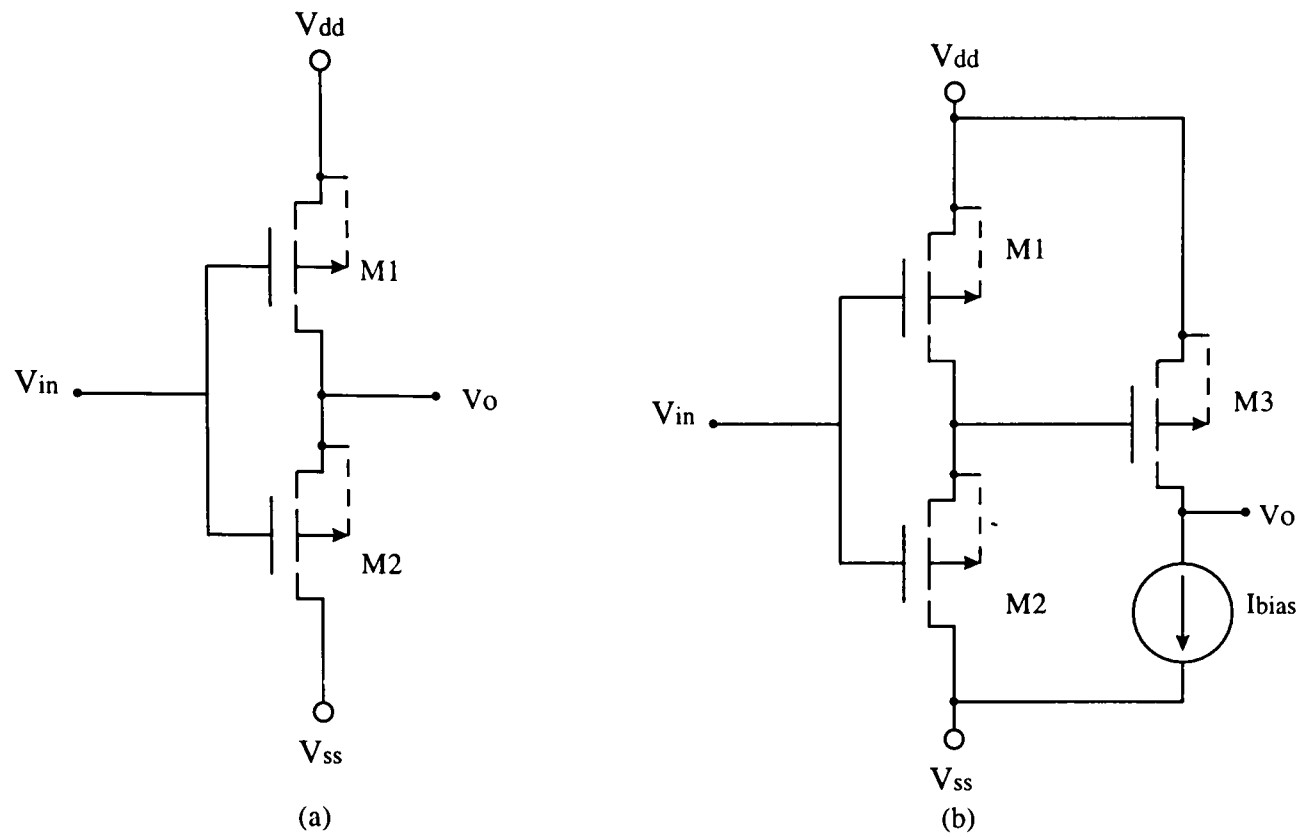


Figure 3-7. Input Attenuator: (a) Active Attenuator[21] and (b) Attenuator with Level Shifter

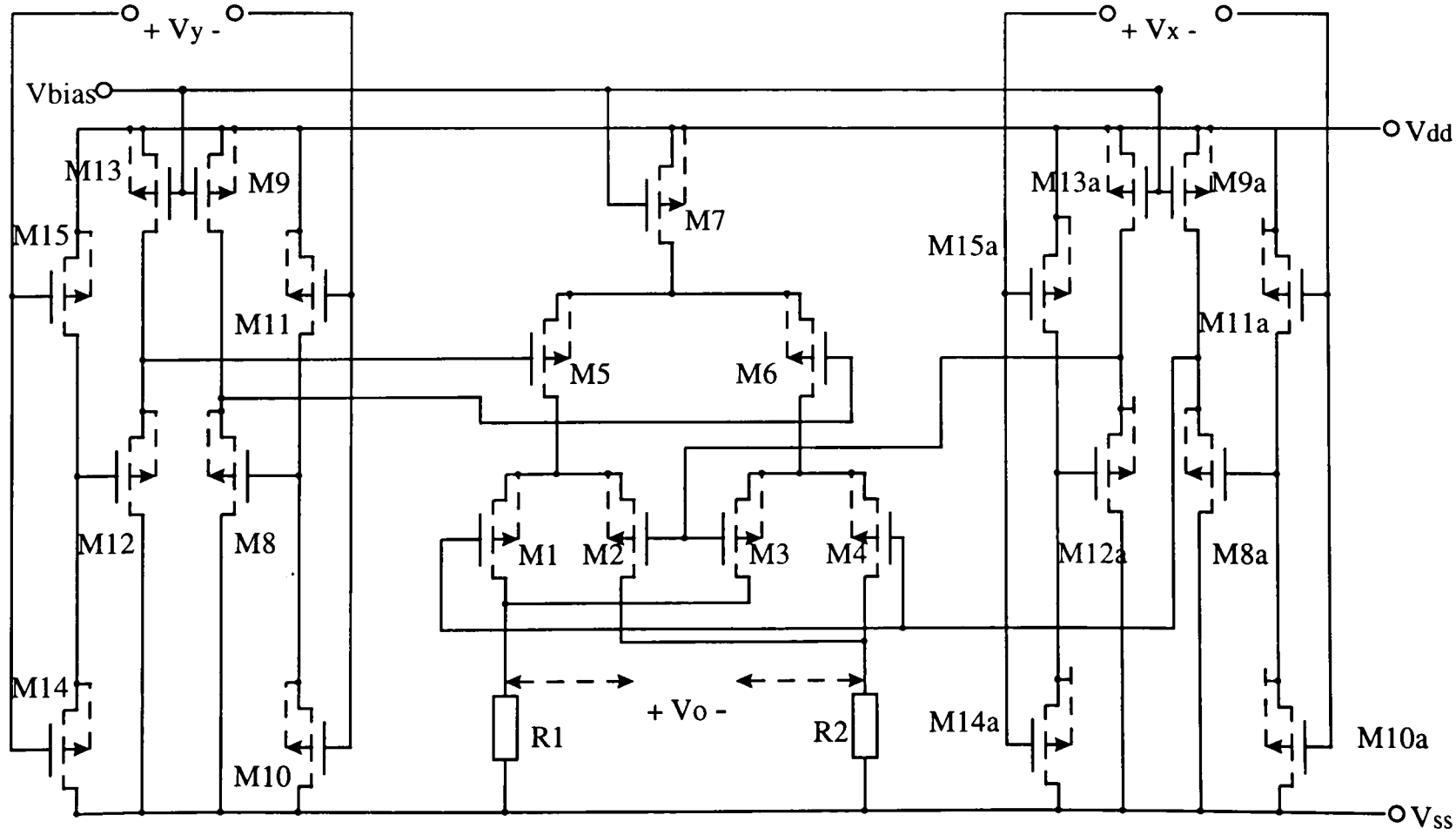


Figure 3-8. Circuit Diagram of the Multiplier Cell

$$V_o = \left[1 - \sqrt{\frac{W_1 L_2}{W_1 L_2 + W_2 L_1}}\right]\left(V_i - V_{DD} - V_T\right) + V_{DD}\,. \tag{3-34}$$

Hence, the gain of the attenuator is roughly given by:

$$m = 1 - \sqrt{\frac{W_1 L_2}{W_1 L_2 + W_2 L_1}}\,. \tag{3-35}$$

For biasing purposes, a level shift is generally needed when coupling the attenuator into the Gilbert cell. A simple source follower can be used for this purpose as shown in Figure 3-7(b).

3.3.1.3 Multiplier Cell

If m_1 and m_2 represent the gains of the active attenuator1 and active attenuator 2, respectively, of Figure 3-6, then using Equation (3-33), the overall transfer characteristics of the CMOS multiplier can be approximated by:

$$I_{od} = I_{o1} - I_{o2} \cong \left[\sqrt{2K_a K_b}\right] V_x V_y m_1 m_2\,. \tag{3-36}$$

If a pair of resistors $R_{L1} = R_{L2} = R_L$ are used to convert a differential output current into a differential output voltage, the output voltage is given by the expression:

$$V_o = R_L I_{od} = \left[\sqrt{2K_a K_b}\right] V_x V_y m_1 m_2 R_L\,. \tag{3-37}$$

The overall circuit diagram of the multiplier is given in Figure 3-8.

3.4 Switched Capacitor Filter

We start our discussion on the switched capacitor filter design, by listing some of the advantages of switched capacitor filters, followed by an introduction to the basic

concepts of switched capacitor circuits, and then we will talk about the stray-insensitive Fleischer-Laker biquads,[22] used to implement our switched capacitor filter design.

Advantages of Switched Capacitor Filters over Active RC Filters:

1. Area savings[15]: Consider filters in the voice band(0~4KHz). Such filters require time constants of the order of 10 krad/s. Even assuming a fairly large capacitor, say 10pF, this requires a resistance around 10 MΩ. Such a resistor would occupy an area of about 1600 mil^2 ~ 10^6 μm^2, which is inordinately large. Such a resistor can be implemented with a switched capacitor. For a sampling frequency of 100 KHz , a 1pF capacitor can realize a resistance of 100 MΩ, and it occupies an area of about 4 mil^2, which is a considerable saving.
2. Accuracy and stability[15]: Typically resistors implemented as diffusion or polysilicon tend to be non-linear. A relative accuracy better than 10% is hard to achieve, even though the tracking error between two resistors can be kept as low as 1~2%. Since capacitors are made in different fabrication steps than resistors, their errors do not track with those of the resistors on the same chip. The errors of the capacitors are of the same order as the resistors, i.e., about 10% individual error and 1% tracking error; hence, the error of any RC time constant can be as large as 20%. Such errors can seldom be tolerated even in low -selectivity filters. Furthermore, the temperature and voltage coefficients of capacitors and resistors are not correlated; hence, the time constants will also vary somewhat with temperature and signal level. By switched capacitor implementations of resistors an RC time constant is reduced to the ratio of two capacitances (as discussed later), $(C_1/C_2)T$, where T is the time-period of the

sampling clock. Since the clock can be generated with high accuracy, and the tracking error between two capacitors on the same chip can be kept as low as 1%, time constants accurate to within 1% can be realized using switched capacitor filters as against 20% in active RC implementations.

3. Bandwidth programmability: A switched capacitor filter has an interesting property of tuning the bandwidth by changing the clock frequency within certain bounds. This is easier to visualize from the filter transfer function, Consider, for example a general second order filter transfer function, which can be represented by

$$H(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{b_0 + b_1 z^{-1} + b_2 z^{-2}}. \tag{3-38}$$

Substituting $z = e^{j\varpi T}$ in Equation(3-38), and re-arranging the terms we get

$$H\left(e^{j\omega T}\right) = \frac{a_0 e^{j2\omega T} + a_1 e^{j\omega T} + a_2}{b_0 e^{j2\omega T} + b_1 e^{j\omega T} + b_2}, \tag{3-39}$$

where 'T' is the sampling period. It can be noted from Equation(3-38), that the dc gain of the transfer function is fixed at $[(a_o+a_1+a_2)/ (b_o+b_1+b_2)]$. It can be easily proved that for two different sampling periods, T_1 and T_2 the 3-dB frequencies $\omega_{1\text{-}3dB}$ and $\omega_{2\text{-}3dB}$ are related by the simple relation:

$$\omega_{1-3dB} T_1 = \omega_{2-3dB} T_2 \tag{3-40}$$

The above relation depicts the tunable bandwidth property of the switched capacitor filter.

3.4.1 Switched Capacitor Resistor

Two possible realizations of switched capacitor resistor implementations are shown in Figure 3-9. Figure 3-9(a) gives a shunt realization and Figure 3-9(b) gives a series realization. The clock wave-forms are shown in Figure 3-9(c). Consider the shunt realization first. Whenever $V_{\varphi 1}$ equals v_c , M_1 is in full conduction since v_c is normally high (5~10V). Hence, during this interval, M_1 provides a low resistance between its drain and source. Whenever $V_{\varphi 1}$ is zero, M_1 acts as an open circuit. Similar conditions hold for $V_{\varphi 2}$ and M_2. Since the clock phases of $V_{\varphi 1}$ and $V_{\varphi 2}$ are non-overlapping, M_1 and M_2 are never turned on simultaneously. It is assumed that v_1 and v_2 are slowly varying signals so that during a clock interval T (Figure 3-9 c), they do not change appreciably. This will be the case if the highest frequency components in v_1 and v_2 are much smaller than the clock frequency $f_c = 1/T$. Typically f_c is 50~100 times the maximum signal frequency. An analysis on the acceptable ratio of the clock frequency f_c to the signal frequency will be given later.

Consider the situation when $V_{\varphi 1}$ is high, now M_1 is conducting and connects the input v_1 to the capacitor through a low drain resistance. Capacitor C is previously charged to v_2 during the phase when $V_{\varphi 2}$ was high. The capacitor C charges to v_1, and the net charge flowing during $V_{\varphi 1}$ can therefore be written as:

$$\Delta q_1 = C\left(v_1 - v_2\right). \tag{3-41}$$

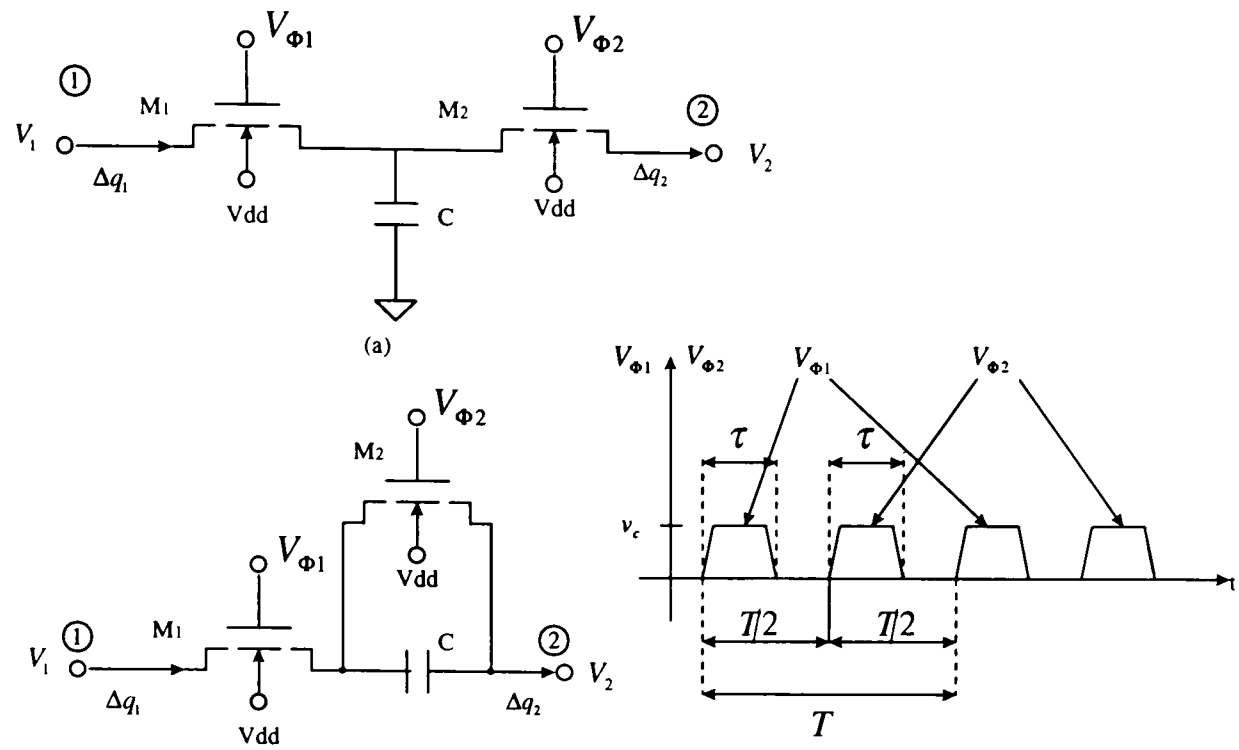


Figure 3-9. Switched Capacitor Resistor Realization : (a) Parallel Realization (b) Series Realization and (c) Clock Wave-forms

Next, $V_{\varphi 1} \rightarrow 0$, M_1 cuts off, and the capacitor C holds its voltage at v_1. When $V_{\varphi 2} \rightarrow v_c$, M_2 conducts and C discharges to v_2. The net charge flowing during $V_{\varphi 2}$, can thus be written as:

$$\Delta q_2 = C(v_1 - v_2) = \Delta q_1 . \tag{3-42}$$

Since, during each clock interval T, a charge $C(v_1 - v_2)$ enters at node '1' and leaves at node '2', we can define the average current flowing from node '1' to node '2' as:

$$i \triangleq \frac{\Delta q_1}{T} = \frac{C}{T}(v_1 - v_2), \tag{3-43 a}$$

or

$$i = \left(\frac{1}{R}\right)(v_1 - v_2); \tag{3-43 b}$$

where, R is defined as:

$$R = \frac{T}{C} = \frac{1}{f_c C}. \tag{3-44}$$

A similar approximate analysis can be performed for the series configuration shown in Figure 3-9(b). Here, when $V_{\varphi 2} = v_c$, M_2 is 'on' and discharges the capacitance C. When $V_{\varphi 1} \rightarrow v_c$, C charges to a potential v_1-v_2, so the effective charge flowing from node '1' to node '2' during the clock interval T is again equal to $C(v_1$-$v_2)$. Therefore, following the analysis given in Equations (3-42) - (3-44), the effective resistance in this case is also given by:

$$R = \frac{T}{C} = \frac{1}{f_c C}. \tag{3-45}$$

3.4.2 Switched Capacitor Integrator

In this section, we analyze the transfer functions of an ideal active RC integrator and a switched capacitor integrator. The goal is to figure out the ratio of the sampling frequency to the maximum signal frequency, so that the switched capacitor integrator implements the same transfer function as the ideal active RC integrator. Figures 3-10(a) and 3-10(b) give the circuit diagrams of the active RC and the switched capacitor integrators and Figure 3-10(c) gives the clock waveforms.

For the active RC integrator of Figure 3-10(a), assuming ideal components, the circuit equations are:

$$v = 0, i = 0 \tag{3-46}$$

and

$$i_1 = \frac{v_{in}}{R_1} = i_2 = -C_2 \frac{dv_o}{dt}. \tag{3-47}$$

Hence, the output-input relation is

$$v_o(t) = -\frac{1}{R_1 C_2} \int_{-\infty}^{t} v_{in}(\tau) d\tau . \tag{3-48}$$

Using Laplace transform and assuming zero initial conditions(i.e., $v_{c2} = v_{in} = 0$, for $t = 0$-), the relations

$$V_o(s_a) = \frac{-V_{in}(s_a)}{s_a R_1 C_2}$$

and

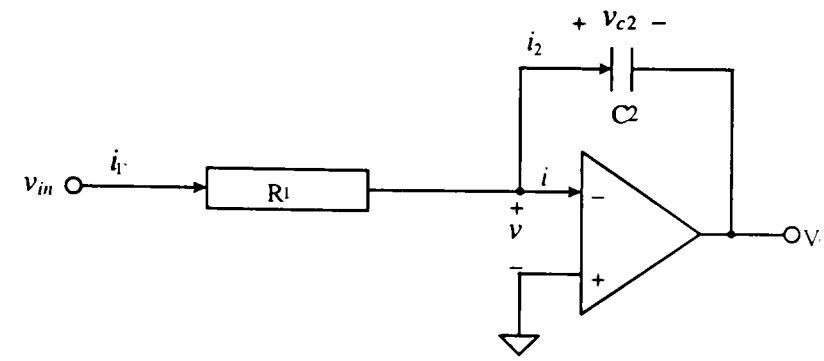
$$H_a(s_a) = \frac{V_o(s_a)}{V_{in}(s_a)} = -\frac{1/R_1 C_2}{s_a} \tag{3-49}$$

result. Here s_a is the analog Laplace-transform variable. A switched capacitor equivalent of this integrator is shown in Figure 3-10(b). When Φ_1 rises to '1' at the time instant $t = t_n - \tau$, M_1 turns on and C_1(which was earlier discharged) recharges to v_{in}. At $t = t_n$, M_1 shuts off and C_1, having acquired a charge

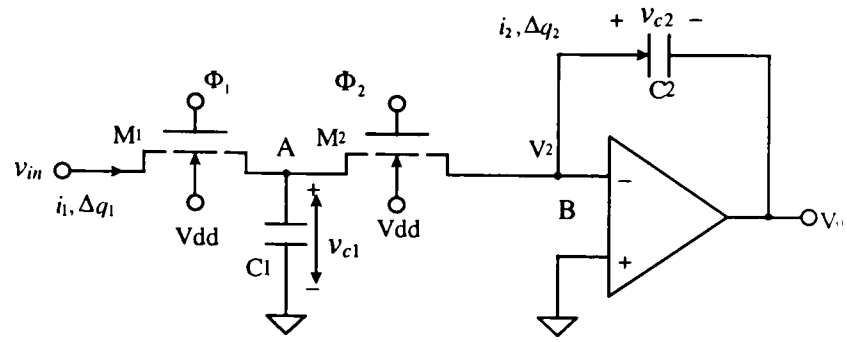
$$\Delta q_1(t_n) = C_1 v_{in}(t_n) \tag{3-50}$$

is isolated. At $t = t_n + T/2 - \tau$, Φ_2 rises to '1' and M_2 turns on. Thus, C_1 is connected between the virtual ground at the inverting input of the op-amp and true ground and hence it discharges. Thus, a charge

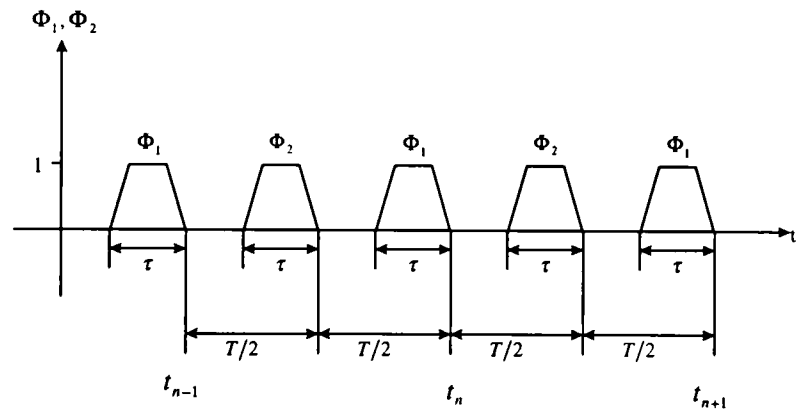
$$\Delta q_2(t_n + T/2 - \tau) = C_1 v_{in}(t_n) \tag{3-51}$$



(a)



(b)



(c)

Figure 3-10. Op-amp Integrator: (a) Active RC Integrator
(b) Switched Capacitor Integrator; (c) Clock Signals

flows through M_2 and into C_2. As a result, the charge stored in C_2 increases by Δq_2, and the voltage v_{c2} across it changes by

$$\Delta v_{c2}(t_n + T/2 - \tau) = \left(C_1/C_2\right) v_{in}(t_n). \tag{3-52}$$

From the above analysis, a difference can be established between the samples of $v_{in}(t)$ and $v_o(t)$ taken at t_{n-1}, t_n, t_{n+1} and so on. Thus, we can write

$$v_o(t_{n+1}) - v_o(t_n) = -v_{c2}(t_{n+1}) + v_{c2}(t_n)$$

$$= -\Delta v_{c2}(t_n + T/2 - \tau) = -\left(C_1/C_2\right)v_{in}(t_n). \tag{3-53}$$

Solving Equation(3-53), using z-transformation, we get

$$V_o(z)(z-1) = -\left(C_1/C_2\right)V_{in}(z) \tag{3-54}$$

and

$$H(z) \triangleq \frac{V_o(z)}{V_{in}(z)} = -\frac{C_1/C_2}{z-1} = -\frac{C_1}{C_2}\frac{z^{-1}}{1-z^{-1}}. \tag{3-55}$$

For $s_a = j\omega_a$, the transfer function of the active RC integrator(Equation 3-49) is given by:

$$H_a\left(j\omega_a\right) = \frac{-1/\left(R_1C_2\right)}{j\omega_a} \tag{3-56}$$

while, for $z = \exp(j\omega T)$, the transfer function for the switched capacitor integrator(Equation 3-55) becomes

$$H\left(e^{j\omega T}\right) = -\frac{C_1/C_2}{e^{j\omega T}-1}. \tag{3-57}$$

For $\omega T < 1$, we can use the Taylor-series approximation

$$e^{j\omega T} = 1 + j\omega T - (\omega T)^2/2 + \ldots \tag{3-58}$$

so that

$$H\left(e^{j\omega T}\right) = \frac{-C_1/\left(C_2T\right)}{j\omega - \omega^2T/2 - + \ldots}. \tag{3-59}$$

We note that $H_a(j\omega_a)$ is a pure imaginary function, whereas $H(e^{j\omega T})$ is not. Also, $H(e^{j\omega T})$ is a periodic function of ω, while $H_a(j\omega_a)$ is not. These two functions can be made

approximately equal only in a limited frequency range. Specifically, if $\omega T << 1$, and $C_1 = T/R_1$, Equation (3-59) gives

$$H\left(e^{j\omega T}\right) \approx \frac{-1/\left(R_1 C_2\right)}{j\omega} \tag{3-60}$$

which is the same as Equation (3-56). We conclude that for signal frequencies satisfying

$$\omega \langle \frac{1}{100T} = \frac{f_c}{100} \tag{3-61}$$

the switched capacitor integrator approximates the active RC integrator.

3.4.3 Stray Insensitive Integrator[15]

The switched-capacitor integrator of Figure 3-10(b) is sensitive to the effects of the stray capacitances between the various nodes and the ground. Consider, for example, node 'A' in Figure 3-10(b). This node is connected to the source/drain diffusions of M_1 and M_2, which have appreciable capacitance to the substrate; also, the leads connecting the top plate to M_1 and M_2 have some capacitance to the bulk. The resulting stray capacitance C_A is in parallel with the capacitance C_1 and therefore represents an error in its value. To have an accuracy of 1%, C_1 has to be made significantly large as the stray capacitance can be of the order of 0.05pF. Thus, a large area is needed on the chip, to swamp the stray capacitance.

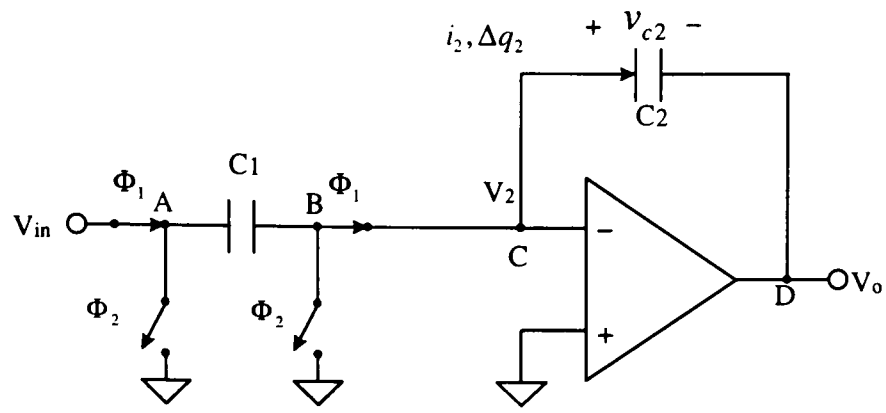


Figure 3-11. Stray Insensitive Integrator

Stray capacitances connected to low impedance sources or to virtual ground (node B) do not effect the operation of the integrator. To eliminate the harmful effects of the stray capacitances the stray-insensitive integrator[15] of Figure 3-11 is used. In this circuit, the stray capacitance C_A between node 'A' and ground is periodically charged from the input source which provides v_{in}, and then discharged to ground. The parasitic capacitance 'C_B' at node 'B' is grounded at both terminals as is 'C_C'. Finally, 'C_D' is driven by the the low-output impedance of the op-amp, and is hence rendered harmless. In conclusion, none of the stray capacitances to ground influence the operation of the circuit.

3.4.4 The Fleischer-Laker Biquad[22]

We designed the low-pass filter (a second-order Butterworth filter) as a switched capacitor filter using the Fleischer-Laker topology, which is shown in Figure 3-12. This topology can realize any biquadratic switched capacitor transfer function. We will first discuss the general Fleischer-Laker biquad, and then we will discuss our implementation.

As is clear from Figure 3-12, the Fleischer-Laker topology uses only two types of switched capacitors. The capacitors C_g, C_h, C_i and C_j provide the feedforward input, whereas C_e and the switched capacitor C_f provide the damping for the two integrator loop. The switched capacitor(SC) circuit has two transfer functions when

$$V_{io} = V_{ie} z^{-1/2}, \tag{3-62}$$

where V_{io} is the odd-phase input and V_{ie} is the even-phase input, with both the op-amp outputs held over a clock period. This is because of the manner in which the switched capacitors are connected. Note that the capacitors, C_a, C_c, C_f, C_g, C_h and C_i perform charge transfer in the even phase only, whereas in the odd-phase, the integrators hold their charge and hence the outputs are held over a clock period. Here Φ_1 corresponds to the even phase and Φ_2 corresponds to the odd phase. Thus, the two outputs V_o and V_o' at two different nodes are considered and the corresponding transfer functions T and T' are given by:

$$T(z) = \frac{V_o(z)}{V_i(z)} = \frac{C_d C_i + \left(C_a C_g - C_d C_i - C_d C_j\right) z^{-1} + \left(C_d C_j - C_a C_h\right) z^{-2}}{C_d (C_f + C_b) + \left[C_a \left(C_c + C_e\right) - C_d C_f - 2 C_d C_b\right] z^{-1} + \left(C_d C_b - C_a C_e\right) z^{-2}}$$

and

$$T'(z) = \frac{V_o'(z)}{V_i(z)} = \frac{\left[C_i \left(C_c + C_e\right) - C_g \left(C_f + C_b\right)\right] + \left[C_h \left(C_f + C_b\right) + C_b C_g - C_j C_c - C_e \left(C_i + C_j\right)\right] z^{-1} + \left(C_e C_j - C_b C_h\right) z^{-2}}{C_d (C_f + C_b) + \left[C_a \left(C_c + C_e\right) - C_d C_f - 2 C_d C_b\right] z^{-1} + \left(C_d C_b - C_a C_e\right) z^{-2}} \tag{3-63}$$

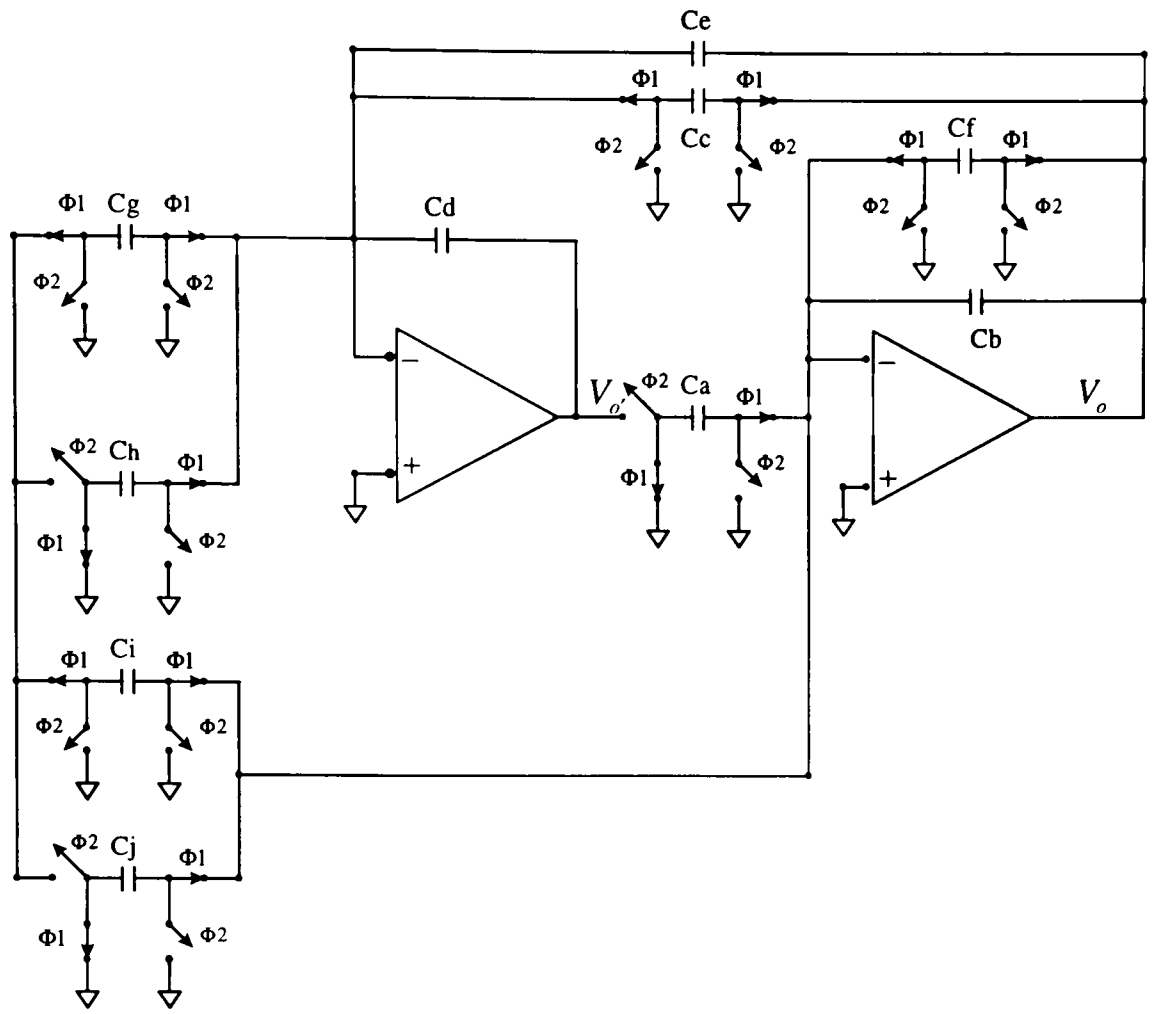


Figure 3-12. Fleischer-Laker Switched Capacitor Biquad

It is thus seen that T and T' realize biquadratic transfer functions. The desired transfer function can be matched with either T or T' to yield the capacitor ratios. The advantage of the Fleischer-Laker biquad is that the transfer functions contain product terms of order 2 (Equation 3-63), and since the outputs are held over a clock period, it is easy to cascade subsequent stages.

3.4.4.1 Filter Specifications

The filter design parameters depend on the particular application for which the 2-D heterodyne detector array is to be used. We designed the heterodyne detection array for

use in acquisition of the spatial derivatives of 2-D masks (intensity transmittance functions). A detailed description of the system has been provided in Chapter 2. For this case, the filter design parameters depend basically on the perturbation frequencies of the mirror (refer to Figure 2-9). With the mirror rotating system we had, the upper limit on the perturbation frequencies we could use was of the order of 1kHz. So we designed the filter assuming f_x and f_y, the x and y perturbation frequencies to be 1kHz and 1.333kHz. The table given below gives the carrier frequencies for up to the second order derivative components (in the photodetector output current), a possible set of reference frequencies which could be fed to the mixer (which precedes the filter) to extract the specific derivative information and a possible set of frequencies to be expected in the mixer output. The mixer output frequencies are of most interest in figuring out the design parameters for the low-pass filter.

Since we are using a low-pass filter to extract the derivative information in our design, it is obvious from the data in Table 3-1 that the dc component of the mixer output carries the derivative information. While designing the low-pass filter, we did not make its pass band extremely narrow around DC, but allowed for a *finite bandwidth* of the filter (approximately 100 Hz) around DC.

3.4.4.2 Finite Bandwidth of the Low-pass filter

Ideally, following the analysis given in Equations 3-1 through 3-5, the derivative information is basically a DC value, which can be extracted by a low-pass filter with a very narrow bandwidth at the origin, but we decided to have a finite bandwidth low-pass

Table 3-2. Analysis of the Mixer O/P Frequencies

Vref→		$\partial\tau/\partial x$ 1000 Mixer o/p		$\partial\tau/\partial y$ 1333 Mixer o/p		$\partial^2\tau/\partial x\partial y$ 333 Mixer o/p		$\partial^2\tau/\partial x\partial y$ 2333 Mixer o/p		$\partial^2\tau/\partial x^2$ 2000 Mixer o/p		$\partial^2\tau/\partial y^2$ 2666 Mixer o/p	
Derivatives		sum	diff.	Sum	diff.	sum	diff.	sum	diff.	sum	diff.	sum	diff.
f_x 1000	$\partial\tau/\partial x$	2000	0	2333	333	1333	667	3333	1333	3000	1000	3666	1666
f_y 1333	$\partial\tau/\partial y$	2333	333	2666	0	1666	1000	3666	1000	3333	667	3999	1333
f_y-f_x 333	$\partial^2\tau/\partial x\partial y$	1333	667	1666	1000	666	0	2666	2000	2333	1667	2999	2333
f_y+f_x 2333	$\partial^2\tau/\partial x\partial y$	3333	1333	3666	1000	2666	2000	4666	0	4333	333	4999	333
$2f_x$ 2000	$\partial^2\tau/\partial x^2$	3000	1000	3333	667	2333	1667	4333	333	4000	0	4666	666
$2f_y$ 2666	$\partial^2\tau/\partial y^2$	3666	1666	3999	1333	2999	2333	4999	333	4666	666	5332	0

filter to be able to process frames of information (i.e., a time varying input image), which can now be input to the system. Thus the derivative information, at a point on the mask, corresponding to a particular detector element, now has a finite bandwidth, which is approximately equal to the frame rate (this is a very optimistic value, since the bandwidth will also depend upon the variations in the derivative value at the same point in consecutive frames of information). Thus allowing for a finite bandwidth low-pass filter, the 2-D spatial derivative extraction system has the ability to process frames of information in real-time applications.

Based on the analysis of the mixer output frequencies, we came upon the following specifications for the low-pass filter:

Pass-band: 0 - 100Hz

Stop band: 100-5kHz

Pass-band ripple: 0.1dB

Stop-band attenuation: 35dB

Sampling frequency(f_c): 10kHz

Order: 2

The filter transfer function(z-domain) which implements the above specifications is given below:

$$H(z) = \frac{1.5794e-3+(3.1588e-3)z^{-1}+(1.5794e-3)z^{-2}}{1-1.8845z^{-1}+(8.908e-1)z^{-2}}. \quad (3\text{-}64)$$

The magnitude response of $H(z)$ is shown in Figures 3-13(a) and 3-13(b).

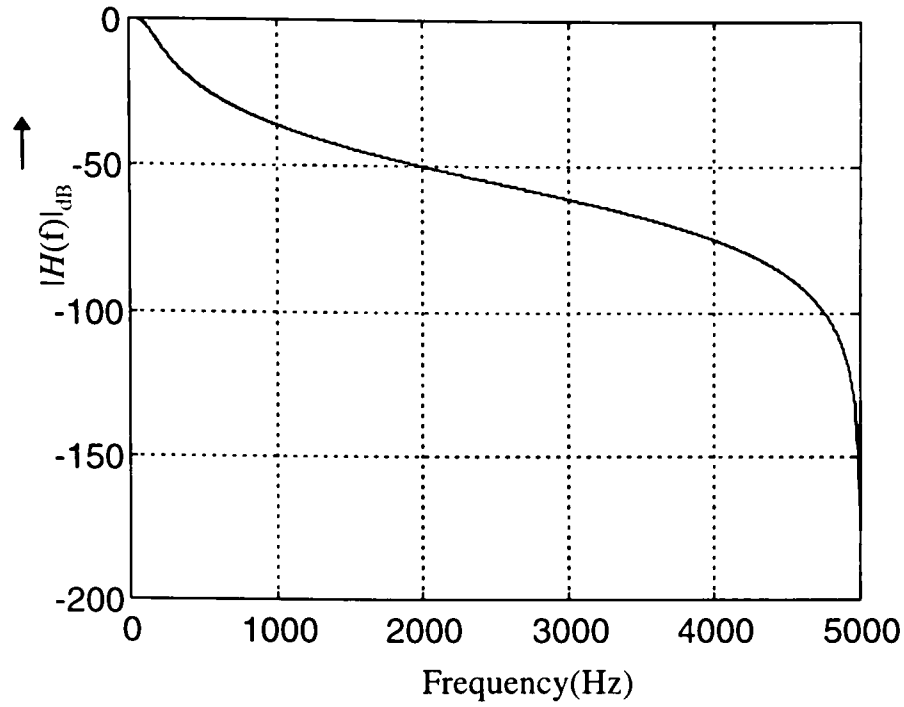
3.4.4.3 Design Procedure and Implementation

The transfer function $H(z)$ was implemented as $T(z)$,as given in Equation(3-63). As is clear from Equation(3-63), either C_e or C_f in the denominator of $T(z)$ can be used to implement $H(z)$. We selected C_f =0, and implemented, what is called the "E-circuit". Also, we selected $C_a = C_b = C_d$ =1, to simplify the design procedure.

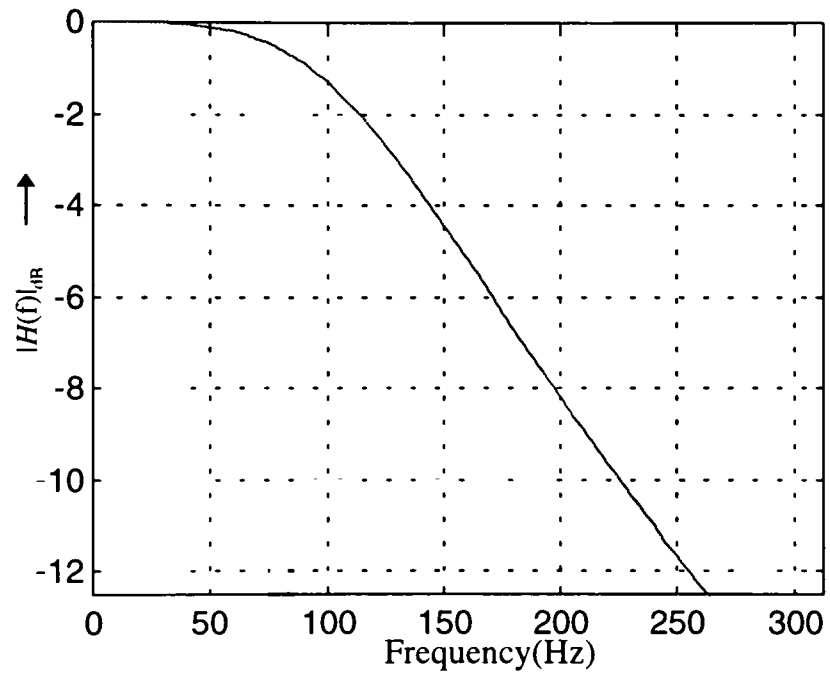
Substituting C_f =0, and $C_a = C_b = C_d$ =1 in Equation(3-63), we obtain:

$$T(z) = \frac{V_o(z)}{V_i(z)} = \frac{C_i+\left(C_g-C_i-C_j\right)z^{-1}+\left(C_j-C_h\right)z^{-2}}{1+\left(C_c+C_e-2\right)z^{-1}+\left(1-C_e\right)z^{-2}}. \quad (3\text{-}65)$$

The values of C_e, C_g, C_h, C_i, C_j and C_c can now be determined by comparing $H(z)$ in Equation(3-64) with $T(z)$ in Equation(3-65). The next step is to compute the maxima of



(a)



(b)

Figure 3-13: SC Filter Transfer Function $H(z)$: (a) Magnitude response of $H(z)$ for the complete frequency range and (b) Magnified Magnitude response of $H(z)$

$T(z)$ and $T'(z)$. While the desired transfer function ($T(z)$ in this case) has a known maximum value, the other transfer function (i.e., $T'(z)$ in this case) can have an altogether different maximum value. In a good design, when the input frequency is swept throughout the frequency range of interest, the active devices in the filter will saturate for

the same input level. This ensures that the SC filter has an optimal dynamic range. To achieve this, the maxima of T and T' are equalized and the capacitors are scaled such that:

$$\mu T'_{\max} = T_{\max}$$

and

$$(C_a, C_d) \rightarrow \left(\frac{C_a}{\mu}, \frac{C_d}{\mu}\right). \tag{3-66}$$

The next step is to consider groups of capacitances which are connected to the virtual ground inputs of the op-amps together, and scale them so that the smallest capacitance in the group is the unit capacitance. For the E-circuit we have selected, these groups would be:

$$Group - I: C_g, C_h, C_d, C_c, C_e$$

$$Group - II: C_a, C_i, C_j, C_b.$$

The final capacitance values obtained by following the above procedure are given below:

$$C_a = 3.67pF \qquad C_g = 0.1pF$$
$$C_b = 63.3pF \qquad C_d = 0.92pF$$
$$C_i = 0.1pF \qquad C_c = 0.1pF\,.$$
$$C_j = 0.1pF \qquad C_e = 1.725pF\,.$$

The SC filter circuit diagram, as obtained directly from the Fleischer-Laker topology (Figure 3-12) is given in Figure 3-14(a). It can be observed from this figure that there are certain capacitors which are switched between the same nodes during the same clock phases. These capacitors can be switched together, using a common switch. Figure

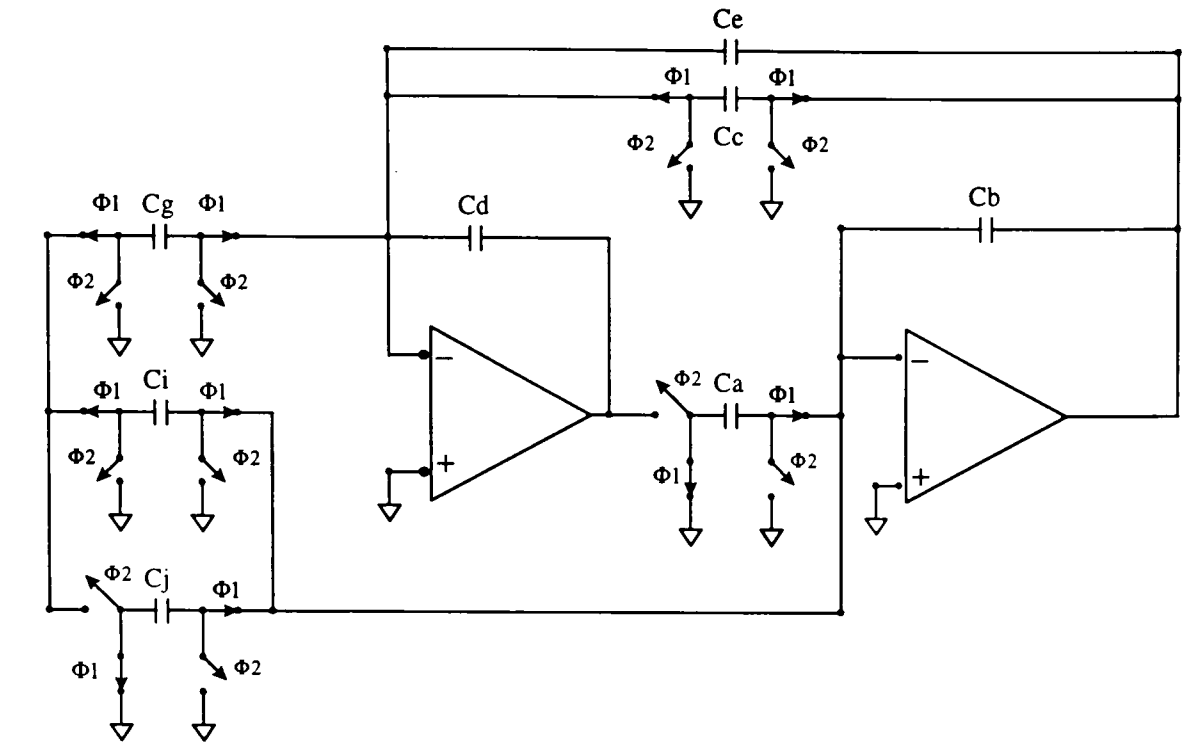
3-14(b) depicts the SC filter circuit with the reduced number of switches. The switch count in this case is seven as against ten in the original topology.

3.4.4.4 MOS Implementation of Switches

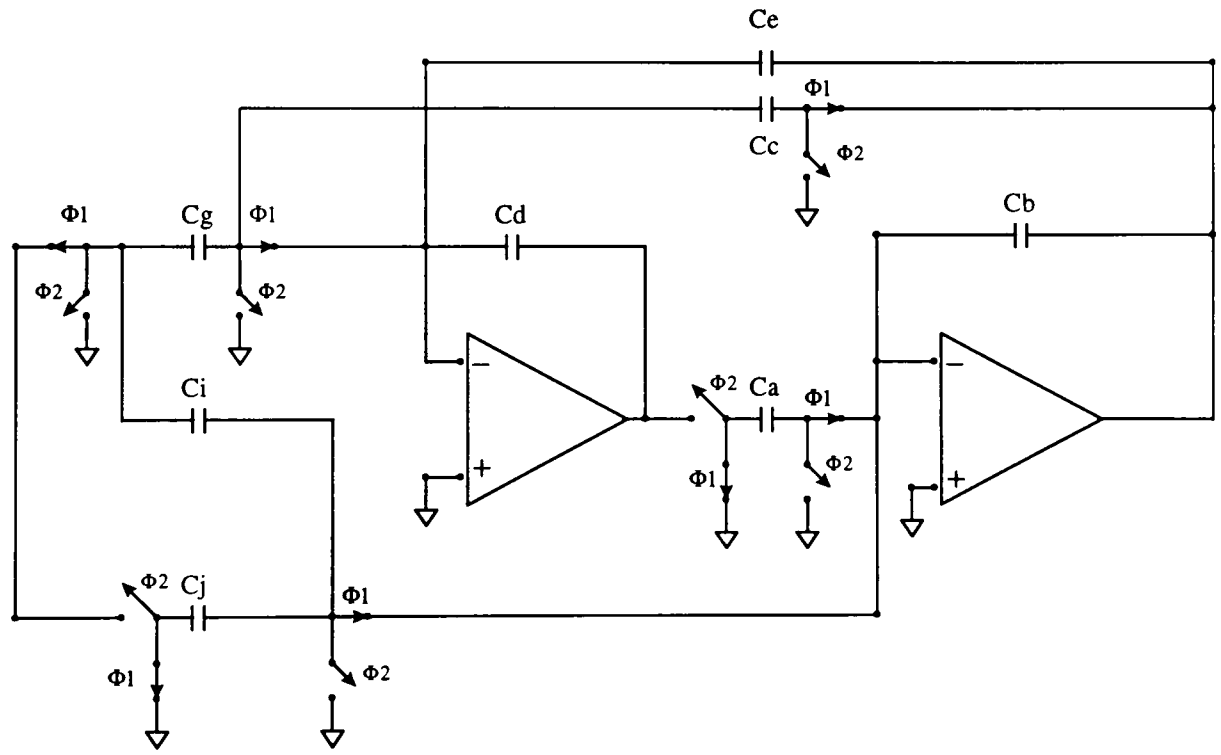
Having talked about the design of the low-pass SC filter, we will digress a little bit from the filter design, and discuss the MOS implementation of the switches. This is a crucial design aspect in the practical design of the SC filter, as there are problems like clock feed-through from the parasitic gate-drain/source capacitances, which effect the performance of the SC filter. Also, the 'on' resistance of the MOS transistor is finite, and therefore there is a finite time constant associated with the MOS drain resistance and the switched capacitance. This time constant should have a certain relation with the sampling clock time period for the successful implementation of the SC filter. In this section we will address these issues and we will also present our implementation of the MOS switch. A simple SC integrator circuit is used to discuss these problems.

First, we will look into the effects of the finite 'on' resistance of the MOS device. If, we neglect the parasitic capacitances of the MOS transistor, then it can be represented by an ideal switch in series with the 'on' resistance of the MOS transistor. The SC integrator of Figure 3-10(b), with the equivalent model for the MOS transistor(Figure 3-15(a)) is shown in Figure 3-15(b). In the ideal case when $R_1 = R_2 = 0$, the transfer function is given by:

$$H(z) = \frac{V_o(z)}{V_{in}(z)} = \frac{-C_1/C_2}{z-1}. \tag{3-67}$$



(a)



(b)

Figure 3-14. SC Filter Realization: (a) SC Filter obtained from Fleischer-Laker topology and (b) SC Filter with switch minimization

Assuming that the switch resistances R_1 and R_2 are linear and that no clipping takes place, at the end of the clock period Φ_1(Figure 3-15(c)), when $t = nt$, the voltage across C_1 is given by:

$$v_1(nT) = v_{in}(nT)\left(1 - e^{-T/2R_1C_1}\right). \tag{3-68}$$

Here, it was assumed that C_1 was fully discharged at $t = (n - ½)T$, and that switches S_1 and S_2 are both closed for periods of length $T/2$, where $T = 1/f_c$ is the sampling period.

Next, during the time when Φ_2 is high $[nT < t < (n + ½)T]$, C_1 discharges into C_2. The charge delivered is

$$\delta q\left(nT + T/2\right) = C_1 v_1(nT)\left(1 - e^{-T/2R_2C_1}\right). \tag{3-69}$$

Also,

$$v_o(nT + T) - v_o(nT) = \frac{\delta q\left(nT + T/2\right)}{C_2}. \tag{3-70}$$

Using z-transformation, and for $R_1 = R_2 = R$, we obtain

$$H'(z) = \frac{-\left(1 - e^{-T/2RC_1}\right)^2 C_1/C_2}{z - 1}. \tag{3-71}$$

On comparison with the ideal transfer function H(z) given in Equation(3-67), we observe that the finite 'on' resistance reduces the effective value of the capacitance ratio C_1/C_2. The relative error is

$$\varepsilon = 1 - \left(1 - e^{-T/2RC_1}\right)^2 \cong 2e^{-T/2RC_1}. \tag{3-72}$$

If ε is much less than the achievable tolerance (typically 0.1%) of C_1/C_2, then this effect will not be noticeable. Typically, we may require, say

$$\varepsilon \cong 2e^{-T/2RC_1} \leq 10^{-4} \tag{3-73}$$

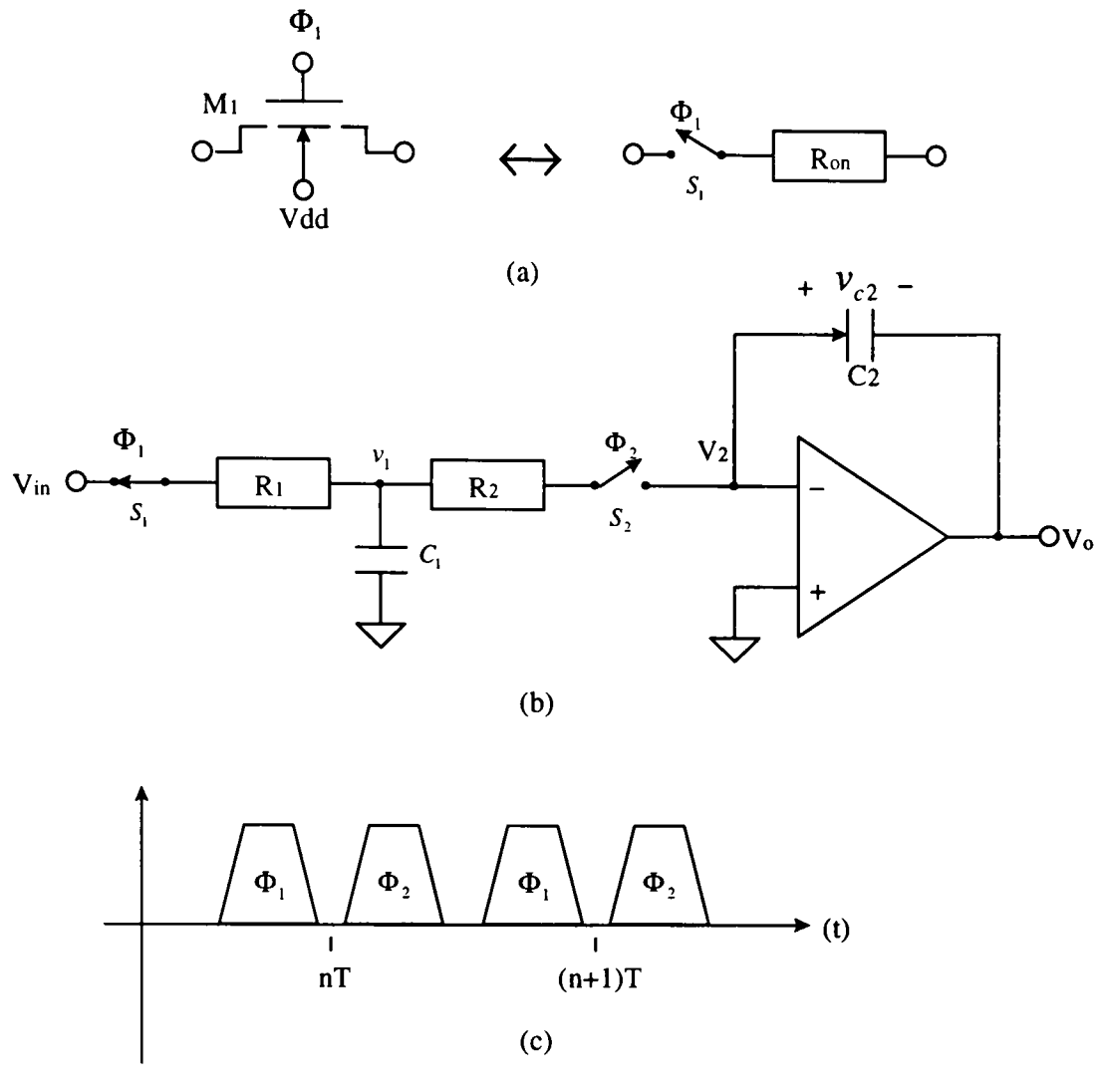


Figure 3-15. Effect of MOS Drain Resistance on SC Integrator Transfer Function: (a) Equivalent of MOS Pass Transistor and (b) SC Integrator and (c) Clock Wave-forms

so that

$$\frac{RC_1}{T} = RC_1 f_c \le \frac{1}{2\ln(20000)} = \frac{1}{20}, \tag{3-74}$$

i.e.,

$$RC_1 \le \frac{T}{20}. \tag{3-75}$$

Now, we address the problem of clock feedthrough. Figure 3-16(a) shows the SC integrator of Figure 3-15(b), with the parasitic capacitances of the MOS transistor included. The parasitic capacitances C_{g1}, C_{g2}, C_{g3} and C_{g4} shown in Figure 3-16(a) are the

MOS gate-source and the gate-drain capacitances. Each of these capacitances contains a voltage-independent (linear) component C_{ov} due to the overlap of the gate electrode and the source or drain diffusion, and a voltage-dependent(non-linear) component C_{ch} due to the gate-to-channel capacitance.

When Φ_1 is high and hence M_1 is conducting but M_2 is off, C_1 is connected to v_{in}, and the stray capacitances do not play any role. However, as Φ_1 goes low and Φ_2 rises, a complicated transient involving the strays occurs. The top plate of C_{g4} acquires a positive charge $C_{g4}V_{\Phi 2}$ from the clock Φ_2. This requires a matching charge - $C_{g4}V_{\Phi 2}$ at the bottom plate, which must come from C_2. Similarly, C_{g3} draws a current from C_1. As $V_{\Phi 2}$ rises, M_2 forms a channel and now C_{g3} also draws some of its charge from C_2. If the net positive charge delivered to both strays by Φ_2 is δq, then v_o changes by $-\delta q/C_2$. In addition, as M_1 cuts off, C_{g2} must recharge from C_2. These effects cause an error due to the strays.

Further, at the end of the half-period, during which Φ_2 is high, $V_{\Phi 2}$ falls. Now, C_{g3} and C_{g4} discharge and v_o is rising. At one point, when $V_{\Phi 2}$ falls below the threshold voltage V_{Tn}, M_2 cuts off and isolates C_1. As $V_{\Phi 2}$ falls further, C_{g3} discharges only through C_1 and not through C_2. Hence, the total charge restored to C_2, will be less than that removed from C_2 when Φ_2 was falling, and due to this there will be a net change in v_o due to clock feedthrough in every clock cycle. Thus, in the absence of a dc feedback, after a number of such cycles the amplifier would saturate. There are a number of ways to reduce the problem due to clock feedthrough. We will just talk about the switch design to compensate for clock feedthrough. For other techniques, the reader is referred to ref[15].

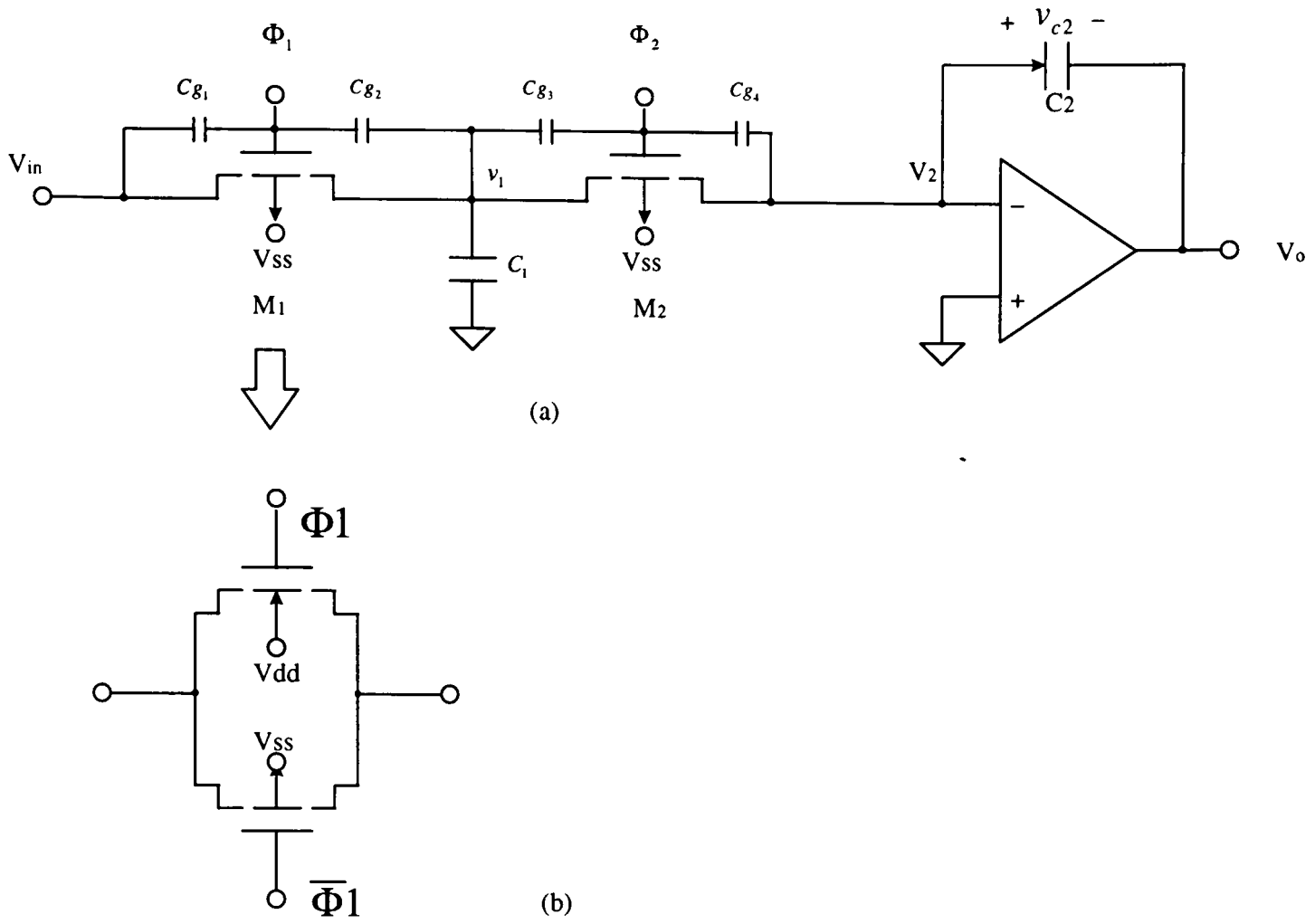


Figure 3-16. Offset Error Due to MOS Parasitic Capacitances: (a) SC Integrator highlighting the Parasitic MOS Capacitances and (b) Transmission Gate Switch

Clock feedthrough can be cancelled to some extent by using a transmission gate switch(Figure 3-16(b)). A transmission gate switch is essentially consists of a P-MOS and an N-MOS connected in parallel. The transmission gate switch requires that complementary clock phases be fed to the gates of the P-MOS and the N-MOS transistors. Therefore, if the *W/L* values of the P-MOS and the N-MOS transistors in the transmission gate structure are equal(since for this case the fixed component of the gate-drain/source parasitic capacitances is the equal for P-MOS and N-MOS), the effect of clock feedthrough due to the coupling of Φ_1 is complemented by a negative clock

feedthrough due to the coupling of $\overline{\Phi}_1$. To achieve better cancellation using this method, the clock waveforms used should be trapezoidal.

3.5 VLSI Layout Guidelines

In this section, we will discuss some of the VLSI layout considerations for different circuit blocks, principally, capacitors and MOS transistors, with emphasis on techniques which ensure better matching of components, e.g., the input transistor pair of the differential amplifier stage of the op-amp. For the novice reader, we provide a summary description of the different layers in a typical VLSI process and illustrate the sequence of making a MOS transistor in Appendix A of the thesis.

3.5.1 CMOS Transistor Layout[23]

For analog applications, the aspect ratios (*W/L*) of transistors are fairly high; therefore it is necessary to design wide structures. In this case, it is important to realize that the diffusion, which is used to implement the MOS source/drain region, has a non-negligible specific resistance(~100Ω/). A few squares may result in an unacceptable drain resistance. Figure 3-17(a) shows an example of a poor transistor layout and its equivalent circuit is shown in Figure 3-17(b). A better layout strategy is given in Figure 3-17(c). A point to be noted in this layout is that increasing the number of source/drain contacts lowers the source/drain resistance.

When the aspect ratio of the transistor is very large, the resulting layout becomes unmanageable. In this case, it is a good idea to split a wide transistor into a parallel

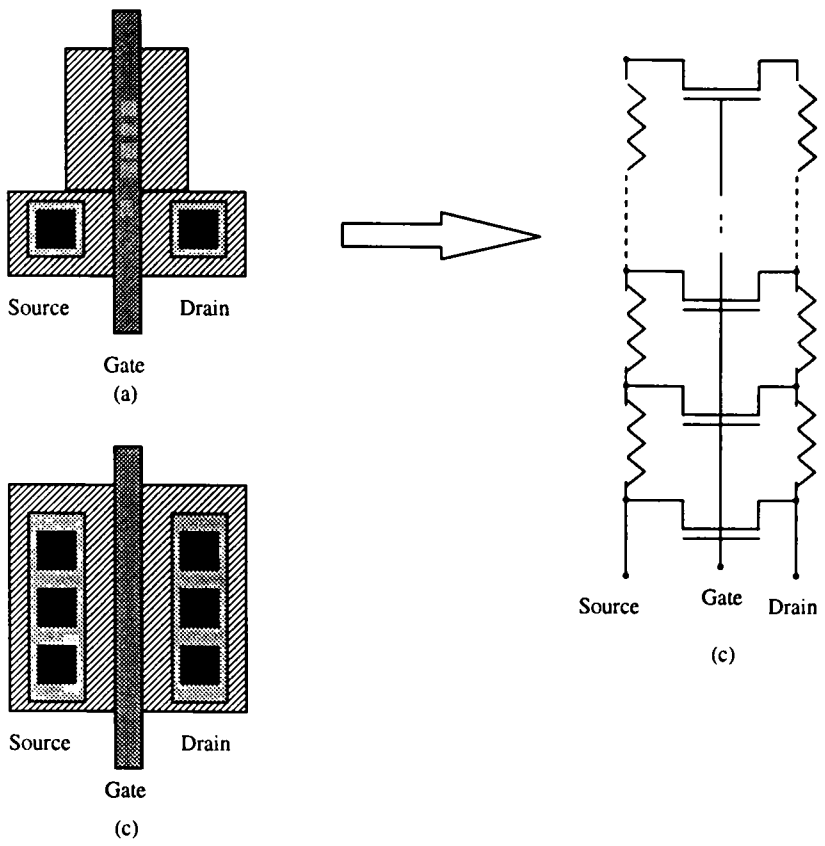


Figure 3-17. Analog MOS transistor with large aspect ratio: (a) Poor layout (b) Equivalent circuit and (c) Correct layout

connection of a number of elements, '*n*' as shown in Figure 3-18(a).[24] The electrical performance of the parallel structure is equivalent to a single transistor whose width is equal to the total width of the parallel elements. The transistor layout in Figure 3-18(b) with $n = 4$, has a shape that better meets the requirements. Additionally, this layout has the advantage that the parasitic capacitance associated with the reversed-biased diffusion capacitance is reduced. For a single transistor the parasitic capacitances C_{sb} and C_{db} (the source and drain diffusion capacitances respectively) are proportional to the width W of the transistor. For split transistors, C_{sb} and C_{db} are reduced by a factor of $(n+1)/2n$ if n is odd; however, if n is even, one of the diffusion capacitances is reduced by half, while the other is reduced by $(n+2)/2n$.

The practice of splitting a transistor into a parallel connection of a given number of parts is also useful for improving the matching between the elements. A major source

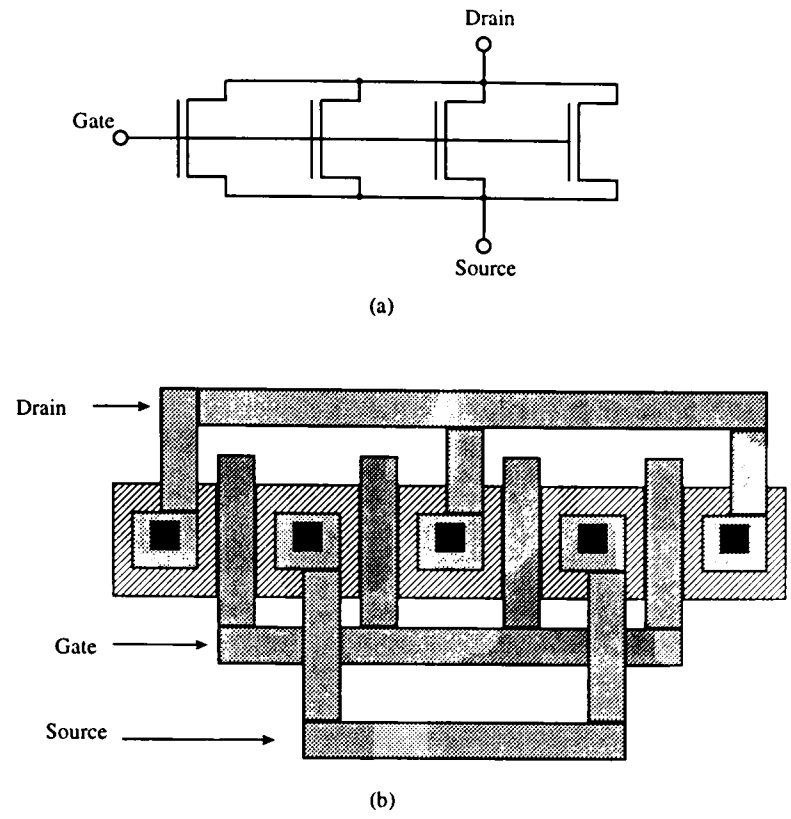


Figure 3-18 Very Large MOS Transistor Implemented as a Split Transistor:
(a) Circuit schematic and (b) Layout

of transistor mismatches is due to gradients that exist in the fabrication process. To minimize the gradient effect, two transistors that must be matched to each other should be very close. This may be difficult for wide transistors. The interdigitized[25] layout shown in Figure 3-19 overcomes this problem.

Another source of mismatch is caused by the boundary dependent etching of polysilicon gates.[26] Figure 3-20(a) illustrates this effect. The etching of unwanted patterns defines the gate of an MOS transistor. However, the etching, even for a non-isotropic process, continues to cut under the protection(undercut). This effect depends on the boundary and the undercut is more efficient for free space around the pattern to be created. Therefore the lengths of the gates G_2 and G_3(Figure 3-20(a)) are reduced less than that of the gates of the terminal elements G_1 and G_4. This effect can be significant

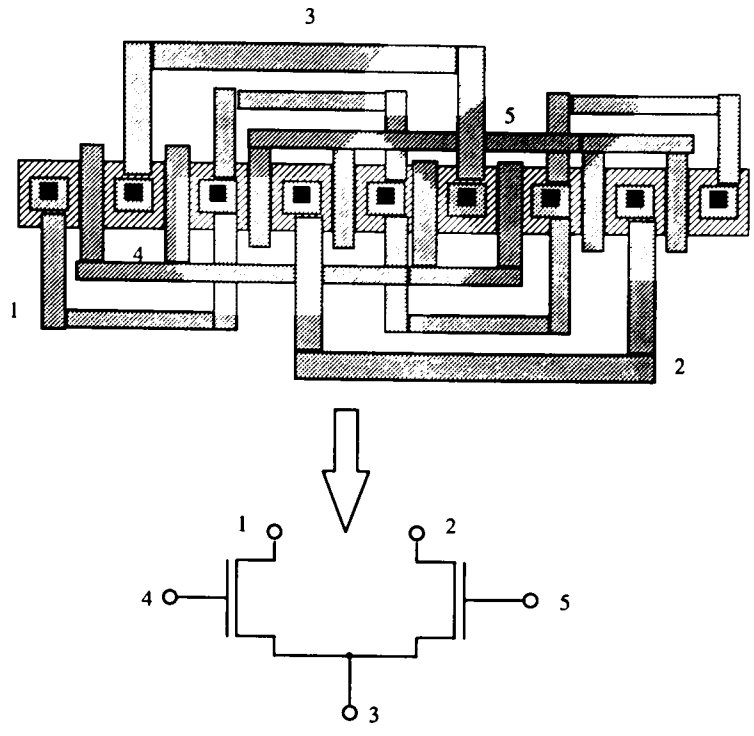


Figure 3-19. Interdigitized Layout for a Differential Pair

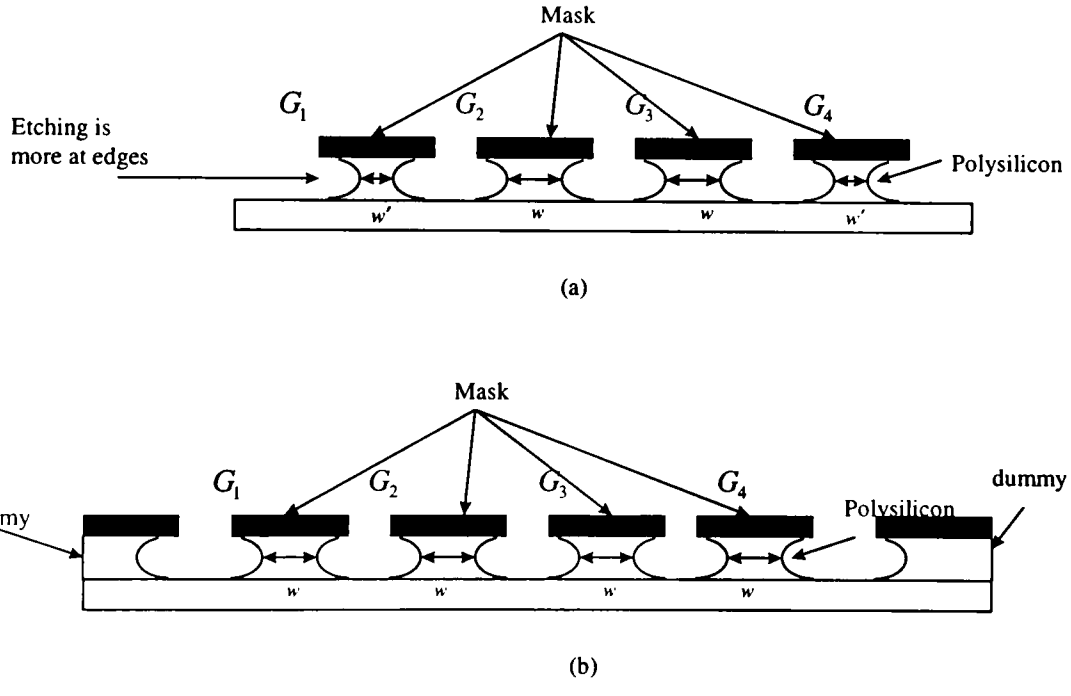


Figure 3-20. Non-uniform Etching: (a) Boundary Dependent Etching and (b) Compensation of Boundary Dependent Etching by Dummy Elements

for precise applications and can be compensated by the using dummy elements, as shown in Figure 3-20(b).

3.5.2 Capacitor Layout[23]

We will list some of the main points which should be considered, while making the capacitor layouts.

Typically, a capacitor is implemented as a *poly-2* overlap of *poly*,(*poly* and *poly-2* are the VLSI process layers, for details refer to Appendix A)with the capacitance given by the product of the area of *poly-2* and the specific capacitance. This is not accurate because of the undercut effect(discussed already for MOS transistor layout). If 'x' is the undercut for a width 'W' and length 'L' of *poly-2*, and C_{ox} is the specific capacitance, then the effective capacitance is given by

$$C_{eff} = (W - 2x)(L - 2x)C_{ox} \approx WLC_{ox} - 2[(W + L)x]C_{ox} = C - PxC_{ox}, \qquad (3\text{-}76)$$

where C is the actual capacitance, C_{eff} is the effective capacitance and P is the perimeter. Thus, the effective capacitance is smaller than the actual capacitance, by an amount which is proportional to the perimeter. This result is important when matched capacitors are to be designed. In order to also match the reduction effect due to the undercut, it is necessary to keep the area-perimeter ratio constant.

Boundary edge effects, as explained in the section on layout for MOS transistors, also occur in capacitor layouts. Most of the large capacitances are implemented as a parallel combination of smaller 'unit' capacitances. In such cases, the outermost unit capacitors are subject to the boundary effects. Dummy capacitors can be used to reduce the boundary effects.

To obtain better matching between capacitors, the capacitors are implemented as parallel combinations of 'unit' capacitances and arranged in a centroid symmetry. For details the reader is referred to ref[23].

Last, to prevent spurious coupling of signals from the substrate through the bottom plate capacitance (parasitic capacitance existing between the bottom plate of the capacitor, usually poly, and the substrate), the capacitors are isòlated from the substrate by placing them in a well and biasing the well to the highest potential (for n-well) or the lowest potential (p-well) in the circuit.

We conclude this chapter by presenting the layouts of the different circuit blocks. Figure 3-21 gives the layout of the bias circuit for the op-amp. Layouts of the transmission gate switch and the complete op-amp are given in Figures 3-22 and 3-23. Figure 3-24 gives the layout of the switched capacitor filter and the multiplier cell layout is given in Figure 3-25. Finally, the layout of the complete design is given in Figure 3-26. We would like to make a general comment on the final layout of the complete design. To an experienced VLSI designer, the layout might not appear optimal. Our goal here is to build the different circuit blocks comprising a single heterodyne detector element and test them individually. This explains the apparently generous usage of the silicon area.

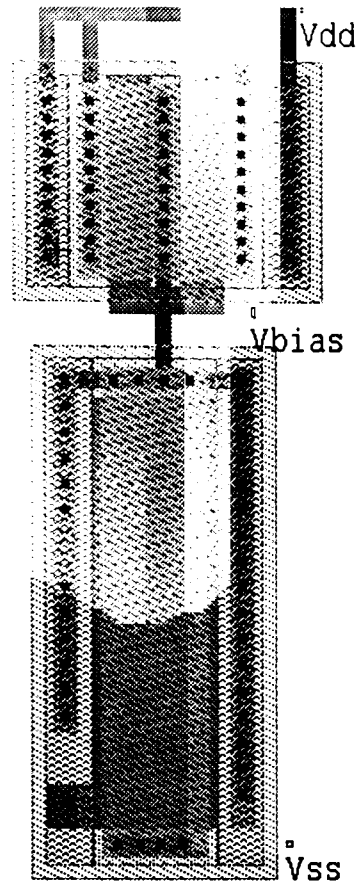


Figure 3-21. Bias Circuit Layout

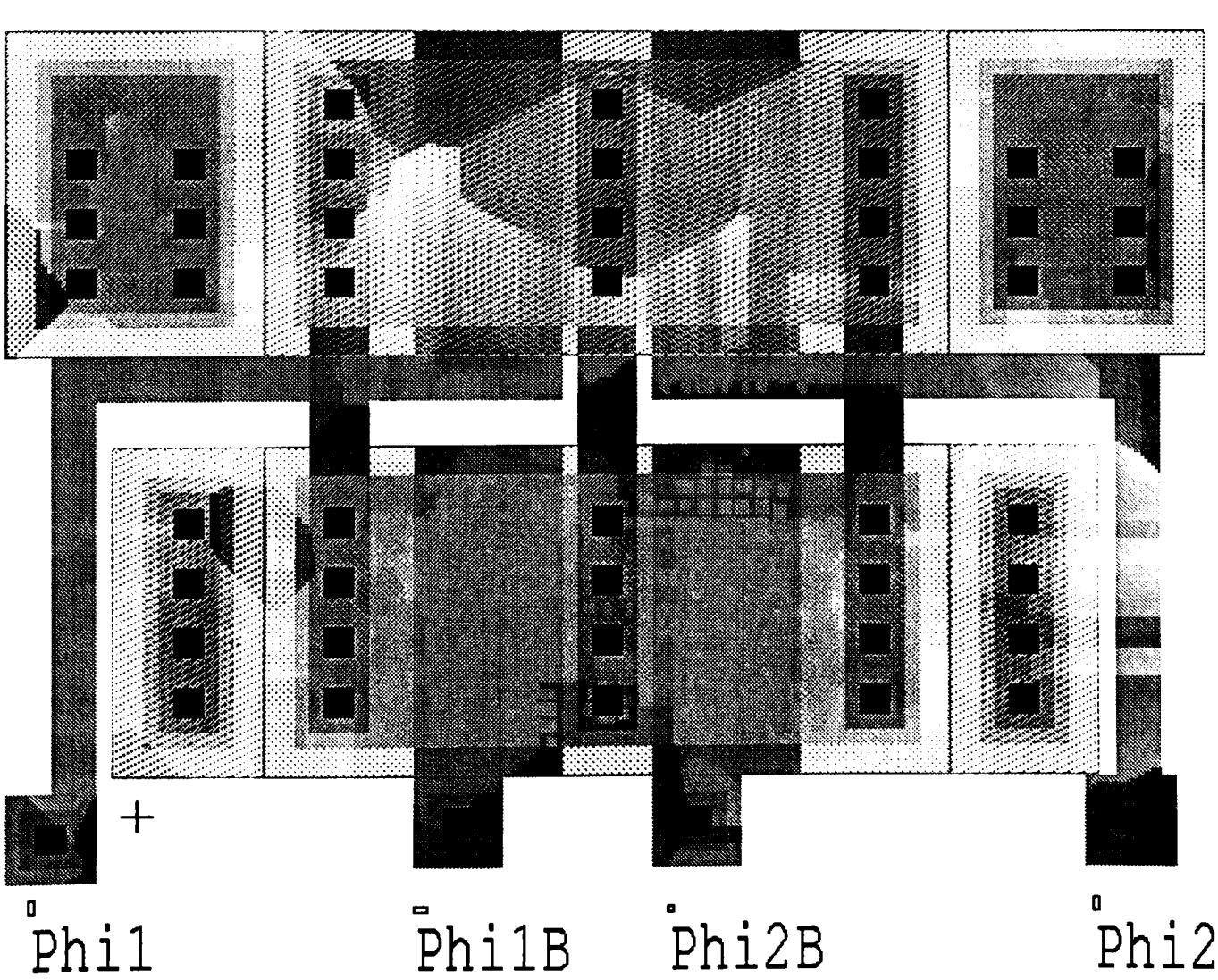


Figure 3-22. Analog Switch(SPDT)

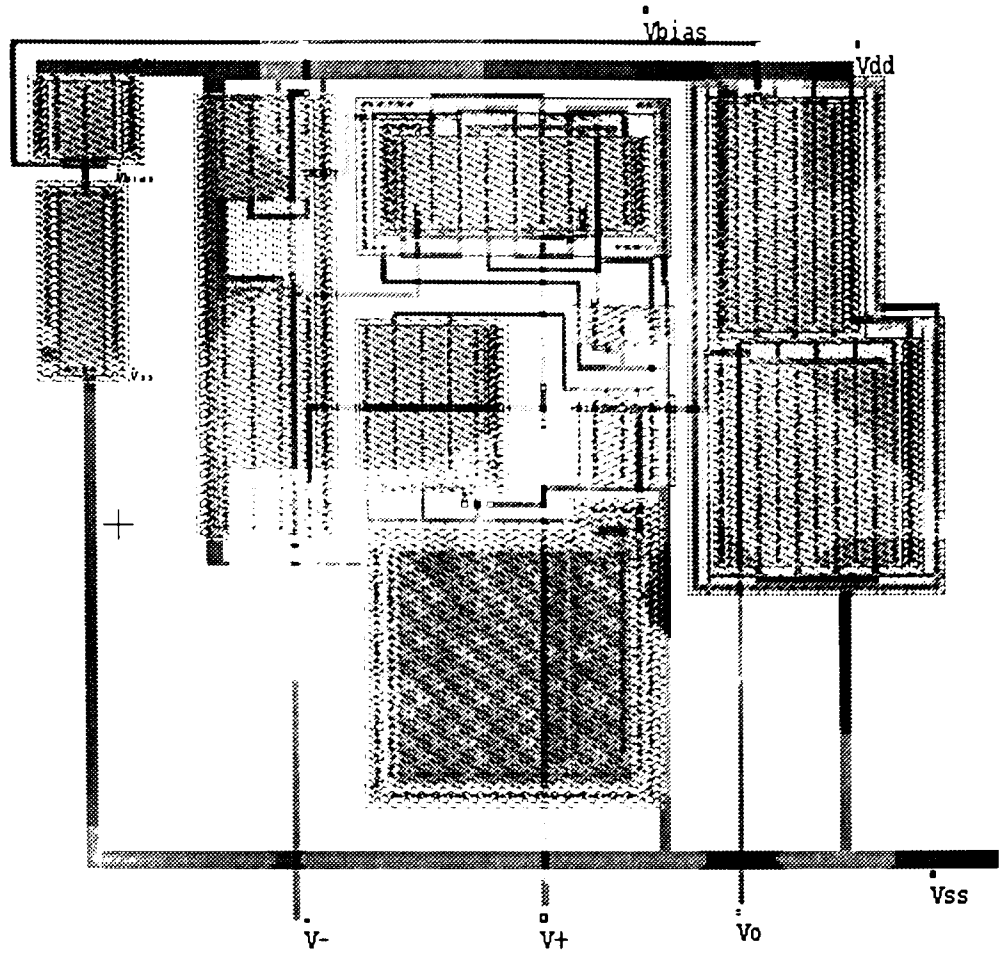


Figure 3-23. Op-amp Layout

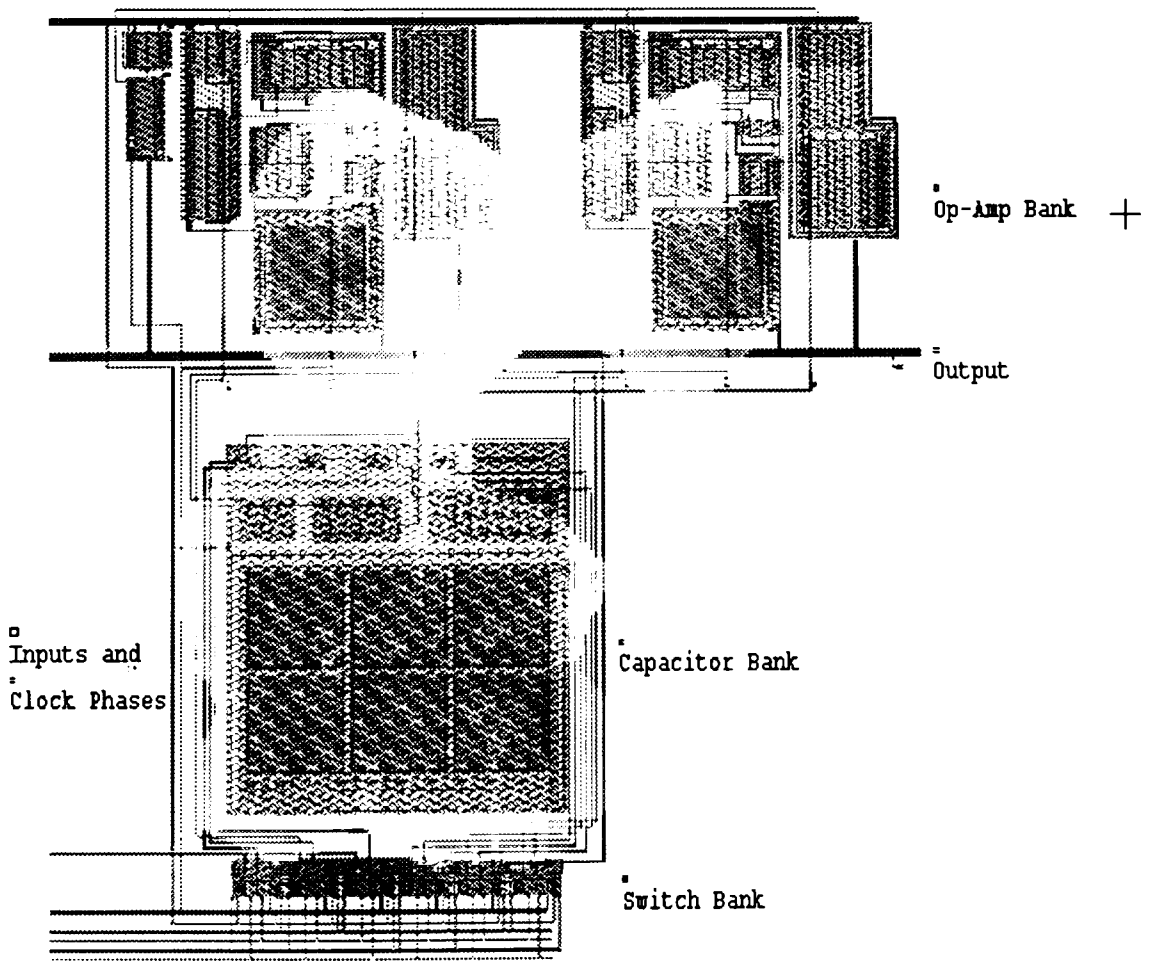


Figure 3-24. Switched Capacitor Filter Layout

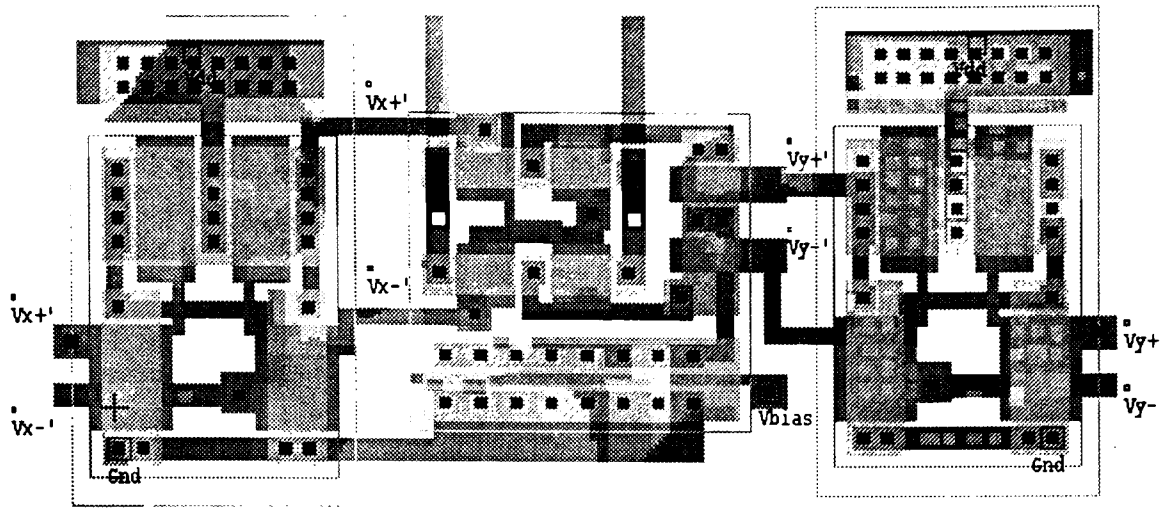


Figure 3-25. Multiplier Cell Layout

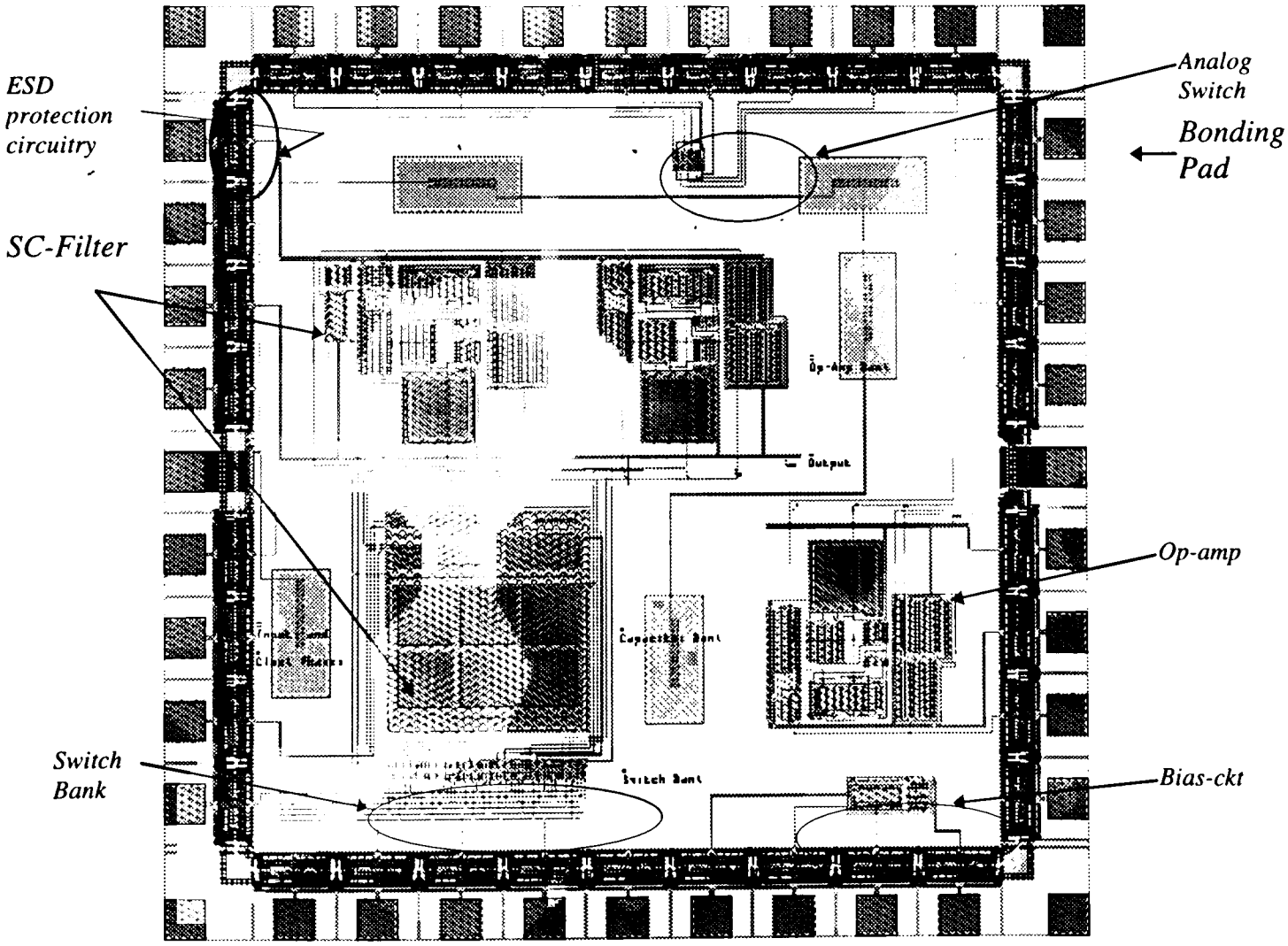


Figure 3-26. Layout of the Prototype Design

CHAPTER 4

SIMULATION RESULTS

In Chapter 3, we presented the detailed circuit design of the individual blocks for the heterodyne detector array. We have tried to make the design of the detector array quite modular. To this end, our preliminary design was aimed at designing individual circuit blocks, comprising a single heterodyne detector element and testing the functionality of each circuit block. Our next attempt would be to fabricate a small heterodyne detector array(4x4) and test its functionality in general, with particular attention to problems like cross-talk. We have used the MOSIS Orbit 2.0μ N-well process for our design. The circuit design and simulations were done in the mixed signal circuit simulator Pspice® and the layout was generated using the VLSI CAD tool L-EDIT. Simulations were also carried out on circuits extracted from the layouts generated in L-EDIT. The extracted circuits contain the parasitic capacitances and simulations on the extracted circuits should better approximate the real-time circuit functionality. In this chapter, we present the simulation and experimental results (from the first prototype) for the individual circuit blocks.

4.1 Op-amp Simulation Results

In Chapter 3, Sec.(3.2.1), we have presented some of the performance metrics for an operational amplifier. We tested our op-amp on similar lines and tried to determine some of the more important properties, i.e., dc-gain, unity gain bandwidth, phase margin,

slew rate, settling time, offset voltage, PSRR (power supply rejection ratio) and CMRR (common mode rejection ratio).

We present below the test circuits used to obtain the op-amp parameters and the simulation results. Figure 4-1 shows the test circuit used to perform a dc-sweep on the op-amp. One of the inputs of the op-amp (non-inverting in this case) is grounded, and a dc-sweep source is applied on the other input (inverting) and the output voltage is plotted against the dc-sweep voltage. The input dc-voltage corresponding to zero output gives the offset voltage referred to the non-inverting input. The simulation results for the Pspice®circuit and the extracted layout are given in Figures 4-2 and 4-3. The results show a decent swing of the output to within a threshold level of the power supply voltages and a low offset voltage of about 0.6mV.

The Pspice® simulation circuit for measuring the ac-gain is the same as used for the dc-sweep (Figure 4-1), with the dc-sweep source replaced by an ac-voltage source. The frequency of the ac-voltage source was swept from dc to 100 MHz, with the input magnitude fixed at 1mV. The simulation results for the designed circuit and the extracted circuit are given in Figures 4-4 and 4-5. The phase margin is obtained by from the phase plots (Figures 4-4(b) and 4-5(b)) of the ac-gain. The phase margin is calculated by adding 180° to the phase of the ac-gain corresponding to unity gain. We obtained a dc-gain of about 63dB and a pretty good phase margin of 70°, for a unity gain bandwidth of 1.5 MHz for the extracted op-amp.

Figure 4-6 gives the simulation circuit for determining the slew rate and the settling time of the op-amp. It is a simple voltage follower (non-inverting), with a load

capacitance of 10pF. The input in this case is a square wave, with rise and fall times greater than the slew rate of the op-amp (4V/μs), so that the op-amp operates under slew rate limited conditions. Slew rate is given by the slope of the op-amp output. The settling time is the difference between the instants at which the step input (edge of the square wave) is applied and the instant at which the op-amp output settles to within 1% of the final value. The slew rate for the extracted op-amp was 4.2V/μs and the settling time was about 3.66μs.

The PSRR can be obtained by the circuit shown in Figure 4-9. The op-amp input is reduced to zero and an ac-source is applied in series with one of the power supplies of the op-amp. If A_{vd} is the small signal differential gain and A_{dd} is the small signal power supply gain, the output voltage can be written as:

$$V_o = A_{vd}\left(V_+ - V_-\right) + A_{dd}V_{dd}\,. \tag{4-1}$$

Substituting $V_+ = 0$ and $V_- = V_o$ in Equation(4-1), we get

$$V_o = \frac{A_{dd}V_{dd}}{1 + A_{vd}} \cong \frac{A_{dd}}{A_{vd}}V_{dd} = \frac{V_{dd}}{PSRR} \tag{4-2}$$

where V_{dd} is the small signal ac-source in series with the power supply. Thus by measuring the output voltage, the PSRR can be obtained using Equation(4-2). Since the PSRR varies with frequency, we swept the ac source from dc to 100 MHz. The PSRR (in dB) for the designed circuit is plotted in Figures 4-10. A maximum PSRR of 73.3dB was obtained from the designed op-amp.

The circuit for determining the CMRR is given in Figure 4-11. Since the CMRR varies with frequency, the input common-mode ac source was swept from dc to 100

MHz. The plot for the CMRR (in dB) for the designed circuit is shown in Figures 4-12. The designed op-amp has a maximum CMRR of 70dB.

The values of the different op-amp parameters obtained from the designed and the extracted circuits are listed in Table 4-1.

Table 4-1. Op-amp Parameters-Designed and Extracted Circuits

	Designed	Extracted		Designed	Extracted
dc gain	64.87	63.58	Settling time	4.6μs	3.66μs
Phase margin	70.42°	77.0°	$(PSRR)_{max}$	73.3dB	-
Offset voltage	-603μV	-610μV	$(CMRR)_{max}$	70.0dB	-
Slew rate	4.2V/μs	4.3V/μs			

4.2 Multiplier Cell Simulation Results

The basic circuit for the simulation of the multiplier cell is given in Figure 4-13. We have used balanced differential signals for the two inputs of the multiplier cell. These are generated using a very simple resistive divider arrangement. We basically tested the multiplier (or mixer) under four different conditions:

1. The first is to test the linearity of the multiplier. This is done by performing a nested dc-sweep on the two inputs to the multiplier, i.e., fix the dc potential on one input and then sweep the second input over the entire input range, then change the dc potential on the first input and repeat the dc-sweep on the other input and so on. The multiplier

is linear for input ranges +2 to -2V for both the inputs. The output curves for the dc-sweep are plotted in Figure 4-14.

2. We performed a transient analysis on the multiplier cell by selecting one input as 1kHz, 0.5V sinusoid and the other as 1.333kHz, 0.5V sinusoid. These inputs are representative of the maximum perturbation frequencies of the rotating mirror used in the spatial derivative extraction system described in Chapter 2. The differential output of the multiplier and the Fourier transform of the output are plotted in Figures 4-15 (a) and (b). As expected the output principally comprises of the sum and difference frequencies, i.e., 333Hz and 2.333kHz, respectively, with a highly attenuated spurious harmonic component at 5.32k.

3. The third case is very much identical to the second case. In this case we went one step further to simulate the actual case. One of the inputs to the multiplier was a sum component comprising 0.5V 1kHz, 1.333kHz , 333Hz and 2.333Hz sinusoids. If we go back to table 3-1 in Chapter 3, we can see that these frequency components correspond to the first order x and y derivatives and a second order joint x-y derivative. The other input was selected as 0.5V 1kHz sinusoid, which would be the reference frequency to extract one of the first order spatial derivatives. Theoretically the output should consist of a dc component and seven different frequencies (sum and difference frequencies of the reference and the input signal). The frequency component corresponding to 1.333kHz cancels out due to the opposing phases generated by the mixing of 333Hz and 1kHz and 2.333kHz with 1kHz. The

simulation results shown in Figures 4-16 (a) and (b) are in total agreement with the theoretically expected output.

4. We also plotted the frequency response of the filter. This was done by fixing one of the input voltages at a fixed dc potential and performing an ac-sweep on the second input. The frequency response of the multiplier is given in Figure 4-17.

4.3 SC Filter Simulation Results

We essentially performed only a transient analysis on the SC filter. Two sets of input signals were selected for the simulation. The first input comprised the pass band and the stop band edge frequencies, i.e., 100Hz and 1kHz (each 100mV). The filtered output and the input signal are plotted in Figure 4-18(a). The Fourier transform of the filter output is shown in Figure 4-18(b). The output frequency components are in close agreement with the theoretically calculated values from the filter transfer function.

In the second transient analysis we added a 333Hz component to the input. The justification for testing the filter for the 333Hz component can be well appreciated if we look at the analysis of the mixer output frequencies presented in Table 3-1, Chapter 3. If the desired component is 100Hz, then there is an error in the filter output due to the 333Hz component. This can be reduced by using a higher order filter, but we tried to optimize the filter order and the real estate silicon area and settled for a second order filter. The results are given in Figures 4-19 (a) and (b).

4.4 Experimental Results

We have submitted two prototype designs for the heterodyne detector element. We wanted to test the individual circuit blocks before putting together the complete 2-D detector array. The second prototype submitted by us to the MOSIS foundry is still under fabrication. The first prototype design was not completely functional. The op-amp circuit block and the analog switch bank gave positive results. Test results on these blocks did not totally meet the design specifications. We attribute this to some circuit design issues which were not taken care of in the design of the first prototype. The principal problems, we think, with the design were a poor estimate of the load capacitance (parasitic capacitances due to the bonding pads and the package leads) and use of level 2 model for the simulation of minimum feature size devices. The multiplier block in the first prototype design did not work. We anticipate some fabrication problems with the multiplier block. The Orbit 2.0μ n-well process is not optimized for the fabrication of photo-diodes, which did not work. The absorption depth for He-Ne laser light (~ 633nm) is about 1.5μm and the p+ diffusion depth is about 0.9μm, which probably explains the poor responsivity of the photo-diodes.

We have redesigned the different circuit blocks for the second prototype design. Since we would be using the circuit blocks from the second prototype design for future designs of the detector array, we were not inclined to include the simulation results from the first prototype design in the thesis. In the second prototype design, we have specifically addressed the design lapses of the first prototype design and we have also performed extensive simulations on the revised design of the circuit blocks. The

simulation results are encouraging and we hope that the second prototype design will work according to the specifications.

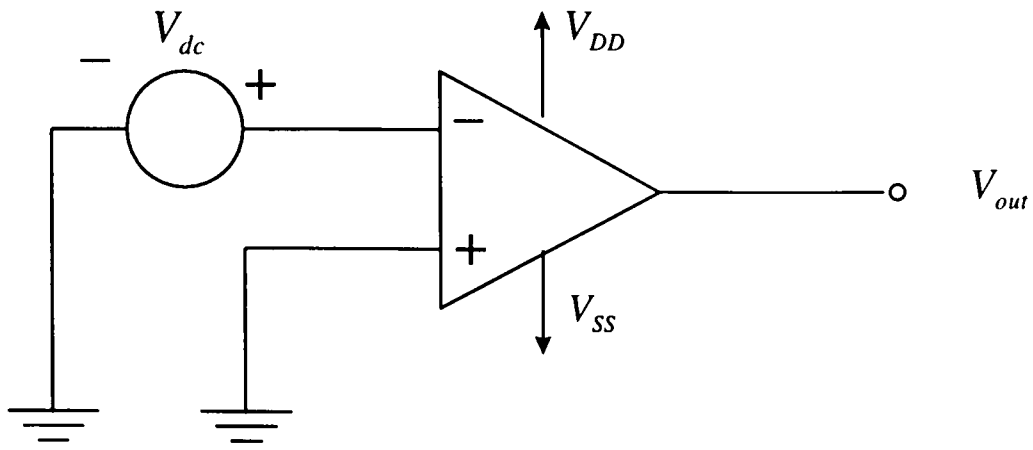
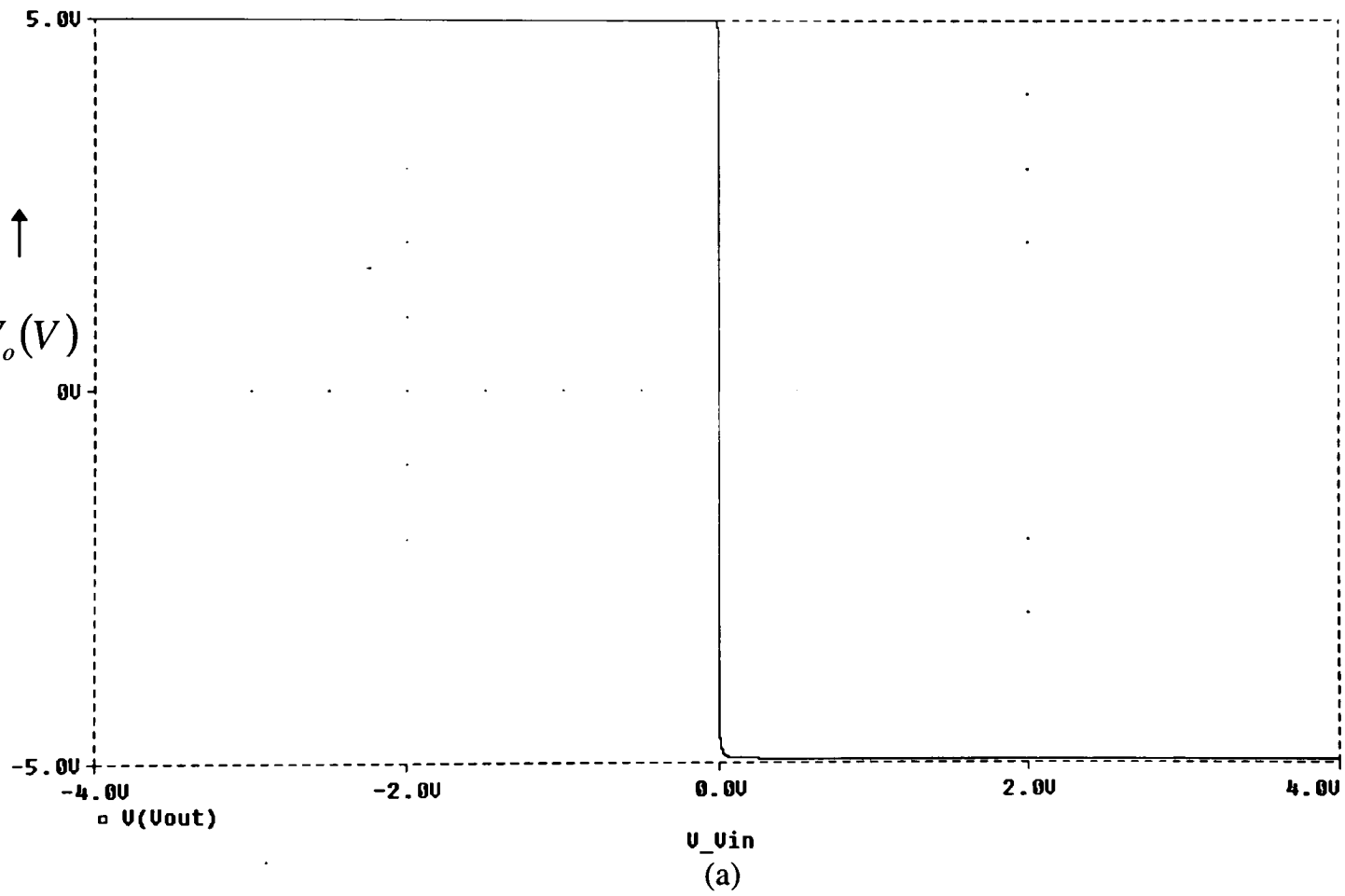
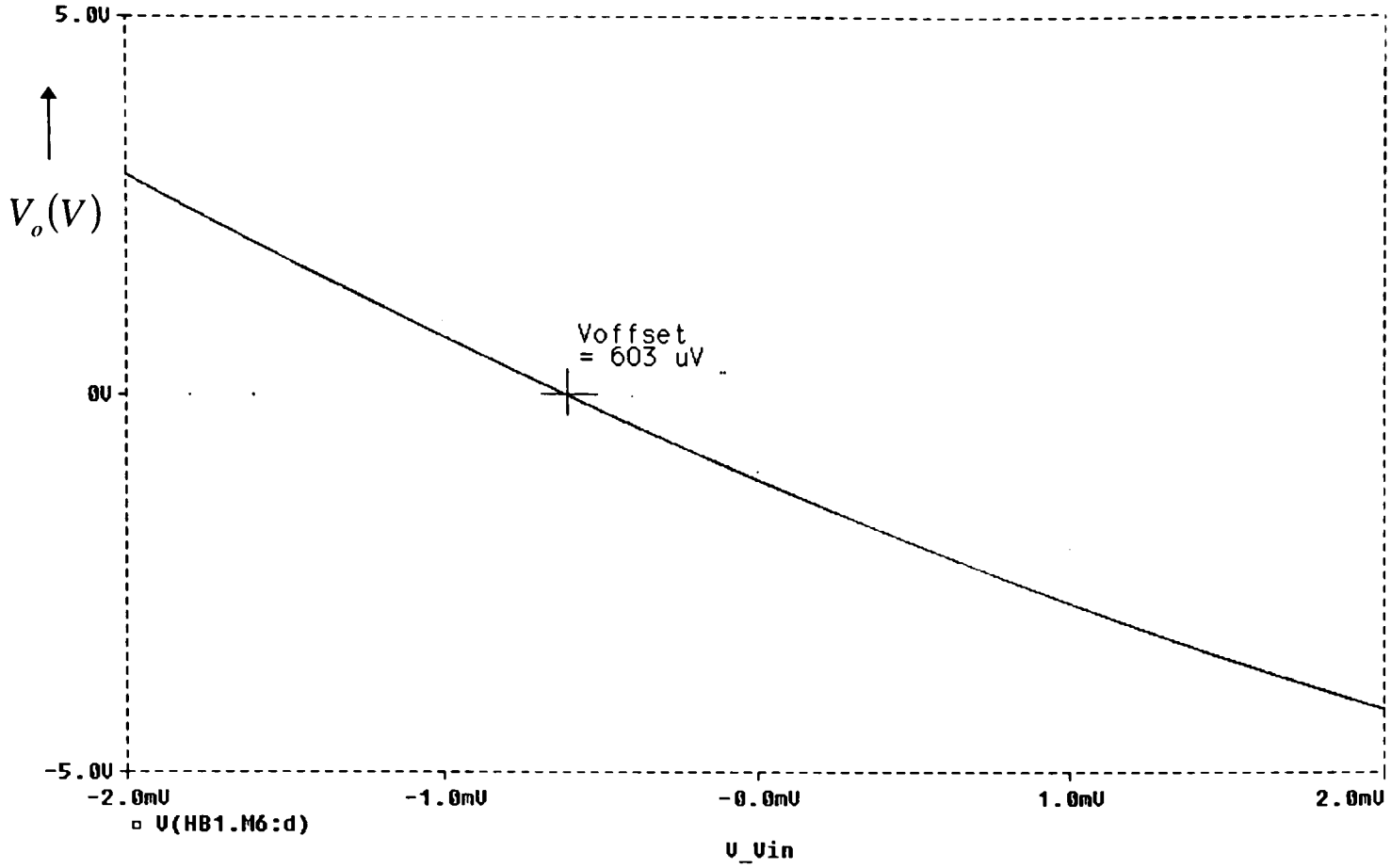


Figure 4-1. DC-sweep Circuit



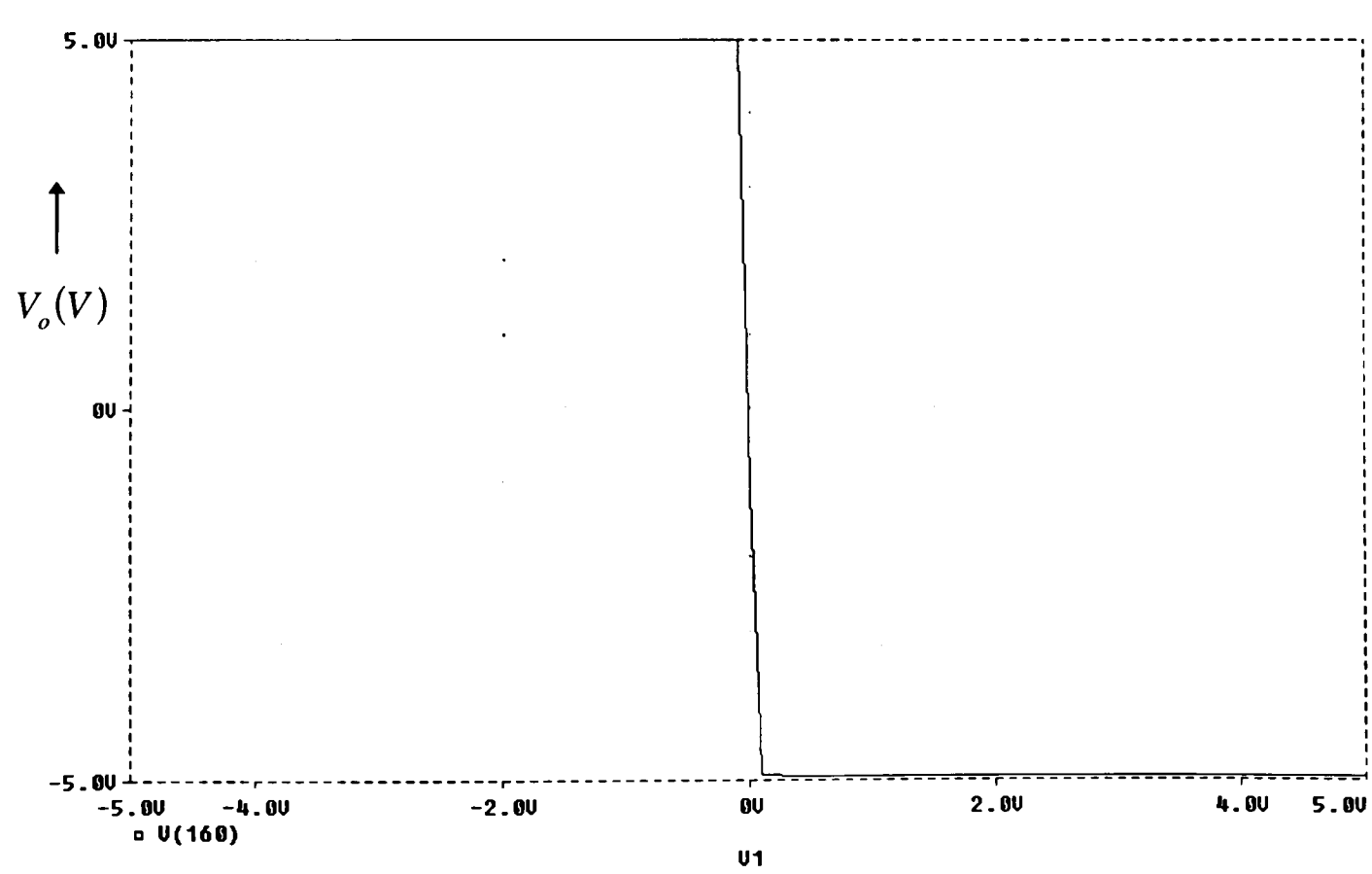
(a)

Figure 4-2. DC Analysis of the Designed Op-amp: (a). DC-sweep on the designed op-amp and (b) Magnified DC-sweep Highlighting the Offset Voltage



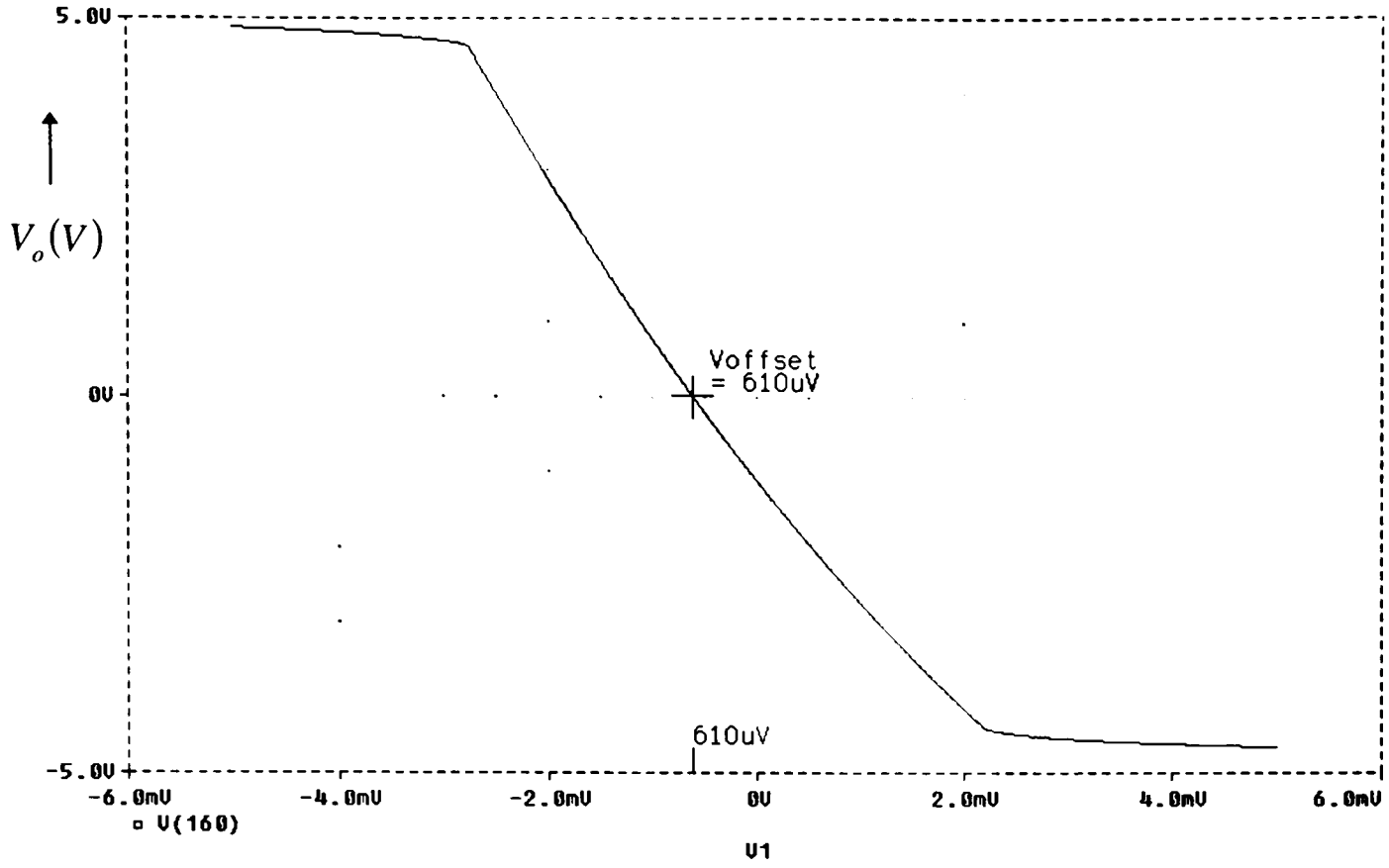
(b)

Figure 4-2 continued.



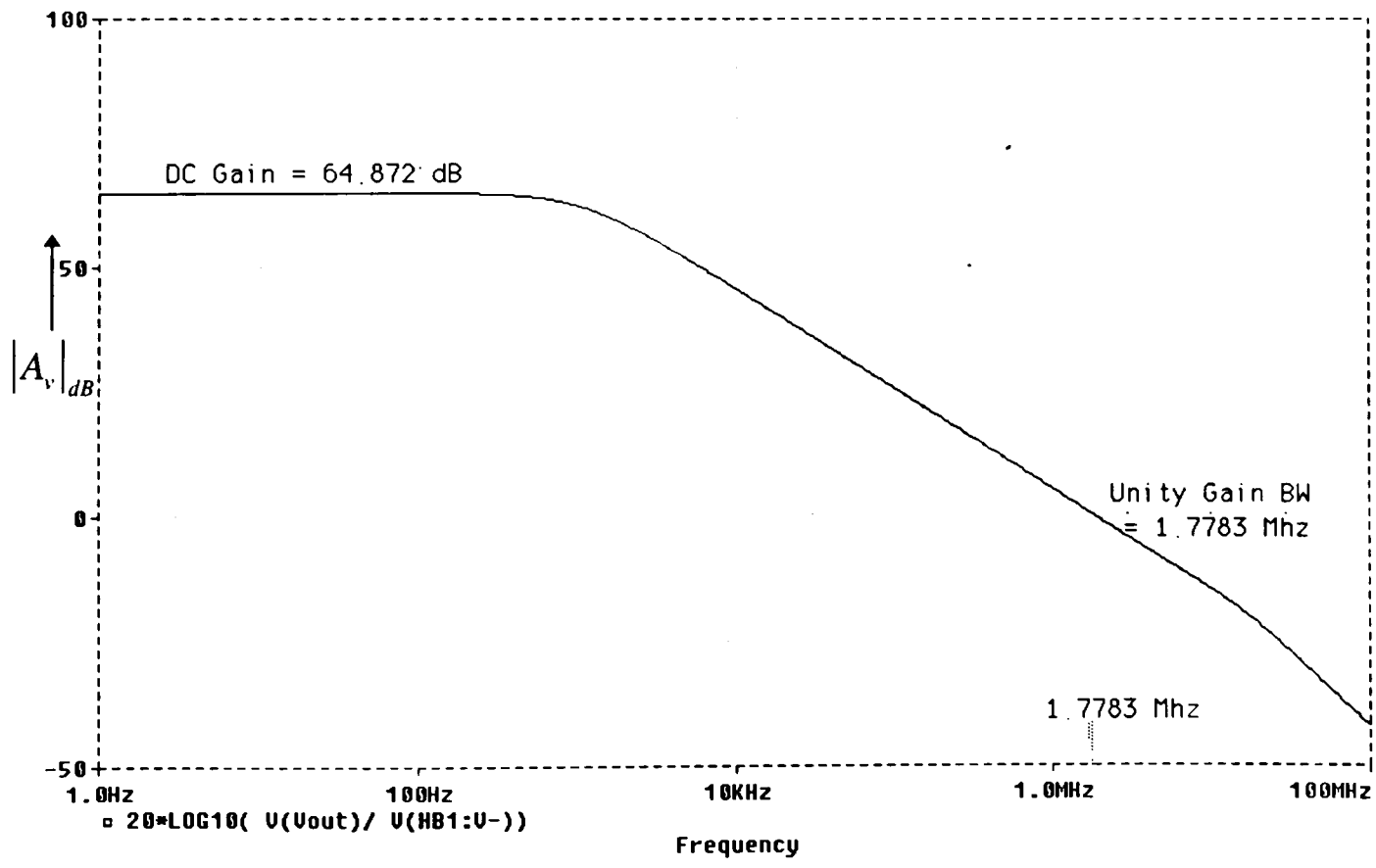
(a)

Figure 4-3. DC Analysis on the Extracted Op-amp: (a) dc-sweep on the extracted layout of the op-amp and (b) Magnified DC-sweep Highlighting the Offset Voltage



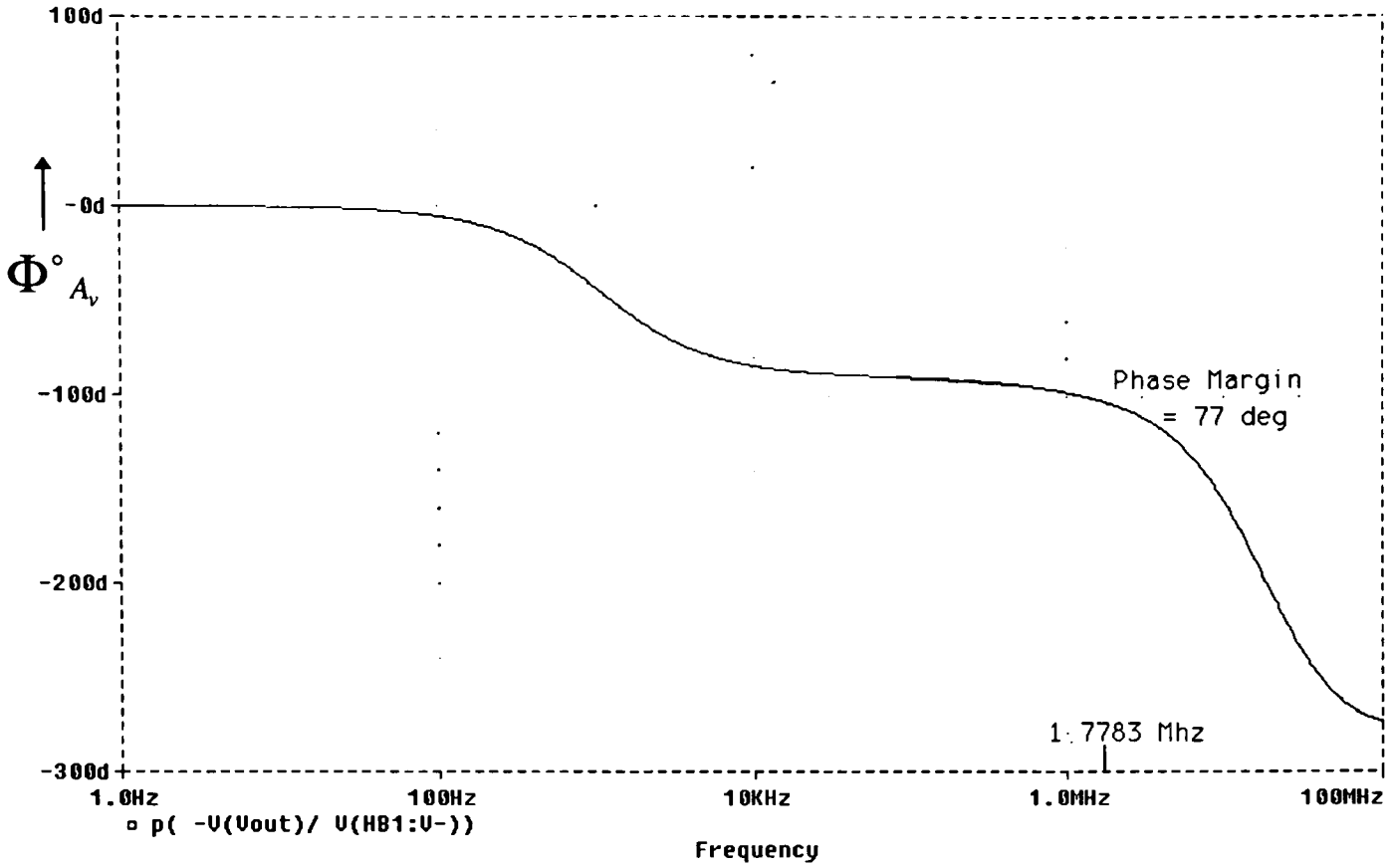
(b)

Figure 4-3 continued.



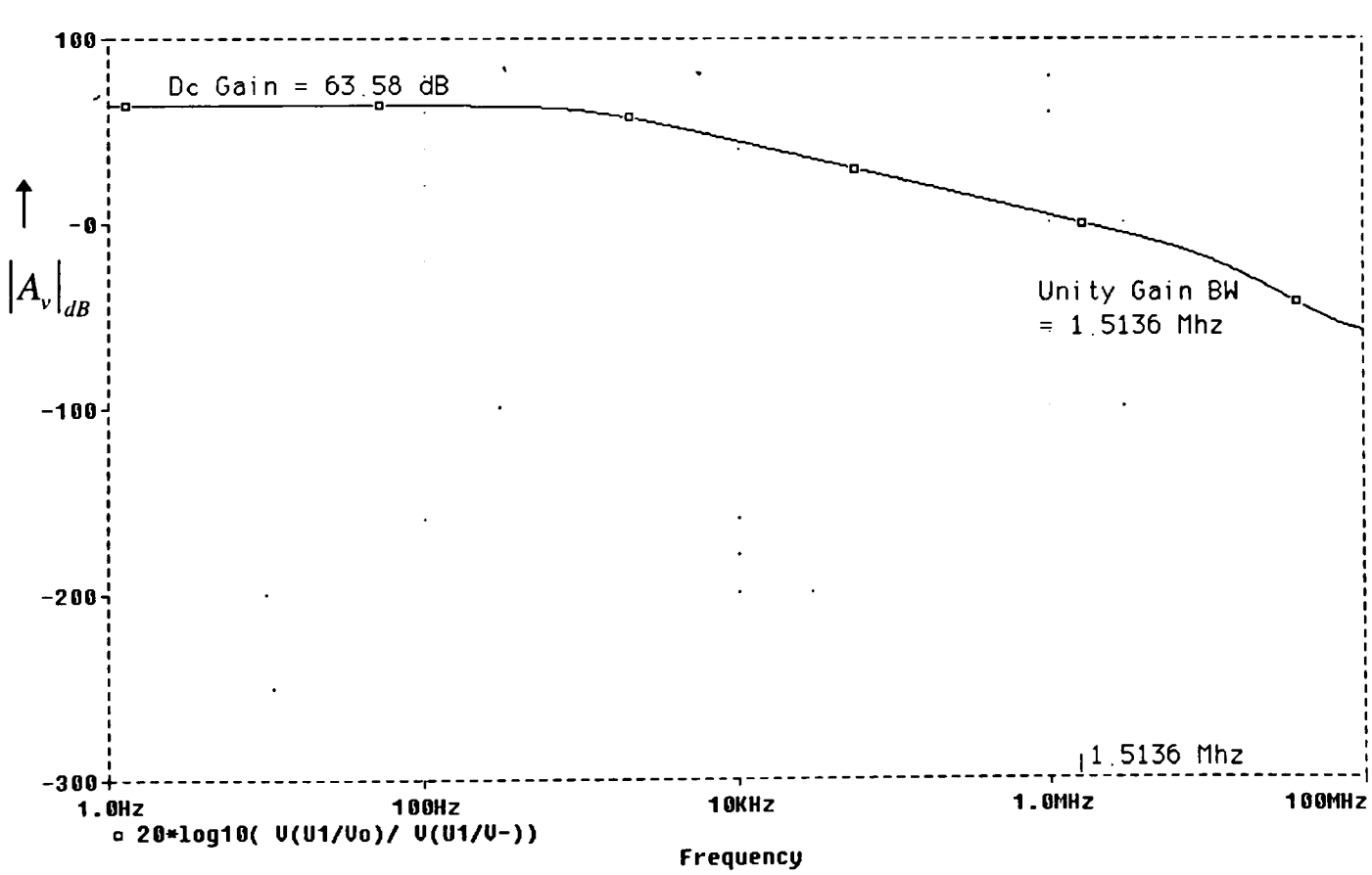
(a)

Figure 4-4. AC Analysis of the Designed Op-amp (a) Magnitude Response of Open-loop Gain and (b) Phase Response of Open-loop Gain



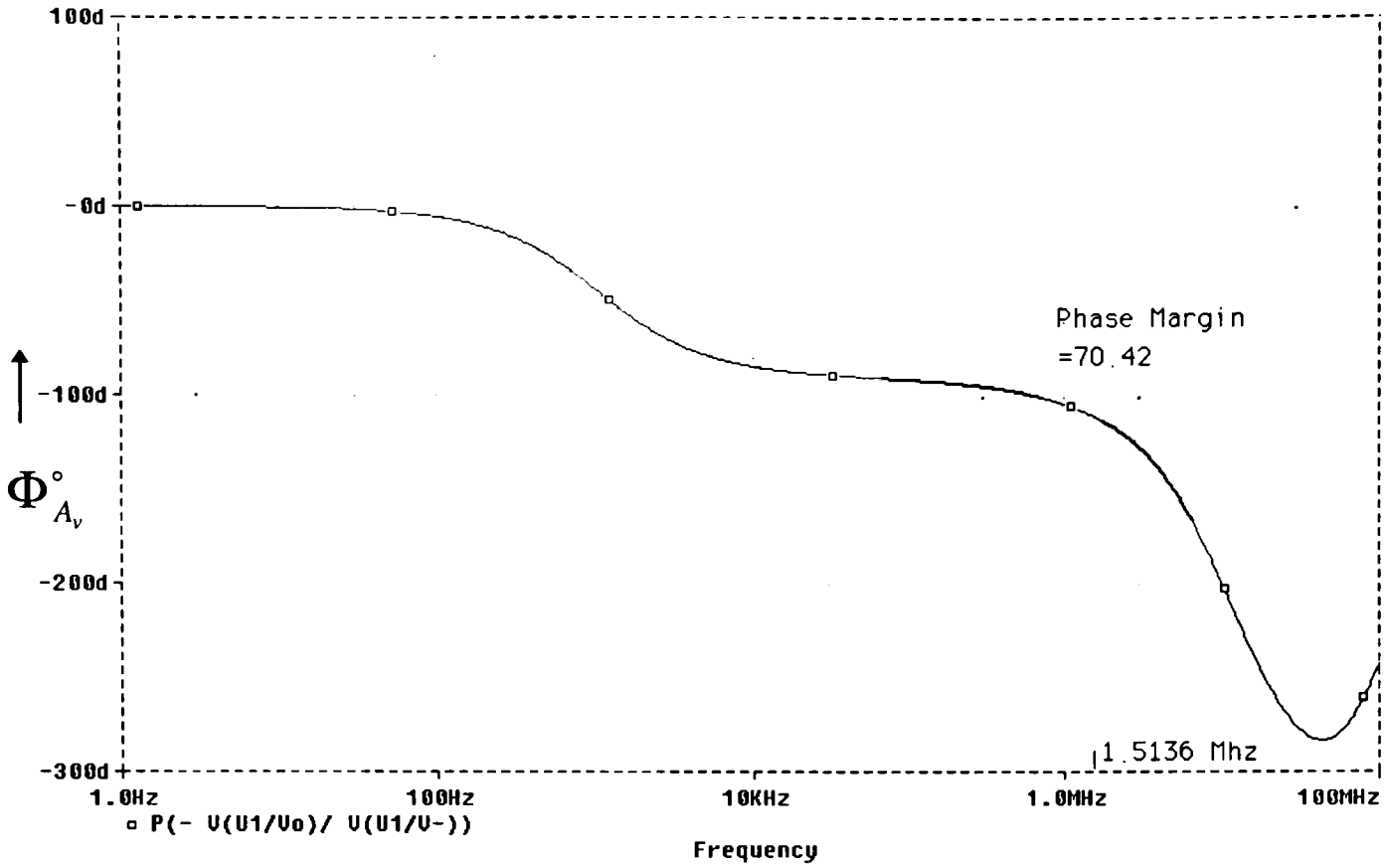
(b)

Figure 4-4 continued.



(a)

Figure 4-5. AC Analysis of the Extracted Op-amp: (a) Magnitude Response of Open-loop Gain and (b) Phase Response of Open-loop Gain



(b)

Figure 4-5 continued.

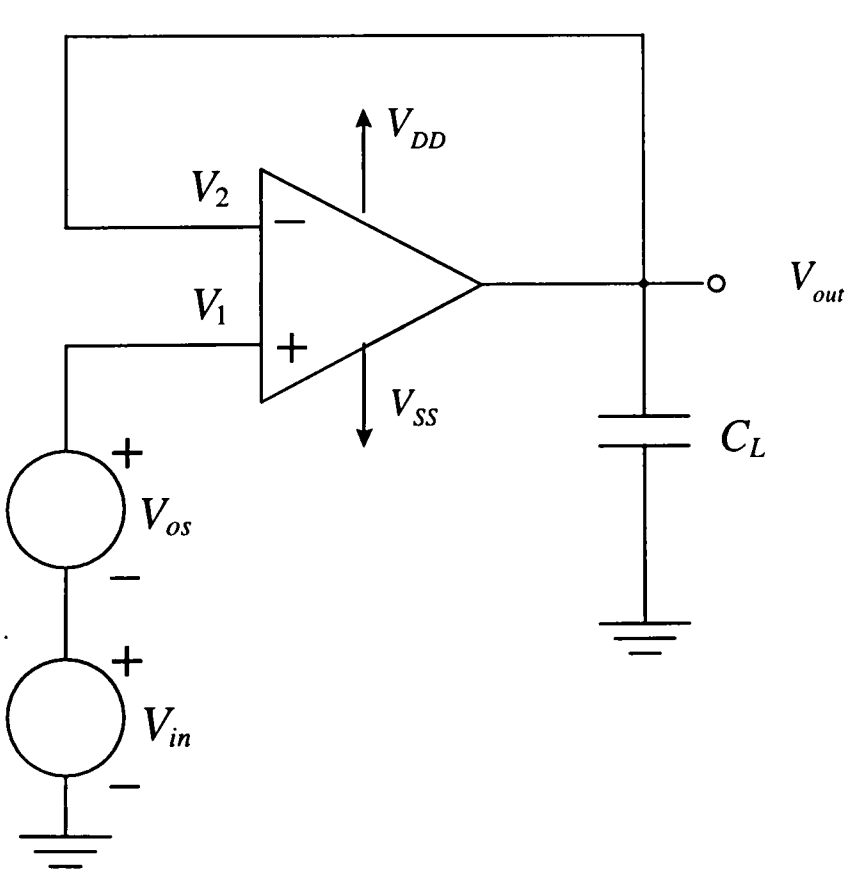
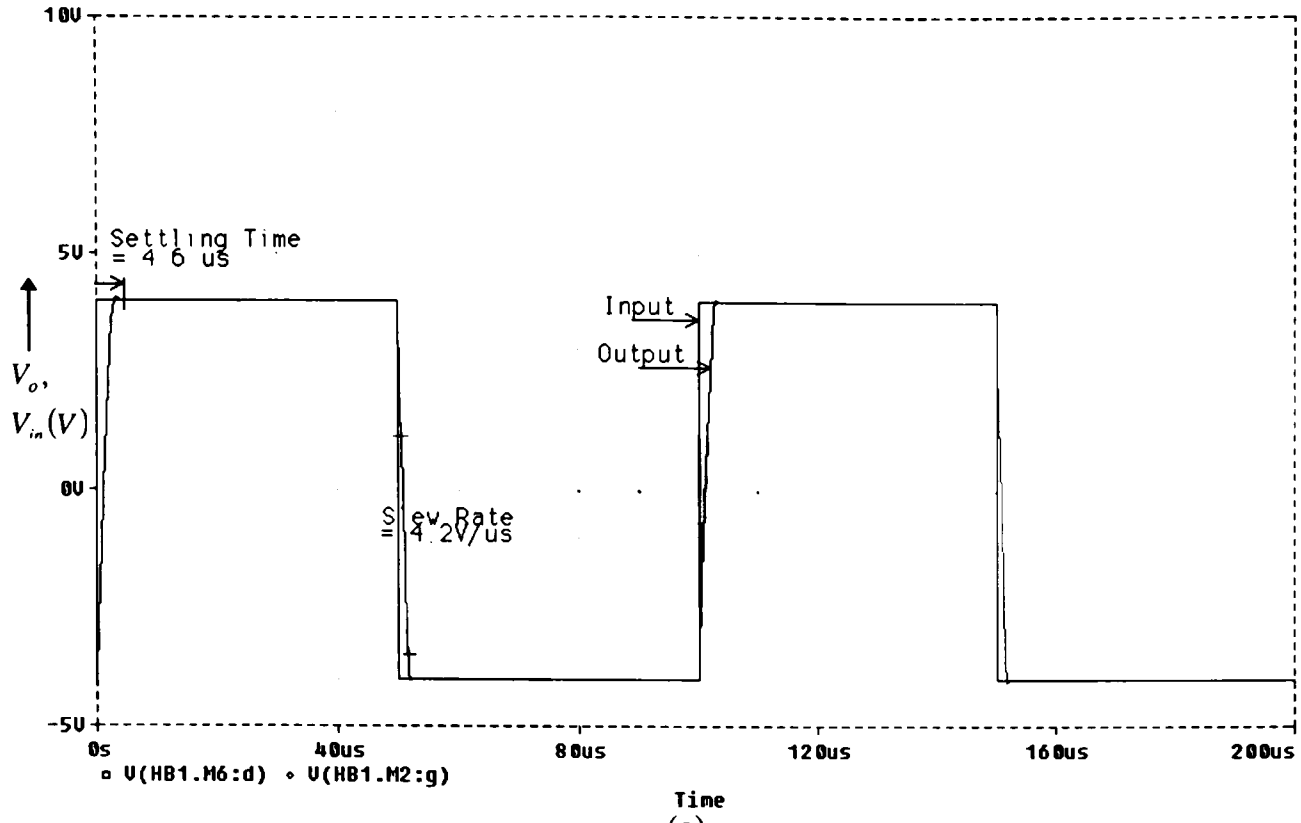
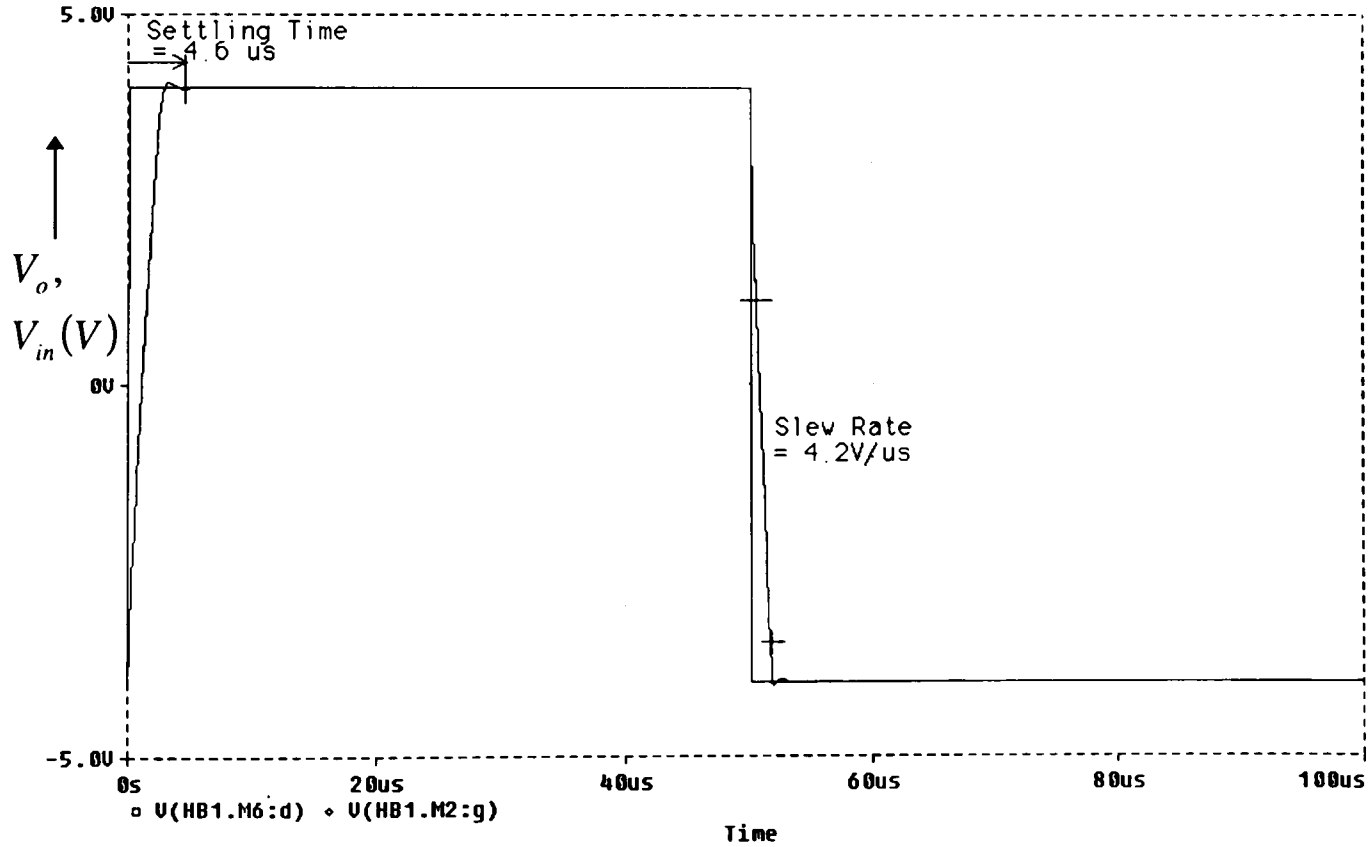


Figure 4-6. Circuit to Determine the Slew Rate and Settling Time of the Op-amp

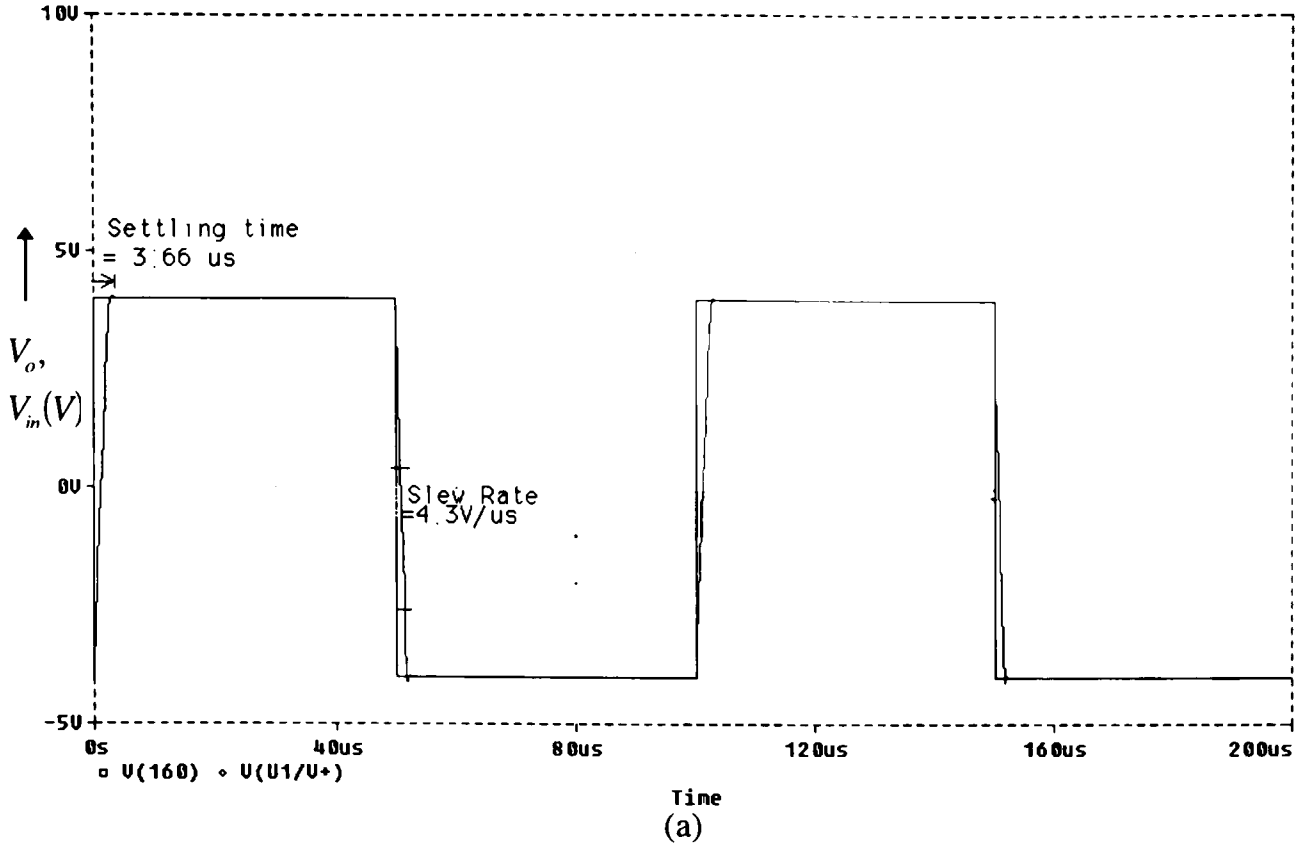


(a)

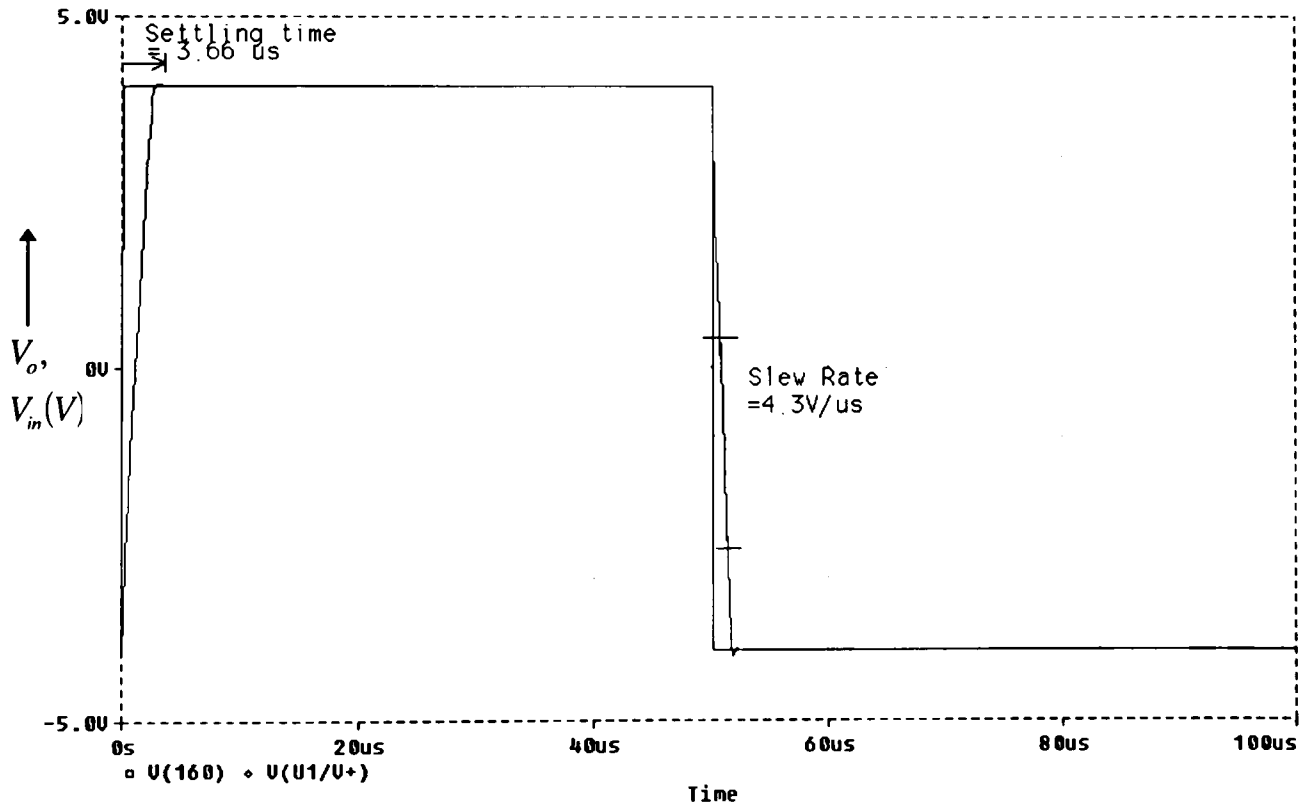


(b)

Figure 4-7. Slew Rate Measurement on the Designed Op-amp: (a). Op-amp output for Square Wave Input (±4V Square wave with 0.1μs rise/fall times) and (b) Magnified Plot of Figure 4-7(a) Showing Slew Rate and Settling Time Measurements



(a)



(b)

Figure 4-8. Slew Rate Measurement on the Extracted Op-amp: (a). Op-amp output for Square Wave Input (±4V Square wave with 0.1μs rise/fall times) and (b) Magnified Plot of Figure 4-8(a) Showing Slew Rate and Settling Time Measurements

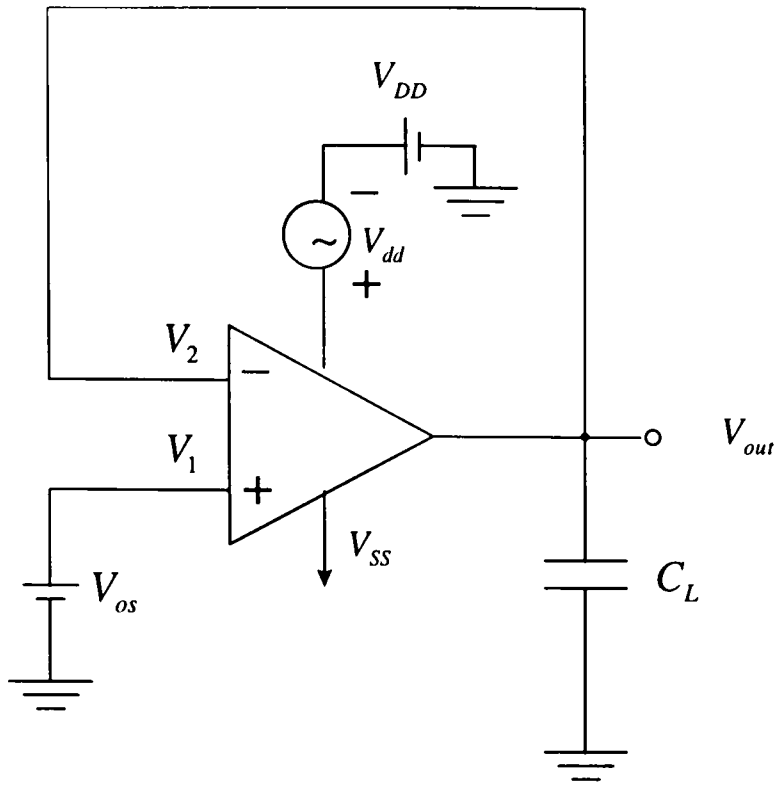


Figure 4-9. Circuit to Determine PSRR

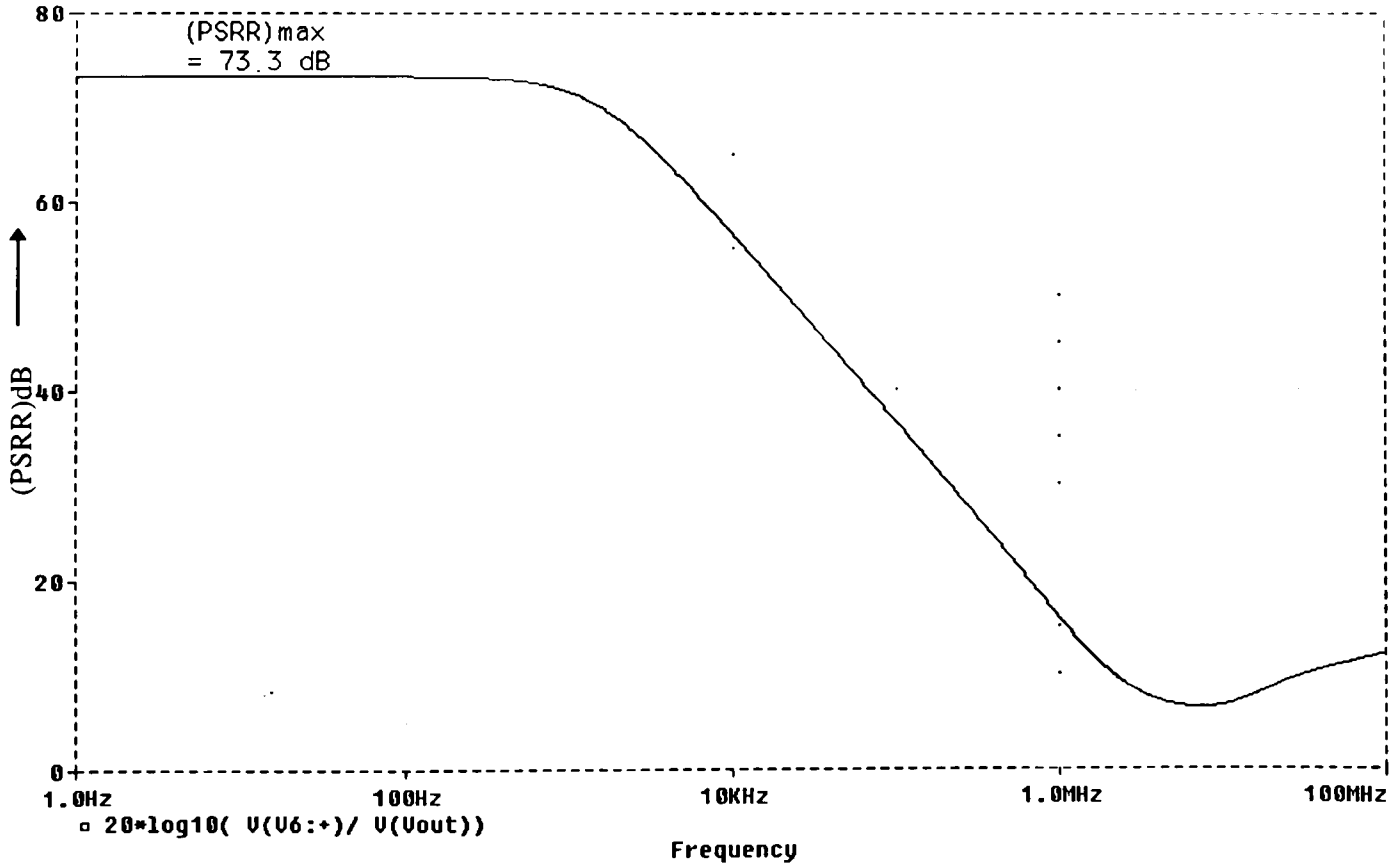
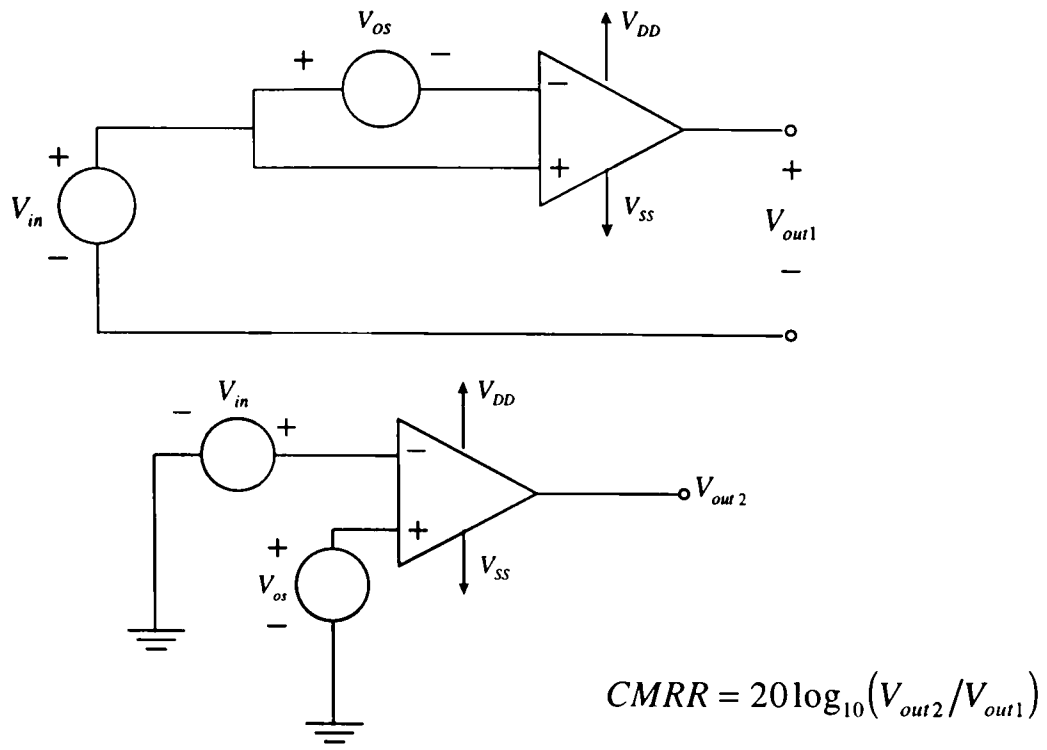


Figure 4-10. PSRR of the Designed Op-amp



$$CMRR = 20\log_{10}\left(V_{out2}/V_{out1}\right)$$

Figure 4-11. Circuit to Determine CMRR

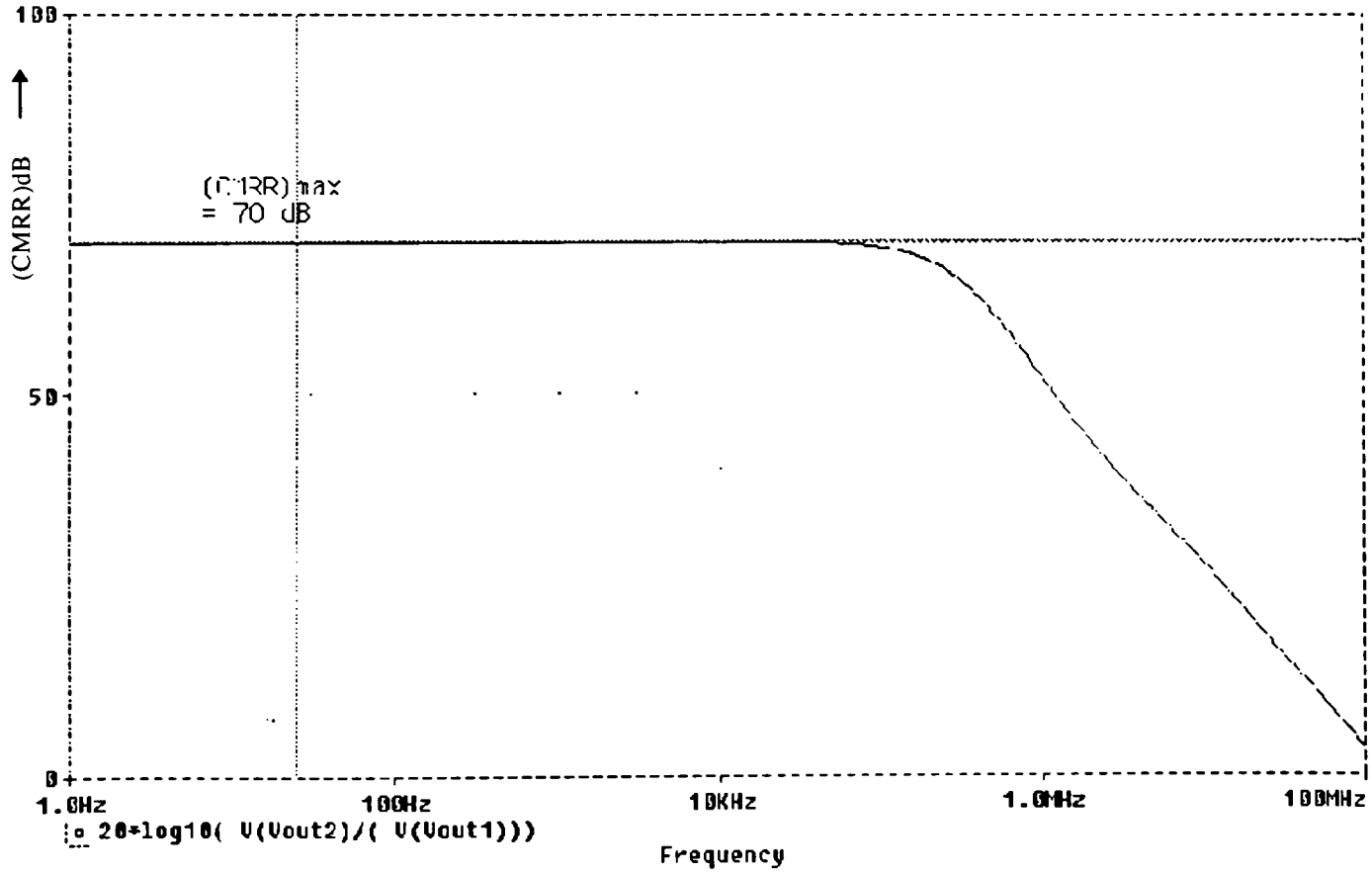


Figure 4-12. CMRR of the Designed Op-amp

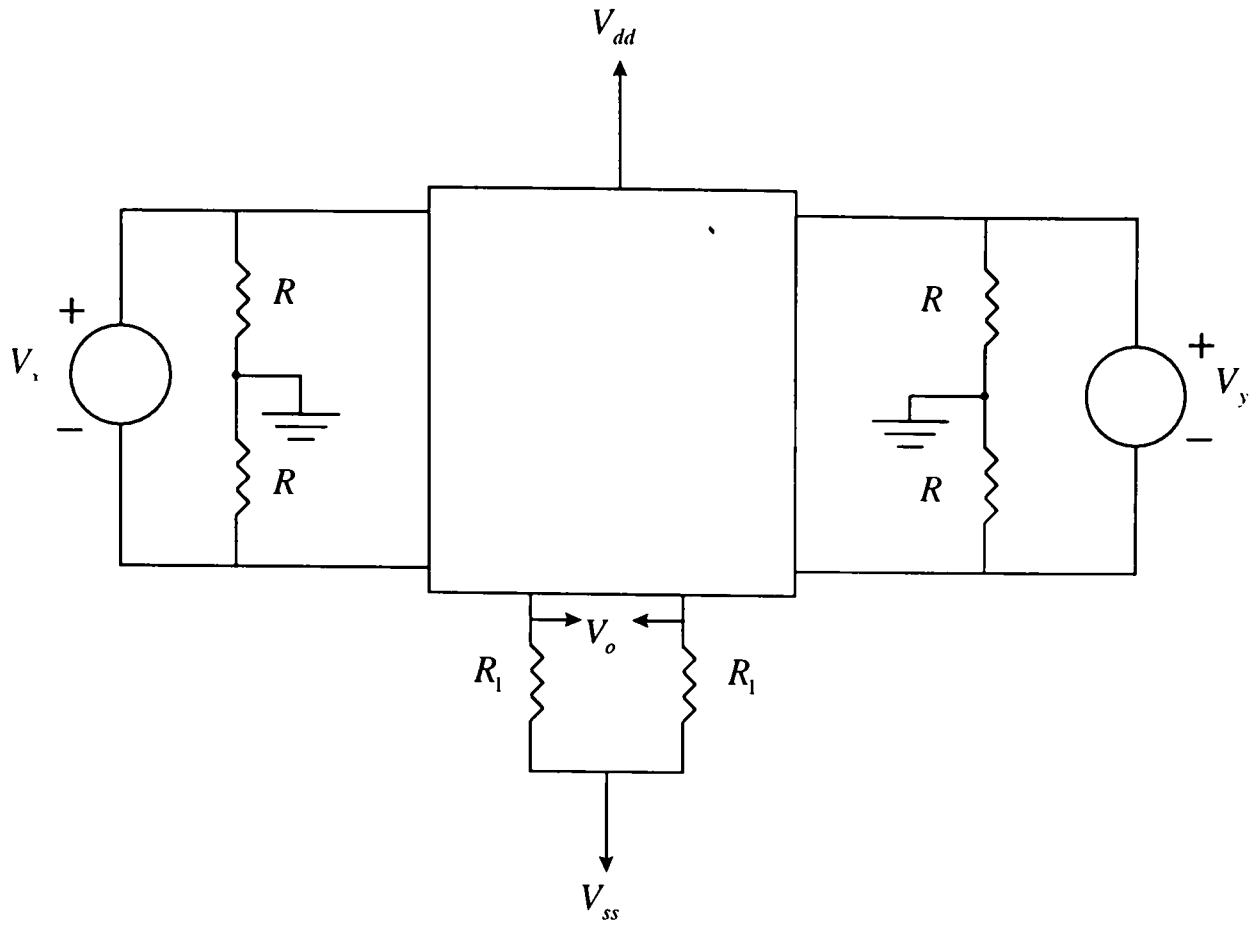


Figure 4-13. Simulation Circuit For The Multiplier Cell

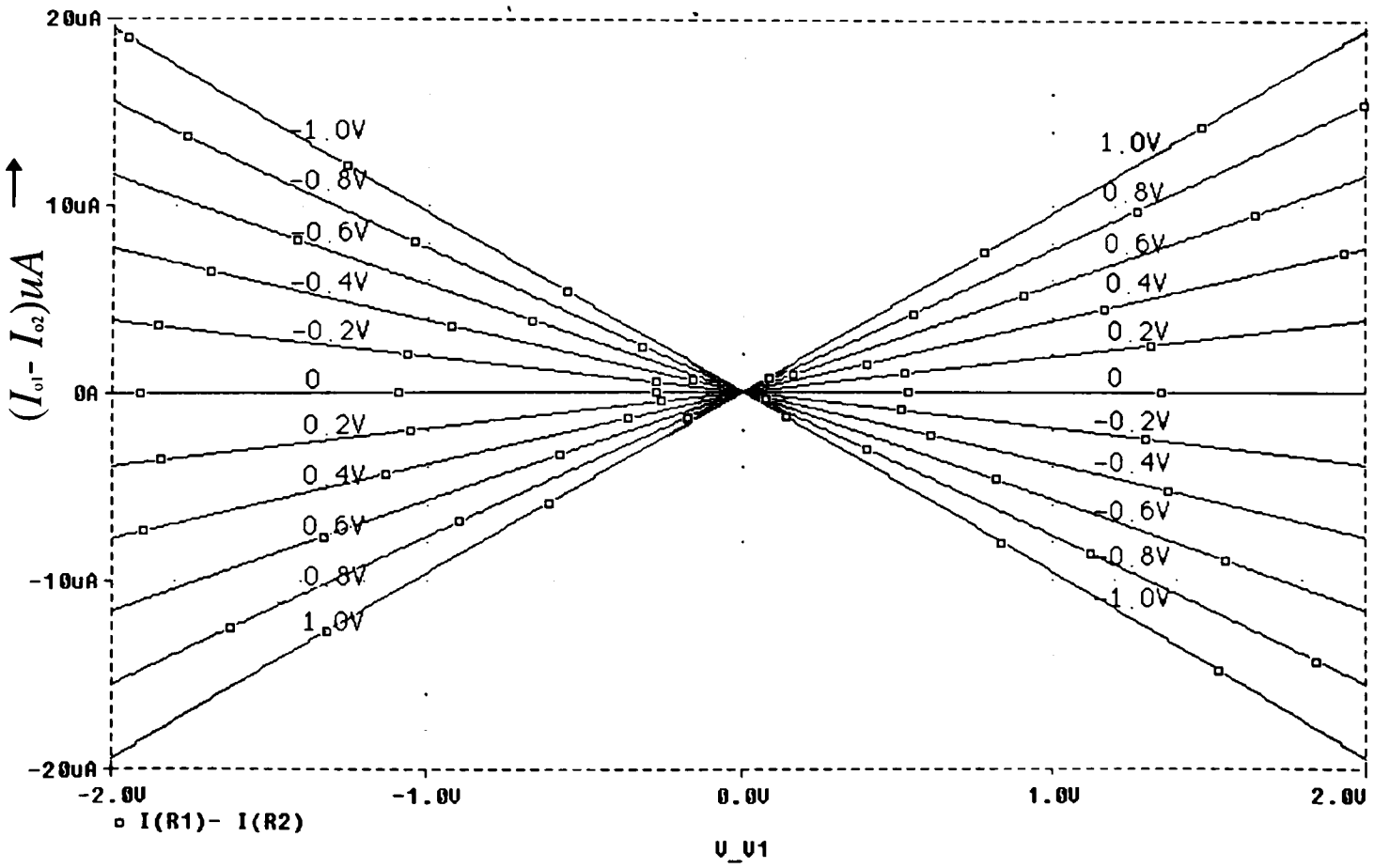
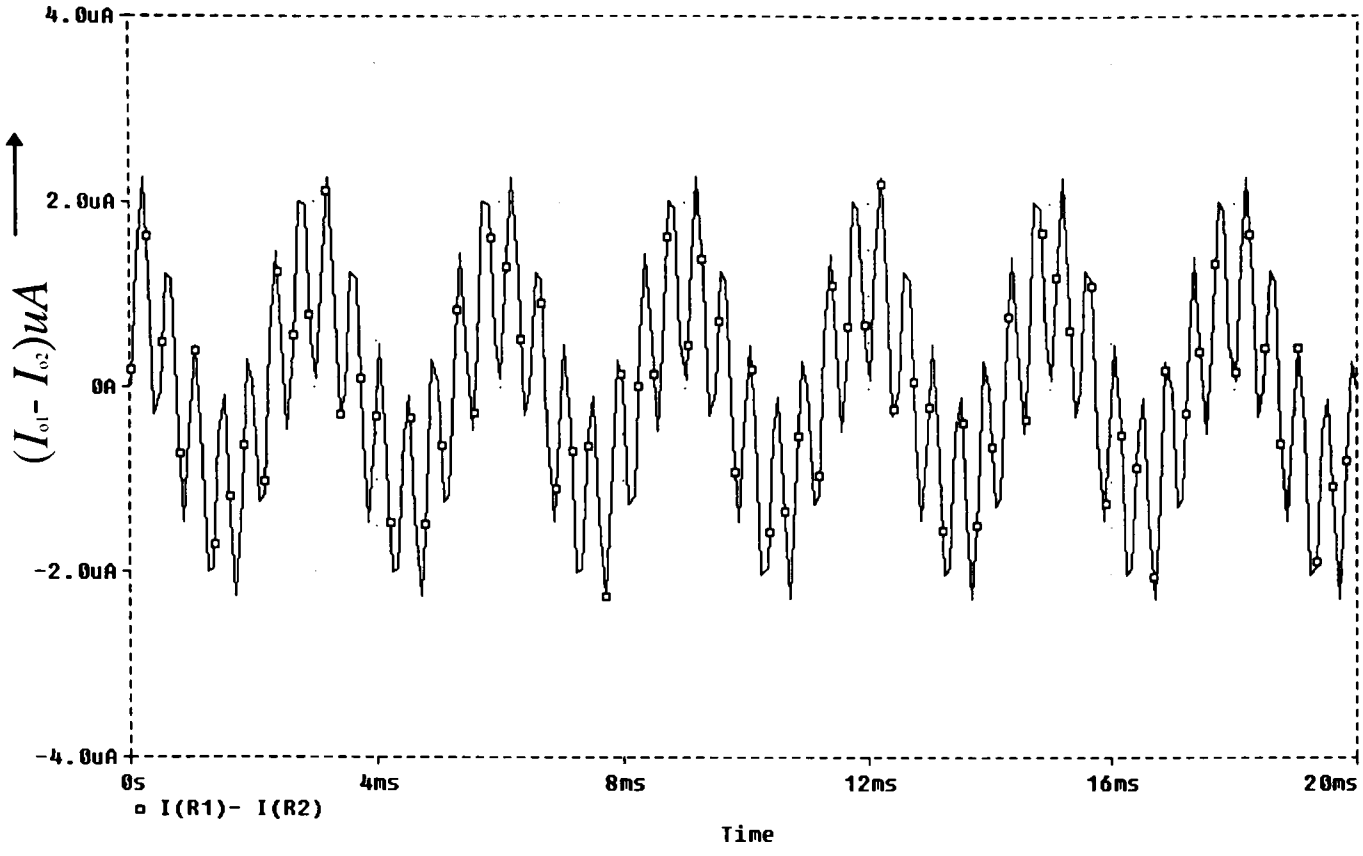
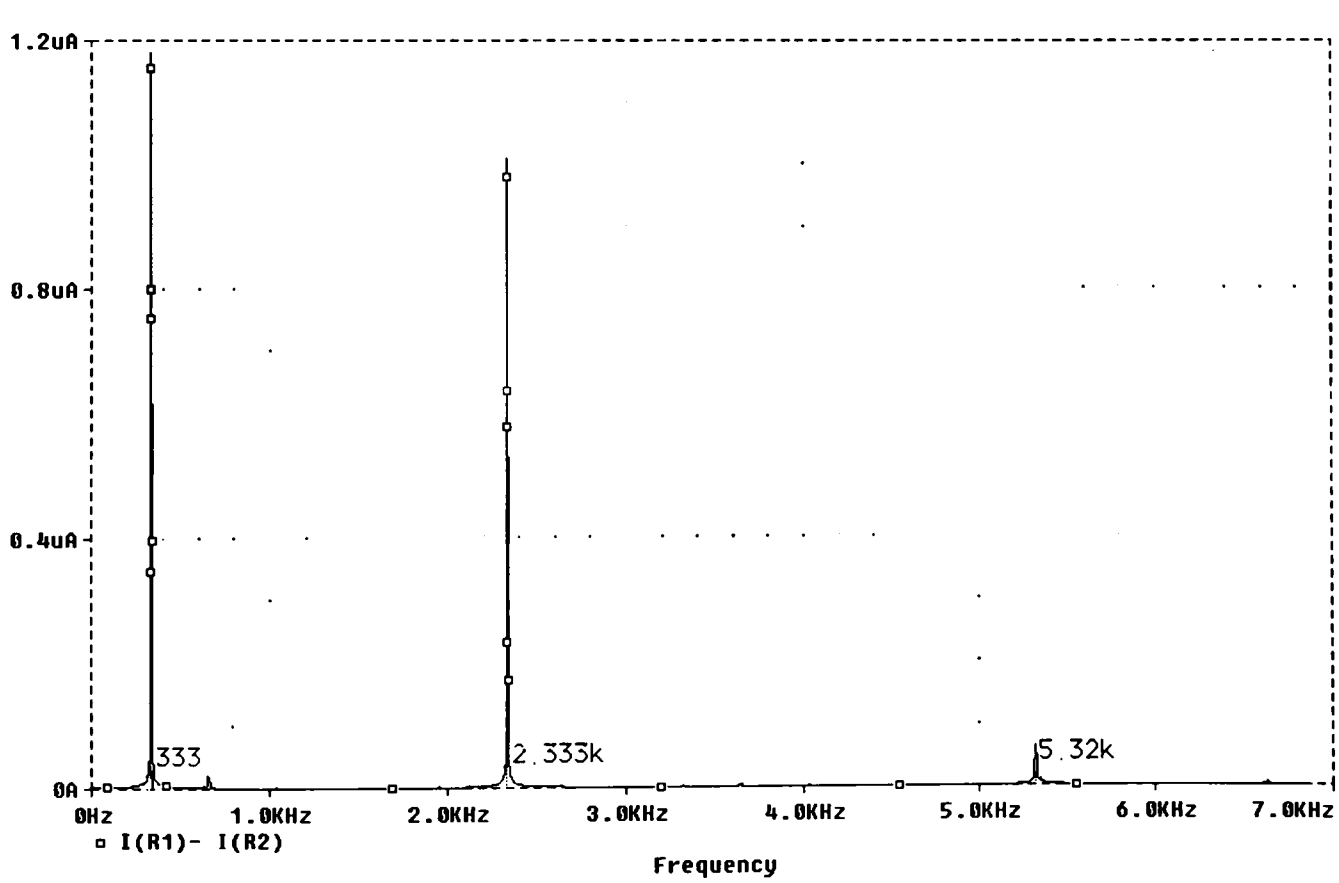


Figure 4-14. DC sweep on the Multiplier Inputs

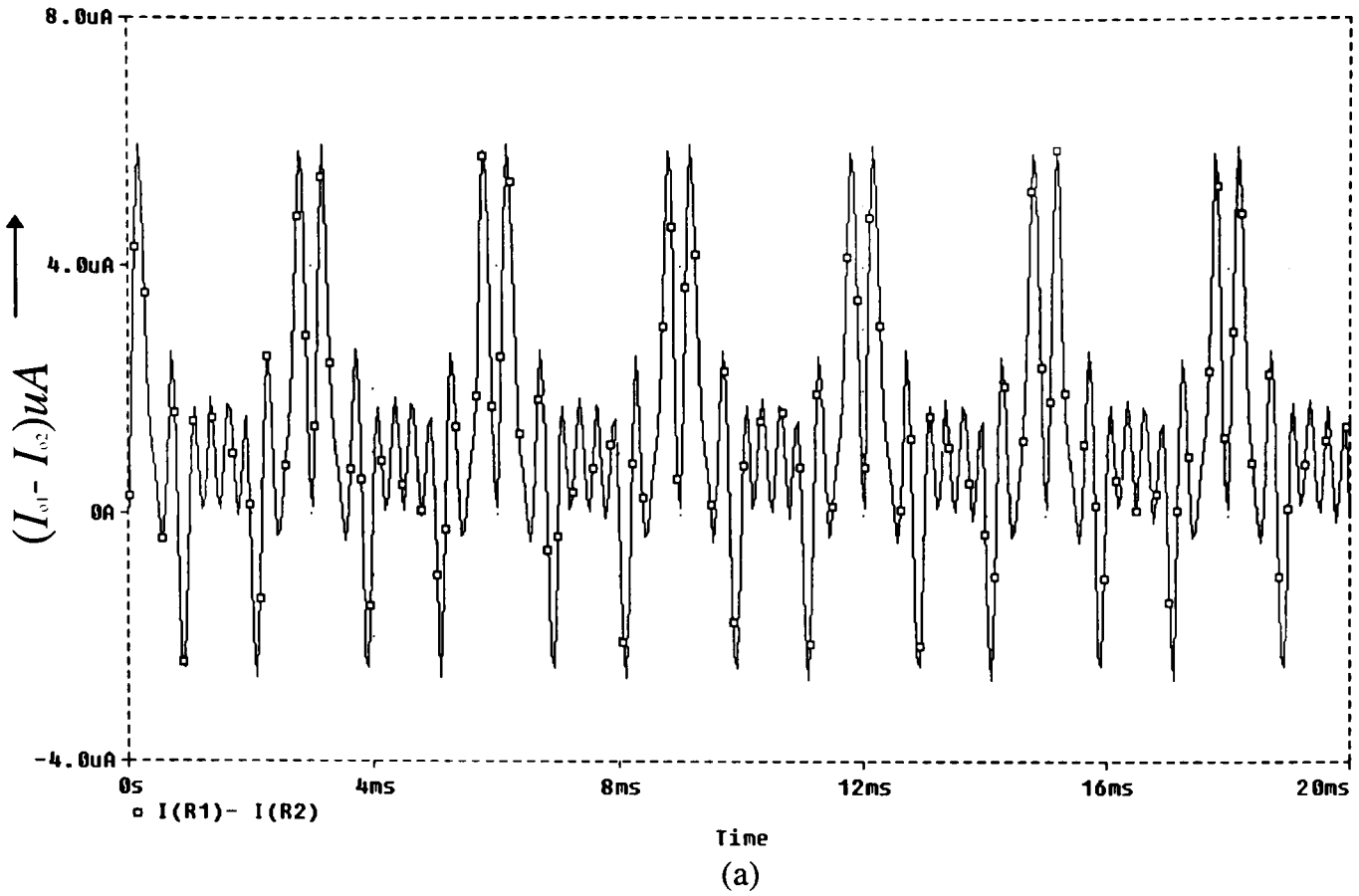


(a)

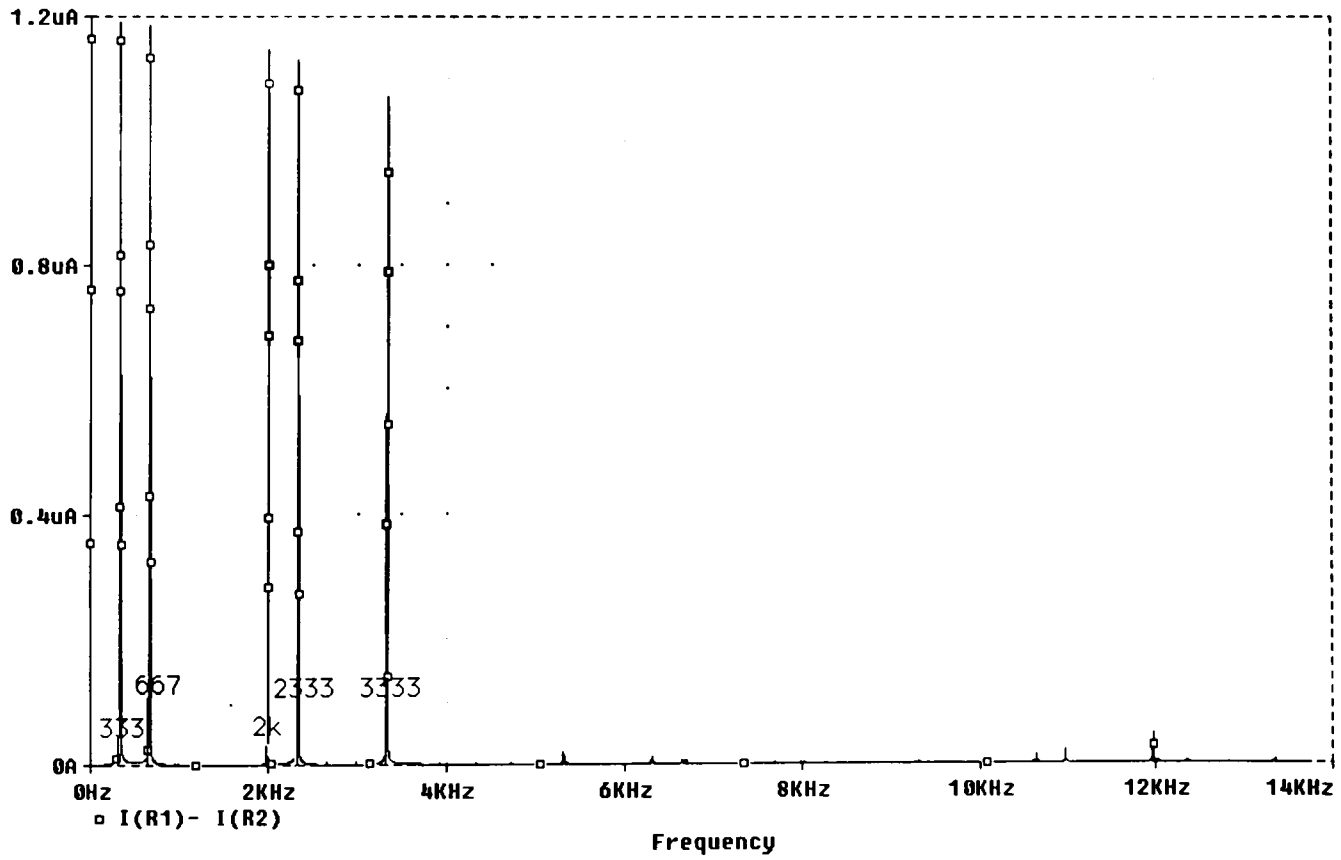


(b)

Figure 4-15. Transient Analysis of the Multiplier Cell: (a) Mixer Output For V_x = 0.5V 1kHz and V_y = 0.5V 1.333kHz and (b) Fourier Transform of the Mixer Output in Figure 4-15(a)



(a)



(b)

Figure 4-16. Transient Analysis of the Multiplier Cell: (a) Mixer Output for V_x = 0.5V(1kHz + 1.333kHz + 333Hz + 2.333kHz) and V_y = 0.5V 1kHz and (b) Fourier Transform of the Mixer Output in Figure 4-16(a)

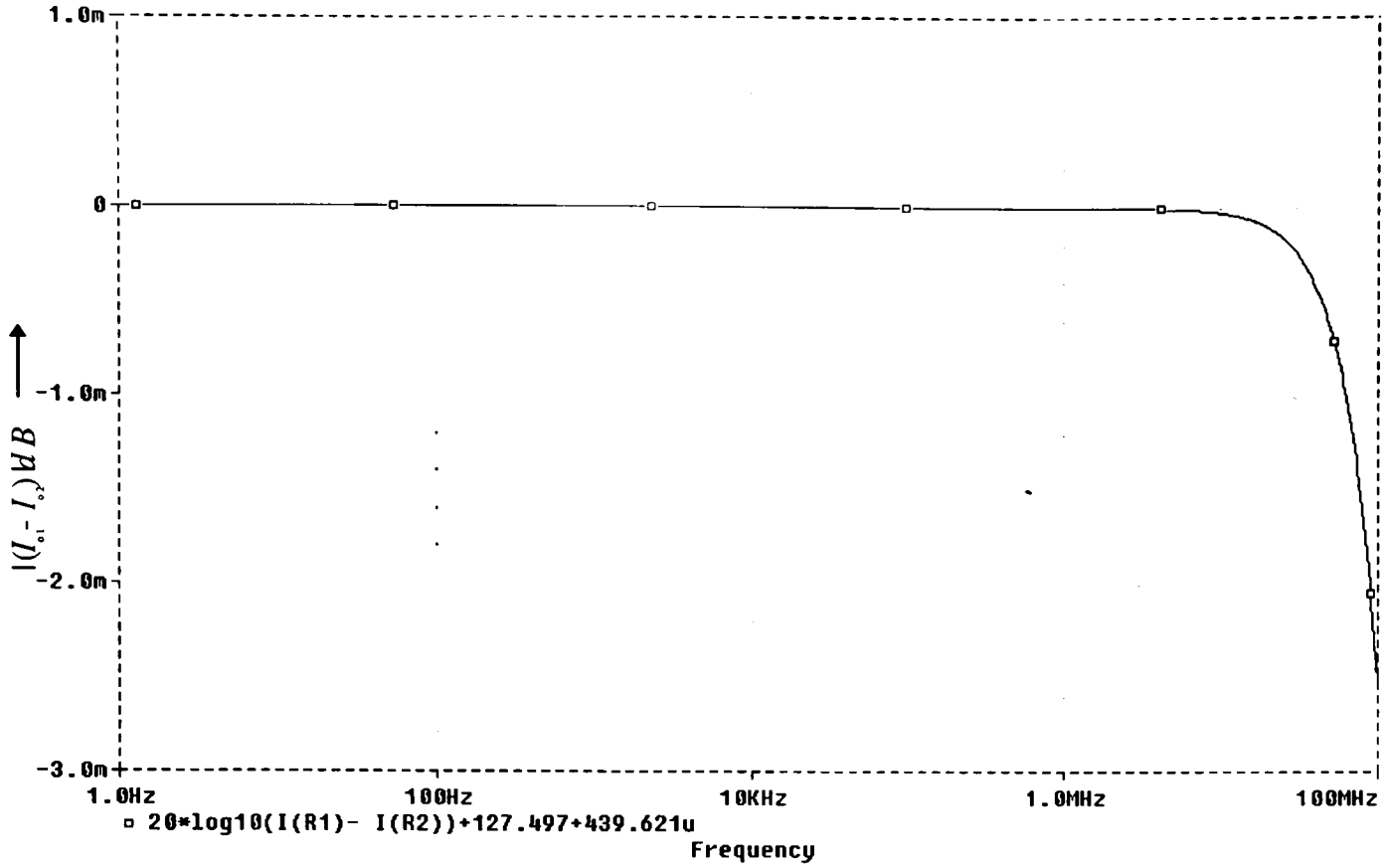
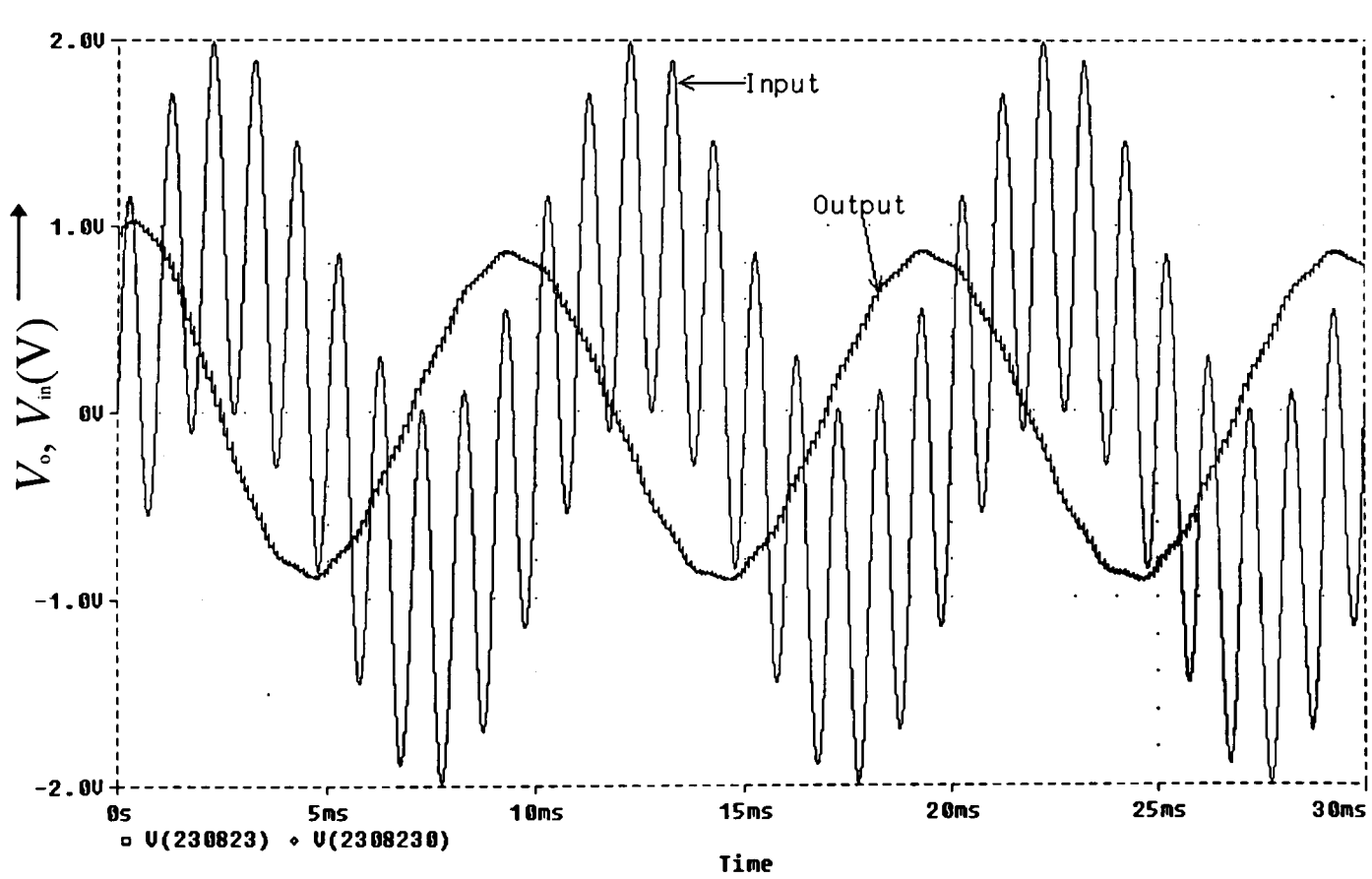
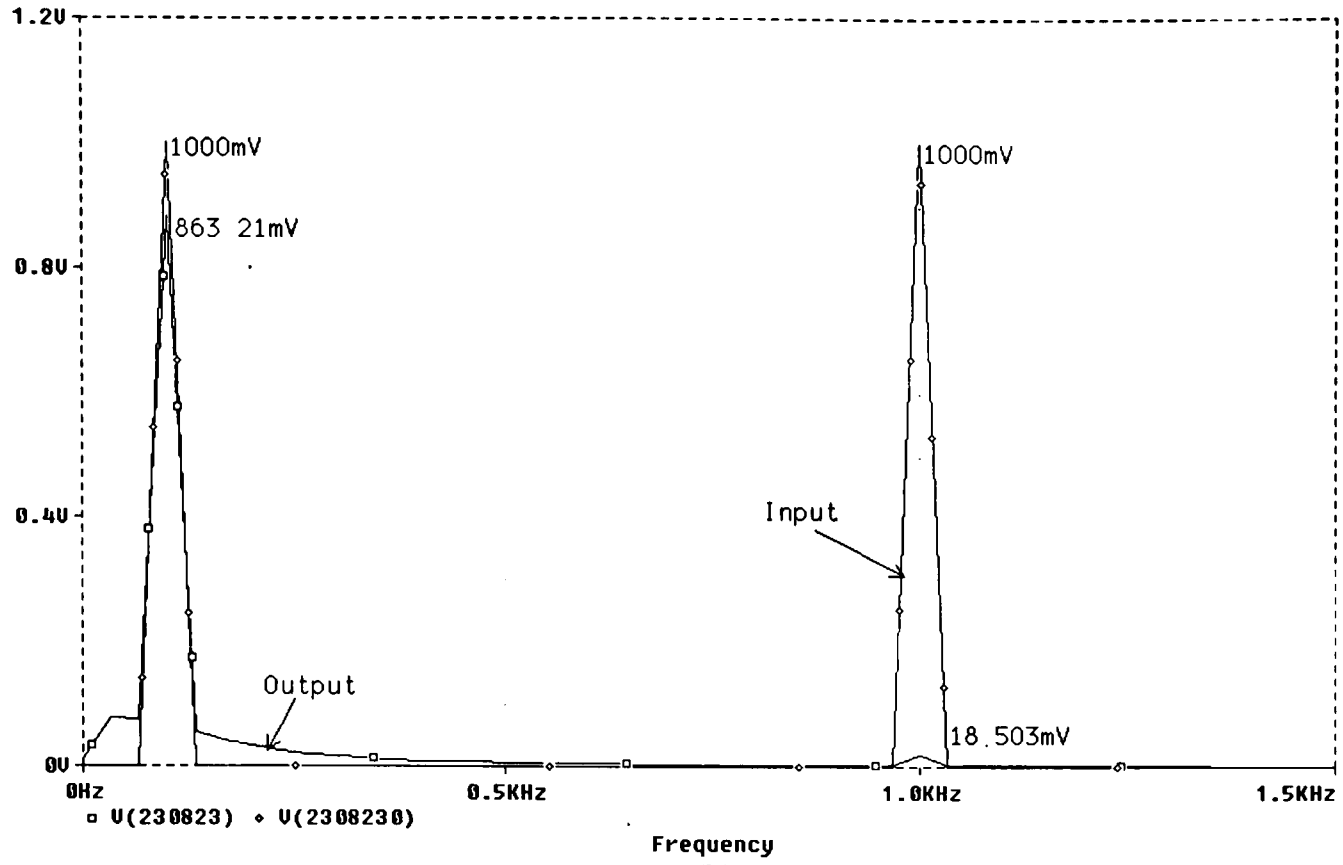


Figure 4-17. Frequency Response of the Multiplier Cell



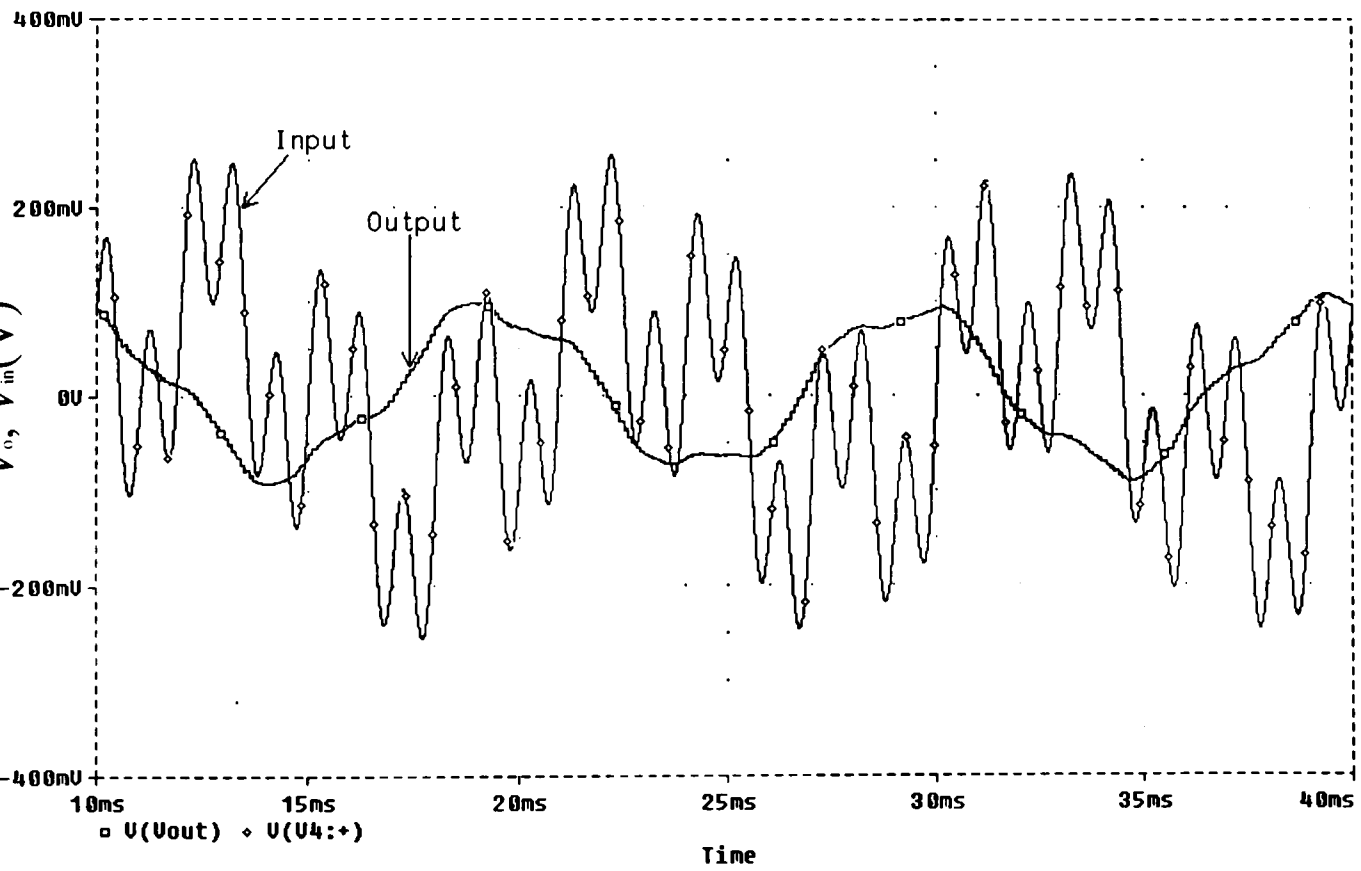
(a)

Figure 4-18. Transient Analysis of the SC Filter: (a) Extracted SC Filter Output for 100mV 100Hz and 1kHz input and (b) Fourier Transform of the SC Filter O/P, I/P plotted in Figure 4-18(a)



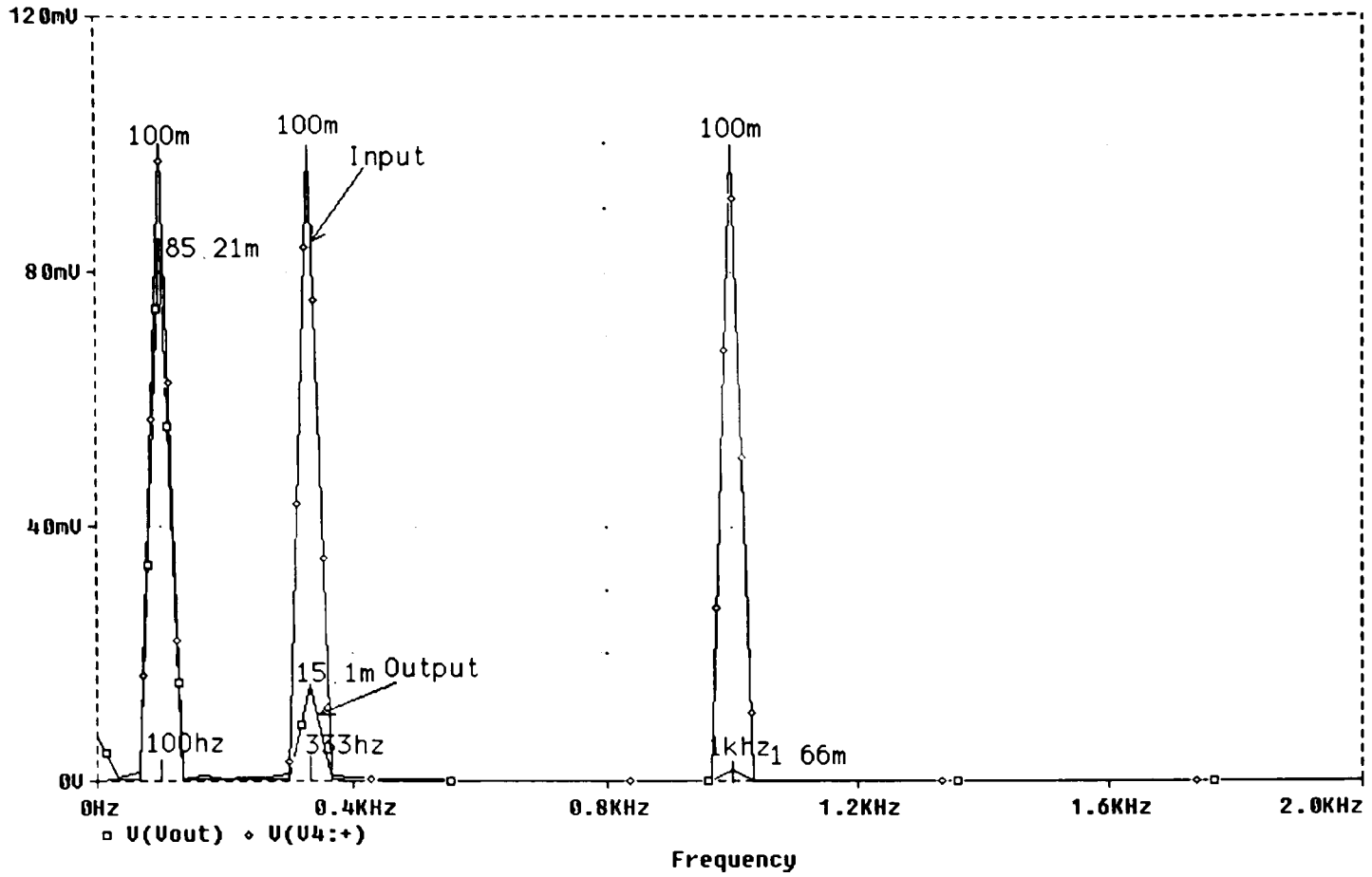
(b)

Figure 4-18 continued.



(a)

Figure 4-19. Transient Response of the SC Filter: (a) Designed SC-Filter O/P for 100mV 100Hz, 333Hz and 1kHz I/P and (b) Fourier Transform of the Filter O/P, I/P shown in Figure 4-19(a)



(b)

Figure 4-19 continued.

CHAPTER 5

CONCLUSIONS

In this work, we have presented the design of a 2-D VLSI optical sensor array, with on-chip circuitry to perform temporal electronic heterodyne detection on a pixel-by-pixel basis. Integration of image sensors with circuitry for driving the image sensor and performing on-chip signal processing is becoming increasingly popular for a multitude of signal processing applications. The need for heterodyne detector arrays in acousto-optics has been emphasized by prominent researchers in the field.[1] Such heterodyne detector arrays can have potentially numerous applications, like real time extraction of directional spatial derivatives of images, spatial filtering, contour tracing, simple imaging, etc., to name a few. Besides, a high degree of on-chip signal processing helps enable miniaturization of instrument systems and simplification of system interfaces.

We have demonstrated the feasibility of 2-D heterodyne detector arrays and have discussed several potential applications of the detector array; with a detailed analysis on the applicability of the 2-D detector array in a spatio-temporal system, with the ability to extract arbitrary order 2-D spatial derivatives of images. Simulation results of the system using representative elementary 1-D and 2-D intensity functions have been given. A possible architecture of the 2-D detector array has been presented. Detailed VLSI design of the circuit blocks comprising a single heterodyne detector element has also been discussed.

With the advancement of the VLSI processes and reduction of feature sizes to sub-micron dimensions (which are already available for digital designers) for analog processes, a high density of such heterodyne detectors can be fabricated on a single chip. We envision the use of such a heterodyne detector array in real-time applications, like imaging cameras. The on-chip heterodyne detection feature of the detector array can help implement different image enhancement operations like spatial filtering. Since most image compression algorithms extract the high frequency content from the images, which essentially resides in the image edges, and selectively truncate the high frequency content, depending on the required image resolution, we believe that with slight modification, the 2-D heterodyne detector array can potentially be used to implement image compression algorithms in real time..

Heterodyne detection techniques are well known to enhance the dynamic range and signal to noise ratio as compared to base band detection schemes. This feature of the detector array can be put to good use in numerous optical imaging applications. By modulating the information of interest to a higher carrier frequency (e.g., by using acousto-optic modulators), heterodyning techniques can be put to good use to eliminate low frequency noise. These techniques are typically implemented using a photo-diode in conjunction with a lock-in amplifier. We believe that the availability of a 2-D heterodyne detector array would simplify the design of such systems and the parallel architecture of the array could in specific situations reduce the data-acquisition time.

Spectral hole burning memories offer unprecedented storage densities, but are potentially limited from realizing their full potential by diffraction effects. Techniques

like wavelength division multiplexing and recording the temporal Fourier transform of the encoded data[6-8] have been used to overcome this problem, but these have their own limitations. An effective approach,[6] which better exploits the full storage density of the material while retaining fast I/O rates, uses a hybrid time-frequency domain approach, in which temporal chirps are imposed on the write beam to broaden its spectral bandwidth. Upon readout, the material renders the temporally encoded data modulated on the chirp carrier. Thus heterodyne detection is required for extracting the data stream, which can be very easily done by the 2-D detector array we have proposed.

We only had the option of selecting one of the analog VLSI CMOS processes provided by the MOSIS foundry. These processes are not typically optimized for the fabrication of photodetectors. This was one of the bottlenecks in our design. But this problem can be solved by using processes specifically suited to the fabrication of opto-electronic sensors.

We have presented a very general circuit level realization of the heterodyne detector element. Depending upon the application, other circuit topologies, favorable to high density integration of the detector array could potentially be investigated. Current multiplier circuits[30] using MOS current squaring circuits could combine the buffering and the mixing operations into one. A major reduction in area can be effected by the use of multiplexed switched capacitor filters, for each row of detectors, but at the cost of reduced processing speed and increased system complexity. A time division multiplexed switched capacitor filter has been presented in ref[31].

Finally 2-D heterodyne detector arrays with fast response times could be implemented using the SEED (Self Electro-Optic Devices) diode arrays. Such arrays are fabricated by AT&T. The heterodyne detection circuitry can be designed in a typical analog VLSI process. The SEED diode array can be flip-chip bonded to the heterodyne detection circuitry using a PGA (pin grid array) package for the detection circuitry.

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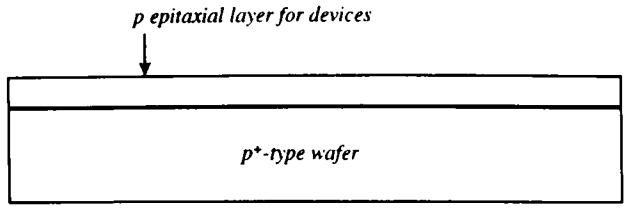
APPENDIX A
VLSI CMOS FABRICATION SEQUENCE

In this section, we would like to provide a general introduction to the VLSI CMOS fabrication sequence[28] for the novice reader. The discussion is quite introductory, for details the interested reader can refer to [27,28,15]. The typical process layers in a n-well process are given below:

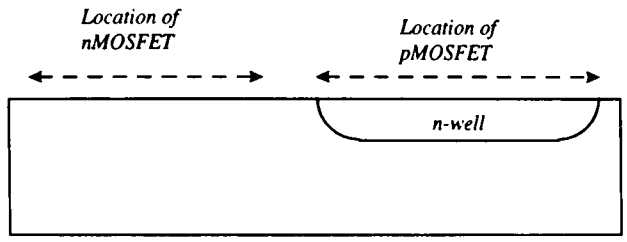
- p-substrate
- n-well
- p^+ diffusion
- n^+ diffusion
- gate oxide
- polysilicon(some processes have two layers of polysilicon denoted as poly and poly-2)
- CVD(Chemical Vapor Deposition) Oxide
- Metal(some processes have two layers of metal denoted as metal-1 and metal-2)

Integrated circuit layout drawings represent the surface patterns of the layers that make up the chip. Both the geometrical and electrical characteristics of the structure rely on the details of the processing sequence. In this section we will examine the basic sequence for a typical n-well CMOS process. The starting point in the process is a p-type wafer.

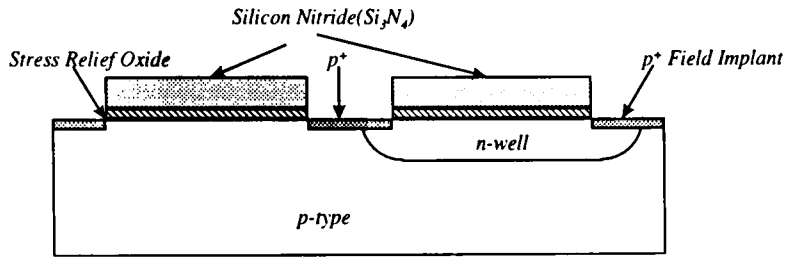
1. Epitaxial Growth: A thin layer of p-type epitaxial silicon is grown on the wafer. This is shown in Figure A-1(a). The epitaxial layer is used as the base layer for building



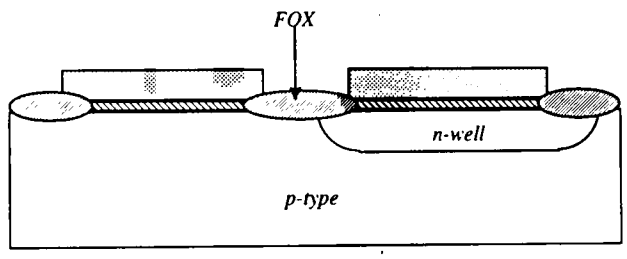
(a): Epitaxial layer Growth



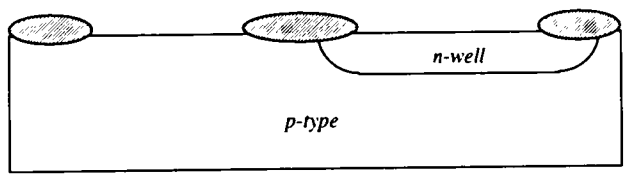
(b): MOSFET placement



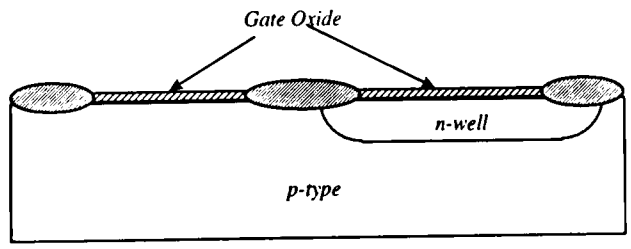
(c): Active Area definition



(d): FOX Growth

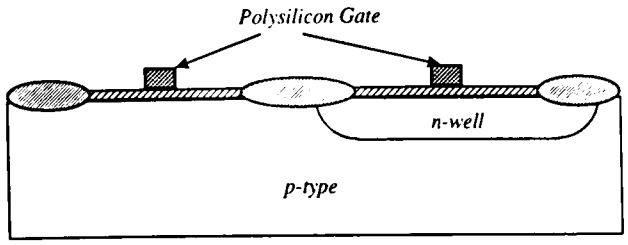


(e): After removal of nitride and stress relief oxide

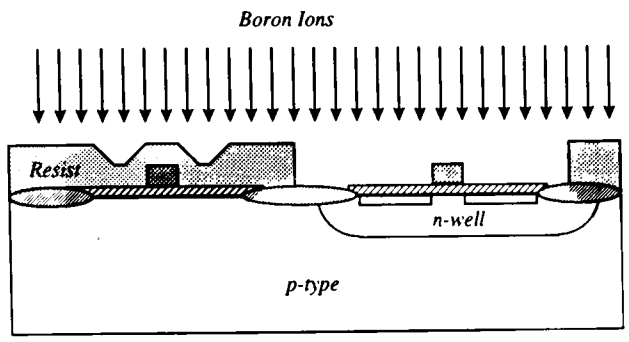


(f): Gate oxide growth

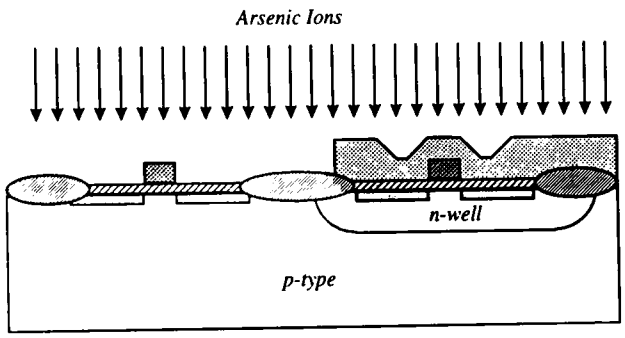
Figure A-1. (a)-(k): VLSI CMOS Fabrication Sequence



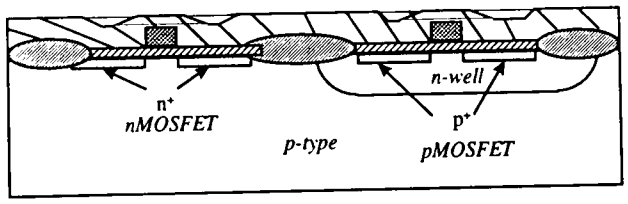
(g): Poly deposition and patterning



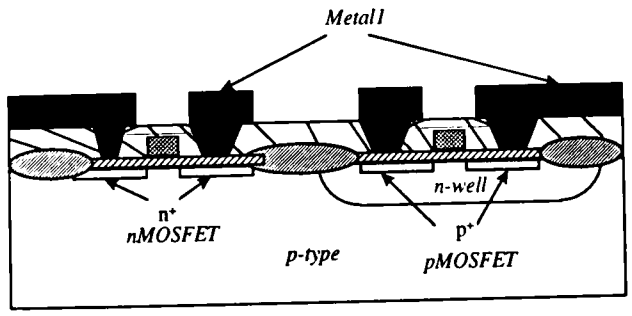
(h): Boron p^+ implant



(i): Arsenic n^+ implant



(j): CVD oxide



(k): After metal-1 deposition and patterning

Figure A-1 continued.

devices. In the remaining cross-sectional drawings (not drawn to scale), only the epitaxial layer would be shown.

2. n-Well Formation: In CMOS, the p-channel MOSFETs must reside in an n-type background. These are obtained by adding an n-well as shown in Figure A1-b, to accommodate the pMOSFETs. Electrically, the n-well region must be biased to the highest potential in the circuit, to reverse bias the parasitic diodes that are formed between the p^+ drain/source regions of the pFET and the n-well. For simplicity, in the cross-sections depicted, we have not shown contacts to the n-well.
3. Active Area Definition and Isolation: Since the transistor density in a VLSI design can be quite high, one needs to be concerned about the isolation of a device from its neighbors. Properly isolated transistors do not exhibit any direct conduction paths to any other devices, except for those that have been explicitly included through other layers. In this step of fabrication sequence, the location of every transistor is defined; isolation is achieved by the next oxide growth.

An *active area* is a planar section of the surface where the transistors are placed. Field regions surround the active areas, and constitute the majority of the surface area. The active areas are defined by patterned layers of silicon nitride (Si_3N_4), which is deposited onto a thin oxide layer (SiO_2) on the silicon surface. The SiO_2 layer is also known as the stress-relief oxide, and is used as a mechanical buffer between the nitride layer and the silicon. The cross-sectional view of the wafer at this point is shown in Figure A1-(c). We also note that a p^+ field implant is used to enhance isolation. The field implant is not explicitly shown in the remaining drawings.

The silicon nitride layer is used in the next step known as the local oxidation of silicon (LOCOS). Exposing the surface of the wafer to a flow of oxygen-rich gas induces the growth of silicon dioxide in the field regions where the silicon surface is exposed, i.e., the field regions. In contrast, areas that are covered with silicon nitride do not get oxidized. Since the growth of silicon dioxide requires silicon atoms from the substrate, the resulting field oxide (FOX) is recessed into the surface as shown in Figure A-1(d).

4. Gate Oxide Growth: After the field oxide growth is completed, the nitride and the stress relief oxide are removed. In this step the critical gate oxide, which serves as the dielectric between the polysilicon gate and the MOSFET channel is grown. These steps are shown in Figures A-1(e) and A-1(f).

5. Polysilicon Deposition and Patterning: A layer of polysilicon ('poly') is deposited over the entire surface and then patterned by a lithography sequence. All of the MOSFET gates are defined by this step. This is illustrated in Figures A-1(g) and (h). The polysilicon may be doped *in situ*. This lowers the parasitic resistance.

6. p-FET Formation: The formation of p-channel MOSFETs is accomplished during the next step. Photoresist is applied and patterned so that it covers all but the location of the p^+ regions. Subjecting the wafer surface to an ion beam comprising boron ions creates the p^+ drain and source regions of the pFETs, as shown in Figure A-1(i). Accurate placement of these areas is achieved by using a self-aligned approach in which the polysilicon gate acts as a barrier for the underlying channel area.

7. n-FET Formation: Another lithographic sequence is used to define all nFETs. Donors (such as arsenic) are ion-implanted to dope the n^+ drain and source regions in the self-aligned transistors as shown in Figure A-1(j).

8. Metal-1: The entire wafer is next coated with CVD (Chemical Vapor deposition) oxide. Contact cuts are patterned to provide matal-1 to active and metal-1 to poly electrical connections. This is shown in Figure A-1(j). A metal-1 layer is then applied and patterned resulting in the structure shown in Figure A-1(k).

If the process has a second metal layer (metal-2), then subsequent steps involve deposition of another layer of oxide, defining vias for connection to the underlying metal-1, followed by the deposition of metal-2 and its subsequent patterning. The final step is to add a protective layer over the surface. Typically, this consists of another layer of silicon dioxide followed by a layer of silicon nitride; the nitride is used because it acts as a good diffusion barrier against contaminants. Contact cuts in the overglass layer are required to access the input/output pads on the final metal layer.

APPENDIX B

PSPICE® LEVEL 2 SIMULATION PARAMETERS

FOR THE MOSIS 2.0μ N-WELL PROCESS

In this section we list the process parameters, which we used for the design of the circuit blocks constituting a heterodyne detector element. These are level 2 parameters for Pspice® simulations for the MOS transistors. First, we will list the different parameters and then provide their values, which we obtained directly from MOSIS. For the details of the level 2 model for the MOS transistor, the interested reader can look up reference[29]. The different parameters are:

- TOX is the gate oxide thickness in meters;
- KP represents the process transconductance in units of [A/V^2];
- VTO is the threshold voltage (in V) for zero bulk-source potential;
- GAMMA is the body bias coefficient;
- PHI is the bulk Fermi potential $2|\phi_F|$ in V;
- NSUB is the substrate doping for the MOSFET;
- LD is the lateral diffusion length;
- CJ is the zero bias bottom depletion capacitance in units of [F/m^2];
- CJSW is the zero-bias sidewall capacitance in units of [F/m];
- MJ is the bottom grading coefficient;
- MJSW is the sidewall grading coefficient;
- PB is the bulk junction potential;

- Lambda is the channel length modulation factor;
- UO is the surface mobility at low gate voltages;
- UEXP is the critical field exponent for the empirical formula which characterizes the degradation of surface mobility[28];
- UCRIT is the critical field for mobility degradation;
- DELTA is the channel width factor;
- VMAX is the maximum drift velocity of carriers;
- XJ is the metallurgical junction depth;
- NFS is the effective fast surface state density;
- NEFF is the total channel charge coefficient;
- TPG is the type of gate;
- RSH is the sheet resistance of the drain and source diffusions;
- CGDO is the gate-drain overlap capacitance per meter channel width;
- CGSO is the gate-source overlap capacitance per meter channel width;
- CGBO is the gate-bulk overlap capacitance per meter channel width;

nMOSFET Process Parameters:

PHI=0.700000; TOX=3.6500E-08; XJ=0.200000U; TPG=1; VTO=0.7685; DELTA=5.0470E+00; LD=2.0130E-07; KP=6.8789E-05; UO=727.1; UEXP=1.1310E-01; UCRIT=9.5480E+03; RSH=1.1000E-01; GAMMA=0.4763; NSUB=6.1170E+15; NFS=9.2910E+10; VMAX=5.2090E+04; LAMBDA=3.2020E-02; CGDO=2.8566E-10; CGSO=2.8566E-10; CGBO=3.4631E-10; CJ=1.27E-04; MJ=0.724; CJSW=5.45E-10; MJSW=0.233 PB=0.65.

pMOSFET Process Parameters:
PHI=0.700000; TOX=3.6500E-08; XJ=0.200000U; TPG=-1;VTO=-0.8758; DELTA=2.8890E+00; LD=1.5770E-07; KP=1.8344E-05; UO=193.9; UEXP=3.2390E-

01; UCRIT=1.2630E+05; RSH=9.0910E-02; GAMMA=0.6471; NSUB=1.1290E+16; NFS=5.9090E+11; VMAX=9.9990E+05; LAMBDA=4.5590E-02; CGDO=2.2379E-10; CGSO=2.2379E-10; CGBO=4.1468E-10; CJ=3.20E-04; MJ=0.602; CJSW=3.86E-10; MJSW=0.164 PB=0.90

APPENDIX C

MATLAB™ CODE

Case I : 1-D Spatial Intensity Function

```
%*************************************************************************
%                              Code Listing
%*************************************************************************
clear all;
x=-2.2:0.01:2.2;(% Defining the coordinates of the 1-D Heterodyne Detectors).
[n,w]=buttord(100/5000,1/5,0.1,35); % Obtaining the order of the Butterworth Filter.
[b,a]=butter(n,w); % Obtaining the Butterworth Transfer Function for the filter.
f1=((1./(1+exp(-20*(x+0.5))))-(1./(1+exp(-20*(x-0.5))))); % 1-D Spatial Intensity
%Function- a pulse with sigmoid edges.
figure(1); % Opening a figure window
plot(x,f1,'b');% Plotting the 1-D Spatial intensity function.
t=0:1/(10000):20/1000;% Defining the time vector so that there are at least 20 cycles of
% sinusoidal perturbations.
Ax=(0.01/2)*cos(2*pi*1000*t);% X-perturbation frequency component-note that the
% maximum perturbation amplitude is half the detector spacing.
count=0;% Initializing loop variable.
% Functioning of the loop- Corresponding to each detector coordinate we generate a
%vector(g) which is the coordinates of the points resulting from the sinusoidal
```

```
%perturbation around the detector mean position. We next generate another vector(f2)
%which is the spatial intensity magnitude corresponding to the vector generated above.
%Next, comes the mixing phase which is the scalar product of f2 and Ax-the sinusoidal
%perturbation vector; f4 is the filtered vector. A vector f5 holds the steady state filter
%output for each f4 generated and corresponds to the first-order spatial derivative of the
%spatial intensity function.
for x=-2.2:0.01:2.2
count=count+1;
g=x*ones(size(t))+Ax;% For detector coordinate 'x' g corresponds to the sinusoidal
%perturbation around 'x'.
f2=((1./(1+exp(-20*(g+0.5))))-(1./(1+exp(-20*(g-0.5)))));
f3=f2.*Ax;% Mixing operation.
f4=filter(b,a,f3);% Filtering operation, steady state output of f4 is the derivative
%information at the detector coordinate x.
f5(count)=f4(200);% holds the derivative information for each detector coordinate 'x'.
end;
x=-2.2:0.01:2.2;% Generating detector coordinates again for plotting figures.
hold on;
plot(x,f5/max(abs(f5)),'b-.');% Plotting the normalized spatial derivative.
```

Case II: 2-D Spatial Intensity Function(2 x 2 checker board pattern)

```
%*****************************************************************
%                          Code Listing
%*****************************************************************
clear all
[n,w]=buttord(100/5000,1/5,0.1,35);% determining the order of the Butterworth Filter.
[b,a]=butter(n,w);% Generating the Butterworth Filter Transfer Function.
x=-2.2:0.05:2.2;% Defining a 1-D detector array coordinate vector.
[X1,Y1]=meshgrid(x,x);% Generating the 2-D Heterodyne detector array coordinates.
f1=[];% Initializing f1 and f2 as matrices to accelerate program execution.
f2=[];
t=0:1/10000:20/1000;% Generating the time vector to include at least 20 cycles of
%sinusoidal perturbations.
dx=(0.05/2)*cos(2*pi*1000*t);% X-perturbation frequency.
dy=(0.05/2)*cos(2*pi*1333*t);% Y-perturbation frequency.
count1=0;% Initializing loop variables count1 and count2.
count2=0;
% The 2-D loop is a simple extension of the 1-D loop described earlier; for each detector
%coordinate the sinusoidally perturbed x-y coordinates are generated; the 2-D intensity
%function is evaluated; its dot product with dx(v_ref for df/dx) or dy(v_ref for df/dy) is the
%mixing operation, and finally the steady state filtered output is stored in the 2-D vector
```

```
%F6 at the coordinates corresponding to the detector coordinate. F6 is the extracted
%spatial derivative information for the 2-D intensity function.
for y=-2.2:0.05:2.2
        count2=count2+1
        count1=0;
        for x=-2.2:0.05:2.2
                count1=count1+1;
                X=x*ones(size(t))+dx; %(x-y coordinates for the sinusoidal perturbation
                %corresponding to detector coordinate(x,y).
                Y=y*ones(size(t))+dy;
                f1=((1./(1+exp(-20*(X+1))))-(1./(1+exp(-20*(X)))));
                f2=(-(1./(1+exp(-20*(Y-1))))+(1./(1+exp(-20*(Y)))));
                F1=f1.*f2;
                f11=((1./(1+exp(-20*(X))))-(1./(1+exp(-20*(X-1)))));
                f22=(-(1./(1+exp(-20*(Y))))+(1./(1+exp(-20*(Y+1)))));
                F2=f11.*f22;
                F3=F1+F2;
                F4=F3.*(10*dx);% Mixing Operation.
                F5=filter(b,a,F4);% Filtering Operation.
                F6(count1,count2)=F5(1,200);% Output derivative information stored in
                %F6 corresponding to the detector location.
end;end;
```

```
% Generating the 2-D intensity function for plotting.

G1=((1./(1+exp(-20*(X+1))))-(1./(1+exp(-20*(X)))));

G2=(-(1./(1+exp(-20*(Y-1))))+(1./(1+exp(-20*(Y)))));

Go=G1+G2;% 2-D Intensity transmittance function.


% Plotting the 2-D intensity function.

Figure(1);

mesh(x,x,Go);

axis('square');

axis([-2.2 2.2 -2.2 2.2 -1 1]);


% Plotting the normalized Spatial derivative.

Figure(2);

mesh(x,x,F6/max(abs(F6)));

axis('square');

axis([-2.2 2.2 -2.2 2.2 -1 1]);
```

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