Transient Analysis of Silicon Carbide Power MOSFET

by

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ABSTRACT

This thesis illustrates the transient performance of Silicon carbide (4H-SiC) Power MOSFET. Transient analysis enables the designer to understand the thermal stress the semiconductor device undergoes while dissipating high power for short period of time. Silicon carbide has been a material of interest in the development of High Power Semiconductor devices especially due to its wide band gap and high temperature operational stability. This research focuses on the transient performance of vertical D-MOSFET structure at room temperature and elevated ambient temperature conditions. The 2D device model was created and simulated using Silvaco© ATLAS Technology Computer-Aided Design (TCAD) physics-based simulation software. Physics-based models were included to accurately model electrical device parameters like mobility, impact ionization, Lattice heating etc.. Orcad PSPICE student version and B2 SPICE A/D V4 LITE simulation tools were also used to verify the circuits before simulating it via Silvaco. In order to aid the research on MOSFET, a parallel plane Silicon Carbide PIN diode was first designed and simulated for its DC characteristics.

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CHAPTER 1

OVERVIEW OF SILICON CARBIDE TECHNOLOGY

Silicon carbide is a compound of Silicon (Si) and Carbon with a chemical formula SiC. Silicon Carbide was discovered back in 1824 but it wasn't until 1989 that Silicon Carbide (SiC) technology was mature enough to be used as a Semiconductor material [1]. SiC has several desirable properties for many electronic applications especially in the field of power electronics. These desirable properties are primarily due to its wide energy band-gap, Critical Electric Field and Thermal Conductivity. Table 1 gives a comparison of important electronic properties of SiC with respect to Si and Gallium Nitride (GaN). Data Compiled from references [2, 3, 4, 5, 6].

Table 1. Silicon Carbide compared with Silicon and Gallium Nitride

Property @ 300K	Silicon (Si)	Gallium Nitride (GaN)	Silicon Carbide (3C-SiC)	Silicon Carbide (4H-SiC)	Silicon Carbide (6H-SiC)
Bandgap (eV)	1.12	3.4	2.3	3.26	3.03
Relative Dielectric Constant	11.9	9.7	9.7	9.7	9.7
Critical Electric Field @ $N_D=10^{17}$ cm^{-3} (MV/cm)	0.6	3.3	1.8	∥ c-axis = 3.0 ⊥ c-axis = 2.5	∥ c-axis = 3.2 ⊥ c-axis > 1.0
Thermal Conductivity (W/cm-K)	1.3	1.3	3.2	3 - 5	3 - 5
Intrinsic Carrier Concentration (cm^{-3})	10^{10}	$\sim 10^{-10}$	$\sim 10^{-4}$	$\sim 10^{-11}$	$\sim 10^{-11}$
Electron Mobility @ $N_D=10^{16}$ cm^{-3} ($cm^2V^{-1}s^{-1}$)	1200	1200	800	∥ c-axis = 900 ⊥ c-axis = 800	∥ c-axis = 60 ⊥ c-axis = 400
Hole Mobility @ $N_D=10^{16}$ cm^{-3} ($cm^2V^{-1}s^{-1}$)	420	30	40	115	90
Saturated Electron Velocity (x 10^7 cm/s)	1	2.5	2.5	2	2

Silicon carbide exists in about 250 crystalline forms [7]. The polymorphism of SiC is characterized by a large family of similar crystalline structures called polytypes which are variations of the same chemical compound that are identical in two dimensions and differ in the third. Hence, the SiC crystal Lattice can be viewed as layers stacked in a certain sequence [8]. Among the three important polytypes of Silicon Carbide (mentioned in Table 1), this thesis is focused on 4H-SiC polytype since the electronic properties of the same are most suited for semiconductor device operation. As per the data mentioned in Table 1, it can be observed that the major electronic properties of 4H-SiC are far superior than Si.

CHAPTER 2

SILICON CARBIDE POLYTYPES

The most common polytypes of SiC currently used for electronics are 3C-SiC, 4H-SiC, and 6H-SiC. The atomic crystal structure of the two most common polytypes is shown in the schematic cross section in Fig. 1. The different polytypes of SiC are actually composed of different stacking sequences of Si–C bilayers (also called Si–C double layers), where each single Si–C bilayer is denoted by the dotted boxes in Fig. 1 [4].

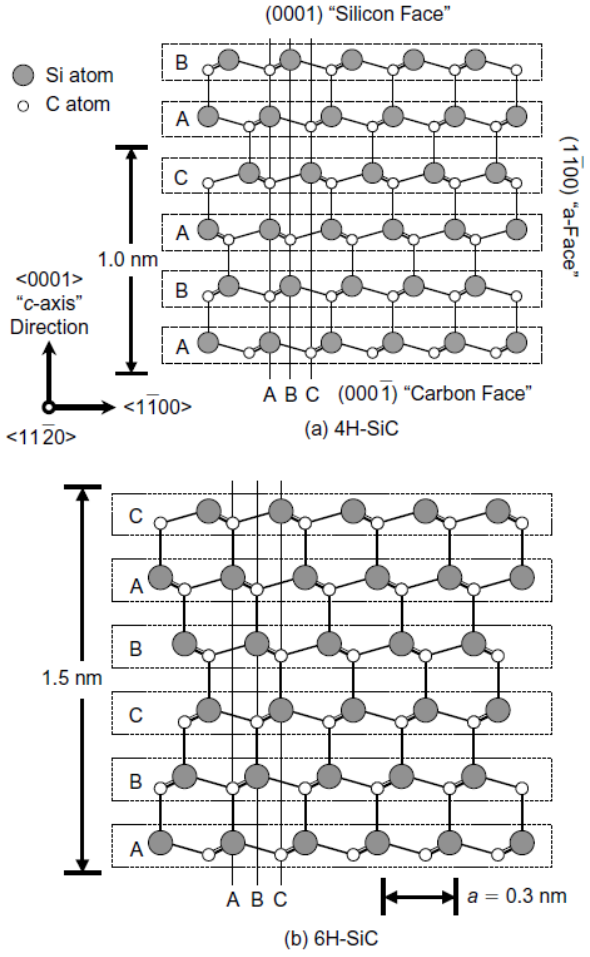

Figure 1. Cross-section of (a) 4H-SiC and (b) 6H-SiC atomic crystal structure [4]

Each atom within a bilayer has three covalent chemical bonds with other atoms in the same (its own) bilayer, and only one bond to an atom in an adjacent bilayer. Fig. 1 a shows the bilayer of the stacking sequence of 4H-SiC polytype, which requires four Si–C bilayers to define the unit cell repeat distance along the c -axis stacking direction (denoted by <0001> Miller indices). Similarly, the 6H-SiC polytype illustrated in Fig. 1b repeats its stacking sequence every six bilayers throughout the crystal along the stacking direction. The <1100> direction depicted in Fig. 1 is often referred to as one of (along with <1120>) the a-axis directions. SiC is a polar semiconductor across the c -axis, in that one surface normal to the c -axis is terminated with silicon atoms while the opposite normal c -axis surface is terminated with carbon atoms. As shown in Fig. 1a, these surfaces are typically referred to as "silicon face" and "carbon face" surfaces, respectively. Atoms along the left-or right-side edge of Fig. 1a would reside on (<1100>) "a-face" crystal surface plane normal to the direction. 3C-SiC, also referred to as β -SiC, is the only form of SiC with a cubic crystal Lattice structure. The non-cubic polytypes of SiC are sometimes ambiguously referred to as α-SiC. 4H-SiC and 6H-SiC are only two of the many possible SiC polytypes with hexagonal crystal structure [4].

CHAPTER 3

IMPORTANT PROPERTIES OF 4H-SiC

3.1 INTRINSIC CONCENTRATION

The Bandgap of 4H-SiC is approximately three times that of Silicon which is the reason for the extremely low intrinsic carrier concentration of 4H-SiC at room temperature. Fig. 2 shows the variation of intrinsic carrier concentration for Silicon Carbide as compared to Silicon. It can see that even at elevated temperatures, the generated carrier density for Silicon carbide is several orders magnitude less than Si. This is due to the fact that electrons require higher energy to cross the large Bandgap.

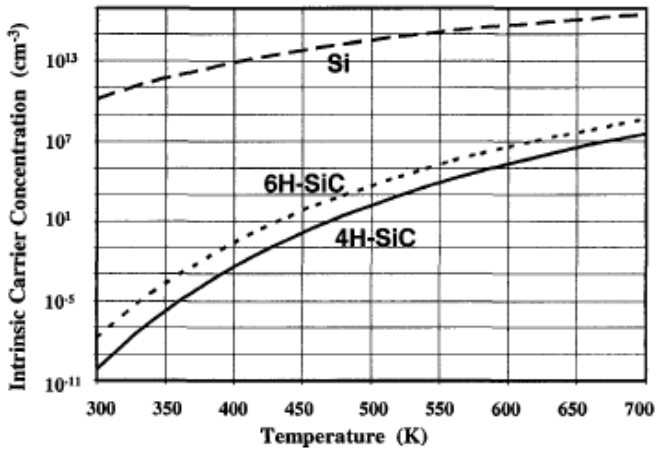

Figure 2. Intrinsic Carrier Concentration vs. Temperature [3]

Due to this wide band-gap, heat and other external influences do not readily disrupt the performance of SiC microelectronics. Therefore, SiC devices can operate at higher temperatures and higher radiation levels as compared to Si devices [8].

The critical field strength for 4H-SiC is approximately four times larger than Si. Due to the higher magnitude of the critical field strength, SiC devices have require a thinner drift region to block the same voltage as compared to Si devices. Since, the thickness of the drift region contributes towards the on state resistance of the device, Silicon Carbide devices exhibit much lower on state resistance for the same blocking voltage

[3]. One of the major challenges faced in the field of Power electronics is the removal of heat generated in the device. The thermal conductivity of Silicon Carbide is much higher than Si which means that the semiconductor material acts as a natural heat sink allowing heat to dissipate more readily than other semiconductor materials. Silver metal has the highest thermal conductivity of 4.29 W/cm-K, hence at room temperature [9], SiC has a higher thermal conductivity than any metal. This property enables SiC devices to operate at extremely high power levels and still dissipate the large amounts of excess heat generated.

3.2 BUILT IN POTENTIAL

The built in potential ($\mathbf{V_{bi}}$) is an important factor in determining the operation and design of power semiconductor devices. If D-MOSFETs are considered, the built in potential determines the zero-bias depletion width which is an important parameter in the calculation of on-state resistance of the device [3]. The built-in voltage is given by the equation:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A^- * N_D^+}{n_i^2}\right) \quad (1)$$

Equation 1. Built in Potential

where k is the Boltzmann constant, T is the temperature, q is the elementary charge, N_A and N_D are the ionized impurity concentration for acceptor and donor type respectively and ni is the intrinsic concentration of the semiconductor. Since the intrinsic carrier concentration for SiC is several orders magnitude less than Silicon, SiC has a much larger built in potential as compared to silicon. This can be a disadvantage due to the larger zero bias depletion width consumes space within the D-MOSFET cell structure increasing the on-state resistance by constricting the area through which the drain current flows. It is due to the higher built-in voltage, it is preferable to use SiC for Unipolar power devices like MOSFETs and Schottky diodes. SiC bipolar devices like PIN diode are used in high power applications where the power loss due to on state voltage is negligible as compared to the total power controlled. Fig. 3 shows the comparison of built in potential for Si and 4H-SiC and Fig. 4 shows the comparison of Zero bias depletion width for Si and SiC polytypes.

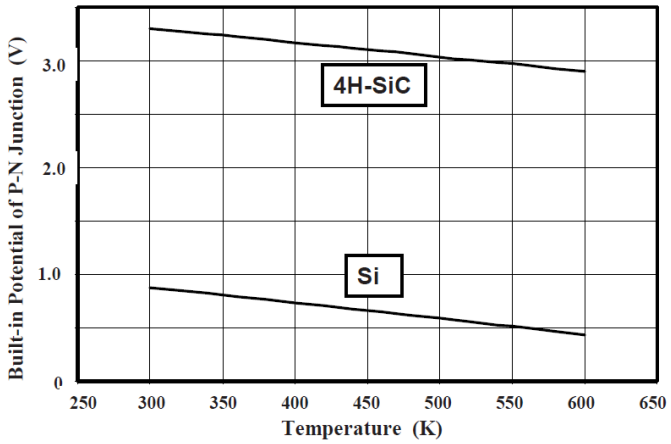

Figure 3. Built in Potential for a P-N junction in Si and 4H-SiC [3]

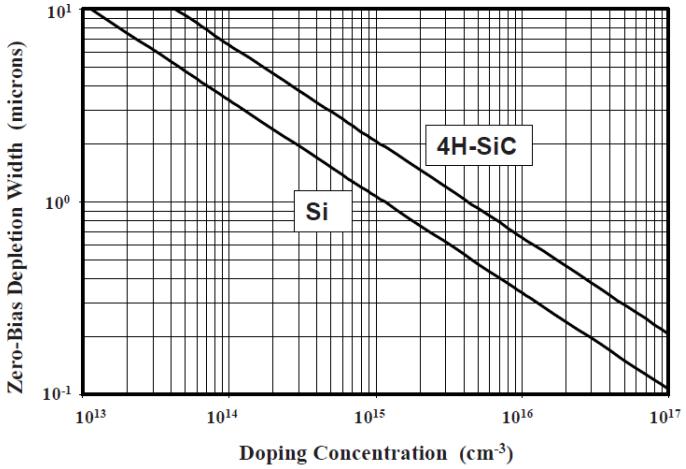

Figure 4. Zero-Bias depletion width in Si and 4H-SiC [3]

3.3 IMPACT IONIZATION

Impact Ionization is the primary mechanism responsible for the Breakdown failure of Power Devices. The process of impact ionization can be quantified using Chynoweth's Law

$$\alpha = a\, e^{\left(\frac{-b}{E}\right)} \tag{2}$$

Equation 2. Chynoweth's Law

where E is the electric field and 'a' and ' b' are constants which are dependent on the nature of the semiconductor and temperature [3]. The term 'α' is referred as impact ionization coefficient which is the number of electron-hole pairs created by an electron/hole while traversing 1 cm through the depletion layer in the direction of electric field. In order to study the process of impact ionization in 4H-SiC, Electron Beam Induced Current (EBIC) technique was used on a defect free region in a PN junction diode [3]. Fig. 5 shows the impact ionization coefficient for holes in 4H-SiC with respect to Si.

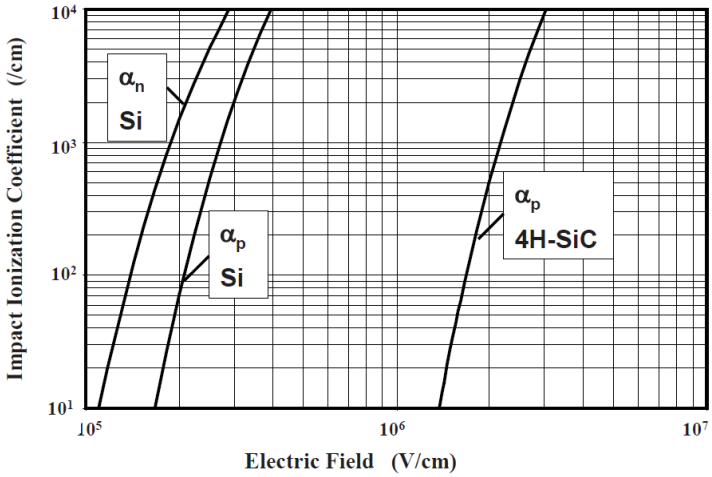

Figure 5. Impact Ionization Coefficient for 4H-SiC [3]

From the above figure, it is clear that the generation of electron-hole pairs become significant for a much higher magnitude of electric field in 4H-SiC as compared to Silicon. This increases the value of Critical Electric Field for the semiconductor. Another striking difference between the impact ionization mechanism between Si and SiC is the fact that the impact ionization rate for holes is higher than electrons for Silicon Carbide which is opposite to that of Silicon.

3.4 ENERGY BAND THEORY

Silicon Carbide is classified as a wide Bandgap semiconductor due to its large Bandgap as compared to Silicon. The Band-gap of 4H-SiC polytype is 3.26 eV which is about three times the Bandgap of Silicon (1.1 eV) [3]. The larger Bandgap enforces

a smaller generation of carriers in the depletion region which causes restricts leakage current through the device during its voltage blocking state. Another advantage of larger Bandgap is its suitability in the development of metal-semiconductor contacts (used in Schottky diodes) since the wide Bandgap raises the Schottky barrier height and restricts the magnitude of leakage current in Schottky diodes and Metal Semiconductor Field Effect Transistors (MESFETs) [3]. Fig. 6 shows the Bandgap and electron affinity values for 4H-SiC.

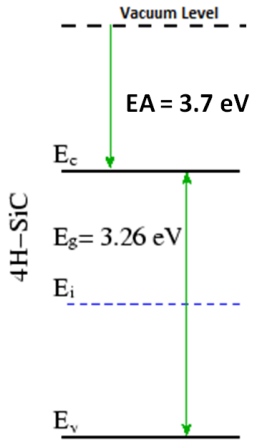

Figure 6. Energy Band Diagram of 4H-SiC [3]

The intrinsic carrier concentration for Silicon Carbide due to the thermal generation of electron hope pairs across the energy Bandgap can be calculated using the following equation:

$$n_i = \sqrt{N_C * N_V} * e^{\left(\frac{-E_G}{2kT}\right)} \quad (3)$$

Equation 3. Intrinsic Carrier Concentration

where $\mathbf{N_C}$ and $\mathbf{N_V}$ are the density of states in the conduction band and valence band respectively, $\mathbf{E_G}$ is the energy Bandgap in electron volts, k is the Boltzmann constant and T is the temperature. For 4H-SiC, the intrinsic carrier concentration can be calculated by the using the standard values in the above equation to obtain:

$$n_i = 1.7 \times 10^{16} T^{3/2} * e^{\left(\frac{-2.08 \times 10^4}{T}\right)} \quad (4)$$

Equation 4. Intrinsic Carrier Concentration (Reduced Form)

From the above equations, the value of intrinsic carrier concentration at a desired temperature for 4H-SiC can be calculated. At 300°K, the intrinsic carrier concentration of 4H-SiC is 6.7 x 10^{-11} cm^{-3} whereas for Silicon is 1.4 x 10^{10} cm^{-3} [3]. This shows that at room temperature, the leakage current for 4H-SiC device will be magnitudes lower than Silicon device. However, the superiority of 4H-SiC over Silicon comes into light when both the devices are exposed to high temperatures. The intrinsic carrier concentration of Silicon matches the typical doping concentrations of 1 x 10^{15} cm^{-3} at 540°K or 267°C whereas even at 700°K or 427°C, 4H-SiC has an intrinsic carrier concentration of 3.9 x 10^{7} cm^{-3}. This makes 4H-SiC an ideal material for high temperature power electronics device fabrication.

CHAPTER 4

SIMULATION TOOL

Silvaco© ATLAS Technology Computer-Aided Design (TCAD) simulation software was used for the AC and DC simulation of the Power Semiconductor Device. ATLAS software is designed to simulate the electrical, optical, and thermal behavior of semiconductor devices. It provides a physics-based, modular, and extensible platform to analyze DC, AC, and time domain responses for all semiconductor based technologies in 2 and 3 dimensions. In this research, the device simulation was carried out in 2 dimensions [10].

ATLAS is a physics based simulation tool which predicts the electrical and electronic characteristics of a semiconductor device with specified physical structure and bias conditions. In a physics based simulation tool, the structure of a semiconductor device is approximated onto a two or three dimensional grid which is divided into a number of grid points or nodes [11]. The electrical characteristics of the device is then predicted by simulating the transport of carriers through the grid points by applying differential equations derived from Maxwell's laws. The major advantages of Physics-based simulation over other simulation techniques is that it is predictive, it provides insight, and it captures theoretical knowledge in a way which is easier to interpret. In order to use this technique relevant physics must be incorporated into the simulation along and the numerical solver which will be used to solve the differential equations. The accuracy of the simulation depends on the simulation precision, the number of relevant physics based models involved, the design of the grid and the nature of the problem statement which needs to be solved. There is a tradeoff between the simulation time and the required numerical accuracy. An accurate simulation result requires a fine grid and large number of nodes whereas faster simulation speed and numerical efficiency requires fewer number of grid points. Hence, the above mentioned simulation parameters must be selected properly in order to obtain optimum simulation conditions [11].

In order to simulate a semiconductor device, ATLAS requires the following input:

- The physical structure of the device
- The physical models to be used
- The numerical methods required to solve the differential equations (both ordinary as well as partial differential equations)
- The bias conditions for the electrical device.

Considering the tradeoff between simulation accuracy and numerical efficiency, the device grid is designed in such a way that the grid/mesh is fine in the critical regions of the device and coarse in the non-significant regions of the device like the substrate in case of power devices. The following are examples of critical regions in a semiconductor device [11]:

- Areas of considerable recombination effects
- Areas of high electric field or impact ionization
- Areas of Metal Semiconductor junctions (e.g. in a Schottky diode)
- Area under the gate oxide in a MOSFET

The device physics related models are selected on the basis of the type of semiconductor device being simulated. ATLAS has a wide variety of models specifically designed for Unipolar and bipolar devices, optoelectronics, organic semiconductors etc. .The selection of appropriate models ensure optimum simulation conditions. Any non-relevant model increases the simulation time and may affect the output adversely. The numerical method selection depends on the convergence and the initial guess. If the initial guess is accurate, a fast convergence algorithm is preferred but if the initial guess is inaccurate, using a fast convergence numerical method would be inefficient and would take more number of steps to converge. The bias conditions for a device needs to be defined considering design parameters for the device itself. Appropriate biasing condition ensures faster convergence of the solutions of the differential equations. As an example, if a device is rated to block 1000V, the bias voltage steps needs to be sufficiently small near to the breakdown voltage since the change in current will be high due to impact ionization.

Fig. 7 shows the simulation process flow diagram for ATLAS. The input files can be generated through either one of ATHENA, DEVEDIT or DECKBUILD programs.

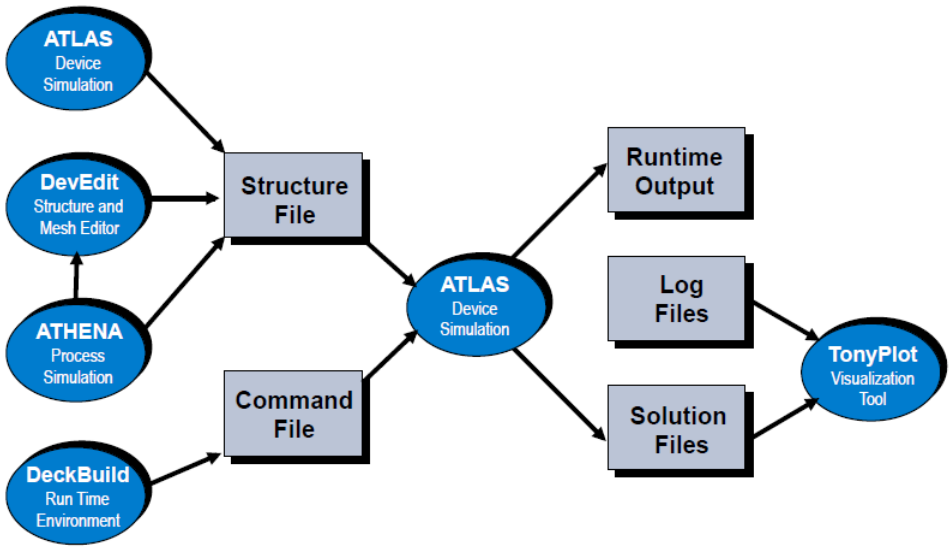

Figure 7. ATLAS Simulation Flow Diagram [12]

The input to ATLAS can be classified as the structure file generated via ATHENA or DEVEDIT or the command file generated via DECKBUILD. The Structure file contains data regarding the grid/mesh on which the device is defined. The command file, which can be generated and edited using either DECKBUILD program or any text editor, contains a sequence of commands/statements which corresponds to the bias conditions and physical models pertaining to the device [11].

The output of ATLAS consists of three types of data. The Runtime output gives the real time status of the simulation. This includes the solution of the semiconductor device physics equations, the tolerance settings and the convergence status. The log file stores the device terminal characteristics calculated by Atlas. These are current and voltages at electrodes in DC simulations (e.g. for a MOSFET, the current and voltages for the GATE, DRAIN and SOURCE electrodes are calculated and stored). In transient simulations, the time is stored. In AC simulations, the small signal frequency, the various conductance values involved and capacitances are saved. The structure file, by default, stores the 2D or 3D data regarding various parameters of the device like the doping concentrations, electron/hole concentration, current density, electric field etc. at a particular bias point. More data can be included in the structure

file (like mobility, current flow lines etc.) via statements in the command file. The structure file gives a graphical view of various processes occurring in the device structure. Program called *TONYPLOT* is used to view the data stored in log files and structure files. ATLAS has in-built modules specifically designed to simulate advanced semiconductor material and for thermal analysis [11].

4.1 BLAZE MODULE

BLAZE© module is a general purpose 2D device simulator which is specifically designed towards the simulation of III - V, II - VI materials. Blaze simulates devices fabricated using advanced materials. It includes a library of binary, ternary and quaternary semiconductors [13]. Once ATLAS detects Silicon Carbide in the material parameter, it automatically enables BLAZE module. BLAZE alters the basic drift diffusion equations to account for effects introduced by compound semiconductors.

4.2 GIGA MODULE

GIGA© module combined with S-Pisces and Blaze device simulators allows simulation of self heating effects. Models in Giga include heat generation, heat flow, Lattice heating, heat sinks, and effects of local temperature on physical constants. Thermal and electrical physical effects are coupled through self-consistent calculations. Giga is a fully integrated component of the ATLAS device simulation framework [14]. GIGA module for Silicon Carbide is discussed in detail in the Lattice Heating section.

CHAPTER 5

SEMICONDUCTOR DEVICE PHYSICS

The equations which are solved in ATLAS TCAD, like any other general purpose physics based simulator, are derived from Maxwell's laws and consists of Poisson's equation, Continuity equation and Transport or Constitutive equation. Poisson's Equation relates variations in electrostatic potential to local charge densities. The continuity and the transport equations describe the way that the electron and hole densities evolve as a result of transport processes, generation processes, and recombination processes.

5.1 POISSON'S EQUATION

Poisson's Equation relates the electrostatic potential to the space charge density by the following equation:

$$div\left(\varepsilon \nabla \psi\right) = -\rho \tag{5}$$

Equation 5. Poisson Equation

where ε denotes the local permittivity, Ψ is the electrostatic potential and ρ is the local space charge density. In ATLAS the reference potential is defined by the intrinsic Fermi potential Ψi . The local space charge density is the sum of contributions from all mobile and fixed charges, including electrons, holes, and ionized impurities. The electric field data is obtained from the gradient of the potential via the following equation [11]:

$$\vec{E} = -\nabla \psi \tag{6}$$

Equation 6. Electric Field Equation

5.2 CARRIER CONTINUITY EQUATIONS

The continuity equations for electrons and holes are defined by the following equations [11]:

$$\frac{\partial n}{\partial t} = \frac{1}{q} div \vec{J}_n + G_n - R_n$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} div \vec{J}_p + G_p - R_p \quad (7)$$

Equation 7. Continuity Equations for Electrons and Holes

where

- n and p are electron and hole concentrations respectively
- $\mathbf{J_n}$ and $\mathbf{J_p}$ are electron and hole current density vectors respectively
- $\mathbf{G_n}$ and $\mathbf{G_p}$ are the generation rates for electron and holes respectively
- $\mathbf{R_n}$ and $\mathbf{R_p}$ are recombination rates for electron and holes respectively
- q is the magnitude of the charge on an electron

By default ATLAS solves both the continuity equations for any simulation. If required the simulation can be configured to run for only one type of carrier.

5.3 TRANSPORT EQUATIONS

Equation a, b and c constitute the general device physics equations. However, secondary equations are required to specify particular physical models for $\vec{J}_n, \vec{J}_p, G_n, G_p, R_n$ and R_p.

The current density equations used by the device simulator are usually obtained by applying approximations and simplifications (shown in Fig. 8) to the Boltzmann Transport Equation. These assumptions can result in a number of different transport models such as the drift-diffusion model, the Energy Balance Transport Model or the hydrodynamic model [11].

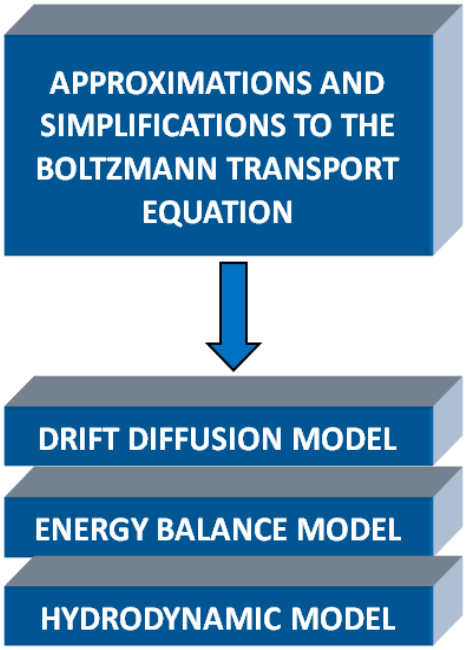

Figure 8. Transport Models [15]

5.4 DRIFT DIFFUSION MODEL

The simplest model of charge transport that is useful is the Drift-Diffusion Model. This model has the attractive feature that it does not introduce any independent variables in addition to Ψ, n and p. The drift-diffusion model is adequate for nearly all devices especially for power applications as the device size is large. ATLAS supplies both drift-diffusion and advanced transport models. The charge transport models and the models for generation and recombination in ATLAS make use of some concepts associated with carrier statistics. In this model the electron current density is expressed as a sum of two components. The drift component which is driven by the electric field and the diffusion component caused by the gradient of the electron concentration [11].

The Simplified form of Drift Diffusion Current equation for electrons and holes can be expressed as:

$$J_n = q\,n(x)\,\mu_n\,E(x) + q\,D_n\frac{dn}{dx}$$

$$J_n = q\,p(x)\,\mu_p\,E(x) - q\,D_p\frac{dp}{dx} \quad (8)$$

Equation 8. Drift Diffusion Current equation for Electrons and Holes

where q is the absolute value of electronic charge, μ_n and μ_p are the motilities of electrons and holes respectively, E represents the electric field as a function of the grid spacing x and D_n and D_p are the diffusion coefficients for electrons and holes respectively. However, the complete drift diffusion model is defined by the set of 1D equations comprising of the Poisson's Equation, Continuity equation and the Transport Equation [16].

Table 2. Drift Diffusion Transport Model features

ADVANTAGES AND LIMITATIONS OF THE DRIFT DIFFUSION TRANSPORT MODEL	
• Simplicity in Simulation • Immediate Physical Interpretation • Efficient Numerical Methods • Faster Simulation Speed • Adequate for nearly all Devices	• Does not introduce carrier temperature or energy as independent variable. • Less Accurate for Deep Sub-Micron devices and too high gradients.

CHAPTER 6

FACTOR AFFECTING DEVICE SIMULATION

The basic factors affecting the simulation efficiency and the results of simulation can be classified into the following conditions:

6.1 THE MESH SIZE Δx

In order to simulate a device using ATLAS TCAD, the device must be first modeled on to a 2D or 3D grid which is divided into grid/mesh points. In order to resolve space charge variations, the mesh size has to be smaller than the Debye length of the semiconductor. Debye Length of a semiconductor is defined as the distance in semiconductor over which local electric field affects distribution of free charge carriers [16]. The Debye length can be calculated using the following equation:

$$L_D = \sqrt{\frac{\varepsilon k_B T}{q^2 N}} \tag{9}$$

Equation 9. Debye Length

where ε is the permittivity of the semiconductor material, k_B is the Boltzmann constant, T is the temperature, q is the magnitude of the electronic charge and N is the doping concentration. As per the equation [16], Debye length is directly proportional to the temperature and inversely proportional to the doping concentration which means a heavily doped region has a smaller magnitude of Debye length. However, it is not always feasible to reduce the mesh size so that it is smaller than the Debye length since there is a tradeoff between the mesh size and the simulation efficiency.

6.2 THE DIELECTRIC RELAXATION TIME t_{DR}

Dielectric relaxation is the momentary delay in the dielectric constant of a material which is usually caused by the delay in molecular polarization with respect to a changing electric field in a dielectric medium [17]. Dielectric Relaxation time can be defined as the characteristic time required by a semiconductor to reach electrical neutrality after carrier injection or extraction [17]. It is estimated using the following equation:

$$t_{dr} = \frac{\varepsilon}{q N \mu} \tag{10}$$

Equation 10. Dielectric Relaxation Time

where ε is the permittivity, q is the magnitude of electronic charge, N is the doping concentration and μ is the mobility [17]. The simulation time step must be smaller than this value in order to avoid convergence errors. However, decreasing the time step also means an extended simulation time which places a tradeoff between the two parameters.

6.3 OBTUSE TRIANGLES IN THE MESH

While defining the device structure mesh, it is very important to make sure that the number of obtuse triangles in the mesh is zero or very less as the presence of obtuse triangle leads to errors in the simulation and in the worst case scenario cause convergence errors. As a general rule, obtuse triangles or high aspect ratio triangles should be avoided in the mesh. The user can run the program after declaring the mesh and the runtime output data will show the percentage and count of obtuse triangles in the mesh.

6.4 DEVICE MESH DOPING DISTRIBUTION

It is advisable to first dope the entire structure with a uniform doping scheme using the doping value which occupies maximum area on the 2D mesh. This prevents the formation of un-doped junctions between two regions. For instance if there is a

device consisting of three regions and if these regions were created and doped separately, there will be junctions between the regions which will not have any doping data. This scenario may create issues while simulating as the simulator may not find the doping data on the basis of which differential equations are solved. In a typical power device, majority of the area is consumed by the drift region. Hence, uniform doping scheme can be first used on the entire mesh region using the value of Drift region doping concentration. For example, in a power D-MOSFET structure, there are four doping concentrations namely N+ Source, Drift region, P-Base region and N+ Substrate. Using the above mentioned technique, first the entire mesh is doped using Drift region doping, then the N+ Source, P-Base region and N+ Substrate doping concentrations will be specified in the code.

6.5 BIASING VOLTAGE STEPS

While solving for Breakdown voltage, it is necessary to take small bias voltage steps (in the order of millivolts) in the beginning of the simulation. This is important because firstly, the device simulator uses numerical methods to solve differential equations and any large bias step will result in convergence error forcing the simulator to reduce the bias step and if the convergence error exists for a given number of iterations, the program will terminate. Secondly, in the breakdown characteristics, the change in magnitude of current is high for initial few volts and during the breakdown phase. In between these two end phases the leakage current almost stays constant. Hence, in order to maximize breakdown simulation efficiency, the voltage bias steps are kept small in the initial and breakdown phase and bias steps can be made large in between the two phases. Normally this process is optimized after multiple trial and error runs to get an estimate of the breakdown voltage.

For any switching power device, the control voltage bias steps must be kept small during the turn on of the device. For e.g. the voltage bias steps for a MOSFET gate must be kept small in the vicinity of the threshold voltage since the magnitude of current rise will be very high.

CHAPTER 7

FACTORS AFFECTING THERMAL SIMULATION

Thermal simulation in Silvaco ATLAS is performed using the GIGA module. Like any other device simulator, ATLAS solves differential equations to obtain different electrical quantities and a proper boundary condition or initial condition must be present to obtain converging results. In order to successfully solve heat equation in ATLAS, the device simulation code must contain proper boundary condition where the generated heat gets dissipated.

The factors affecting thermal simulation include the thermal conductivity, heat capacity, ambient temperature and most importantly, the Heat Transfer Coefficient. Using the correct models for thermal conductivity and heat capacity ensures accurate results. It is always advisable to verify the default values supplied by the simulator with the values available in research papers. Thermal Conductivity and Heat Capacity models will be discussed in detail in the Lattice Heating section. Heat Transfer Coefficient can be defined as the rate at which heat leaves a surface. It is a function of the heat flow, temperature difference between the surface and the ambient and the area of the surface. It has a unit of W cm^{-2} K^{-1}. This property depends on the interface between the heat source and sink and does not depend on the nature of the material. It is given by the equation [18]

$$\boldsymbol{Q = \alpha\ A\left(T_{source} - T_{sink}\right)} \tag{11}$$

Equation 11. Heat Transfer Equation

where

- Q is the Heat Flow (J s^{-1} or W)
- α is the Heat Transfer Coefficient (W cm^{-2} K^{-1})
- A is the Heat Transfer Surface Area (cm^2)
- $\Delta T = T_{source} - T_{sink}$ is the difference in temperature between solid surface and surrounding fluid area (K)

The value of heat transfer coefficient has to be carefully selected as it can severely affect the convergence of the program. A low value of heat transfer coefficient results in excessive heat dissipation especially during the initial bias voltage calculation in DC simulation or device turn on in transient simulation. On the other hand, a high value will result in a higher transfer of heat from the source (in this case, semiconductor device Lattice) to the sink (boundary condition) and this leads to lower temperature rise being recorded in the solution/structure file. This research used trial and error technique to optimize the value.

CHAPTER 8

SIMULATION PLATFORM

Silvaco ATLAS software has been developed for both Windows and Linux platforms. However, certain features of ATLAS are not supported on Windows platform. This includes Extended Precision which is one of the major requirements while simulating wide Bandgap semiconductors. The simulation was performed on different hardware profiles which included:

- Intel CORE^{TM} i7 Processor with 8 processing cores @ 1.6 GHz and 6GB RAM
- Intel Xeon^{TM} X5460 processor with 6 processing cores @ 3.16 GHz and 10GB RAM

However, due to the extremely long simulation time on the above systems, the simulation required for this research was conducted on a mainframe at the High Performance Computing Center (HPCC) at Texas tech University. The program was executed on Redhat Linux version 2.6.18 platform. Since Silvaco ATLAS was not designed for cluster processing over several nodes on the super computer, each simulation was run on a single node having 12 processing cores with 24 GB RAM.

CHAPTER 9

SETTING UP THE SIMULATION ENVIRONMENT

Silvaco ATLAS , like any other numerical simulator, is optimized for Linux environment. Since multiple hardware platforms were tested for this simulation, Linux was installed on the every hardware platform excluding the super computer where it was already in use. To avoid the complicated Linux installation procedure on the following hardware profiles.

- Intel CORE™ i7 Processor with 8 processing cores @ 1.6 GHz and 6GB RAM
- Intel Xeon™ X5460 processor with 6 processing cores @ 3.16 GHz and 10GB RAM

Oracle© VM VirtualBox software was installed. It's a free virtual machine software provided by Oracle. Using this software, Fedora 14 Linux was installed on the above machines while still operating on Windows 7 platform. Fedora 14 was chosen due to its similarity to Red Hat Linux which is a paid version of Linux. Since Intel© i7 and Xeon Processor hardware is optimized for virtualization technology, there was no noticeable difference in the performance of Linux installed on the virtual machine.
Once Silvaco was installed at HPCC, the program execution had to be carried out through job scheduling scripts. The following (Fig. 9) is the syntax of a job scheduling script used on HPCC [19].

```
#$ -V
#$ -cwd
#$ -S /bin/bash
#$ -N test
#$ -o $JOB_NAME.o$JOB_ID
#$ -e $JOB_NAME.e$JOB_ID
#$ -q normal
#$ -pe fill 12
#$ -P hrothgar
hostname
```

Figure 9. HPCC Job Scheduling Script Format [19]

Fig. 10 shows an example script file used in this research. The file is saved in ***.sh*** format. Once the script file is prepared, the command ***qsub*** is used to schedule the particular job in the queue. There were issues regarding read/write permissions on the super computer which were resolved with the help of technical support team at HPCC.

```
#$ -V
#$ -cwd
#$ -S /bin/bash
#$ -N Current_1
#$ -o $JOB_NAME.o$JOB_ID
#$ -e $JOB_NAME.e$JOB_ID
#$ -q normal
#$ -pe fill 12
#$ -P hrothgar
(cd /home/bpushpak/DMOS/Half_Cell/Current_Pulsing_1/; /lustre/work/apps/simucad/bin/deckbuild -run -ascii  -as
/home/bpushpak/DMOS/Half_Cell/Current_Pulsing_1/Current_Pulse.in -outfile Runtime)
```

Figure 10. Sample Job Scheduling Script File

CHAPTER 10

EXTENDED PRECISION

A critical factor that needs to be considered while simulating Wide Bandgap devices is the numerical precision of the simulator. During the initial phase of the research, simulations were conducted on a 4H-SiC PIN Diode rated for 10kV blocking voltage and 1A forward current. The PIN diode was simulated using the standard precision available in the simulator which was 64-bit or 8 bytes [11]. However, when the device was simulated for its breakdown characteristics, it was observed that the reverse leakage current waveforms were severely distorted and the device was not breaking down even at five times the designed breakdown voltage. The simulation was repeated for different parameters but incorrect results were obtained each time. This led to the conclusion that the device simulator settings must be altered manually to cater to Wide Bandgap materials.

Wide Bandgap materials are typically characterized by their extremely low intrinsic carrier concentration as compared to small Bandgap material like Silicon. This results in extremely low values of carrier current densities during simulation (for e.g. in case of 4H-SiC, these values were in order of 10^{-80} A). If the simulator is not configured for higher precision, the results of every iteration will be truncated to the default precision value resulting in incorrect values being piled up. These incorrect values prevented the avalanche multiplication process as the there was no trigger point for the breakdown process. This issue can be better understood by the following analogy. In reality, no matter how much snow is accumulated on a mountain top, there must be some sort of trigger to initiate the avalanche formation. This issue in Wide Bandgap device simulation can be bypassed by the following techniques:

- Artificially increasing the intrinsic carrier concentration using ATLAS command.
- Artificially increasing the intrinsic carrier concentration by focusing high energy beam (e.g. LASER) on the device Lattice to generate electron-hole pairs.
- Increasing the Device Simulator Precision.

The first two techniques are feasible but impractical since any device should be simulated the way it is instead of artificially modifying its properties. Impact ionization process is initiated by high energy particles (electron/holes) in a semiconductor but as per the Maxwell Boltzmann Energy function (Fig. 11), higher the particle energy, lower the particle density.

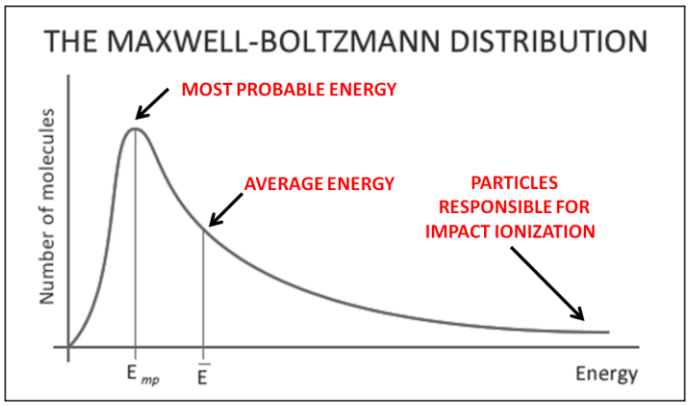

Figure 11. Maxwell Boltzmann Energy Distribution [20]

So in order to capture the events of the few high energy particles, the device simulator precision must be increased. Increasing the device simulator precision will give accurate results without altering the device properties but at the expense of simulation time. As per theory of carrier statistics, it can estimate that for an accurate and convergent simulation [11]

$$P \geq \frac{1}{\ln(2)} \left(\frac{E_G}{k_B T_L} \right) \tag{12}$$

Equation 12. Simulation Precision

where P is the required precision, E_G is Bandgap in Joules, k_B is the Boltzmann constant and T_L is the Lattice temperature. For 4h-SiC, if the values of Bandgap, E_G = 3.26 eV and Lattice temperature T_L = 300K are used in the above equation, the required precision would be approximately 182-bit. This would require ATLAS to be configured for an extended precision of 256-bit which is the maximum for ATLAS. However, the simulation time is a strong function of the simulator precision. In order to obtain accurate results without adversely affecting the simulation time, the device was simulated using the available extended precision options in ATLAS (80-bit, 128-

bit, 160-bit and 256-bit). It was observed that 128-bit simulation resulted in accurate results with minimal increase in simulation time as compare to the other precision option. All the simulation for this research were carried out with an extended precision of 128-bits.

CHAPTER 11

SIMULATION MODELS

For any physics based simulation software, the selection of simulation models is a key factor. This requires a considerable amount of knowledge regarding the model used. A device simulation that includes models which are not required for the simulation will not only increase the simulation time but also jeopardizes the result. In this research, the following models were used in the simulation of the PIN diode and the D-MOSFET.

11.1 FERMI - DIRAC STATISTICS

In this simulation, the default Boltzmann Statistics simulation option was overridden with the Fermi Dirac Statistics. This was done because firstly the default Metal Oxide Semiconductor (MOS) device simulation requires Fermi Dirac Statistics and secondly it is required to incorporate high concentration effects. In Silvaco ATLAS, it is enabled by ***FERMIDIRAC*** parameter in the ***MODEL*** statement which is by default included in the ***MOS*** parameter.

Electrons in thermal equilibrium at Lattice temperature TL in a semiconductor obey the Fermi-Dirac Statistics [11] which is the probability that an available electron state with energy E is occupied by an electron and is given by

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{k_B T_L}\right)} \tag{13}$$

Equation 13. Fermi-Dirac Probability Function

where E_F is the Fermi Level, k_B is Boltzmann constant and T_L is the lattice temperature.

11.2 RECOMBINATION MODELS

11.2.1 SHOCKLEY READ HALL RECOMBINATION

Recombination through defects is known as Shockley-Read-Hall or SRH recombination. Since it is dependent on the defects in the material, it does not occur in pure material. In this process, either an electron is trapped by an energy state which is introduced through defects in the crystal Lattice or a hole moves up to the same energy state before the electron is thermally re-emitted into the conduction band, then it recombines These defects can either be unintentionally introduced or can be deliberately added to the material to alter its properties. In Silvaco ATLAS, Shockley-Read-Hall Recombination is activated via ***SRH*** parameter in the ***MODEL*** statement and its modeled by the equation [11]

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_P\left[n + n_{ie}\exp\left(\frac{ETRAP}{k_B T_L}\right)\right] + \tau_N\left[p + n_{ie}\exp\left(\frac{-ETRAP}{k_B T_L}\right)\right]}$$

where

$$\tau_N = \frac{TAUN0}{AN + BN\left(\frac{N_{TOTAL}}{NSRHN}\right) + CN\left(\frac{N_{TOTAL}}{NSRHN}\right)^{EN}} \quad (14)$$

$$\tau_P = \frac{TAUP0}{AP + BP\left(\frac{N_{TOTAL}}{NSRHP}\right) + CP\left(\frac{N_{TOTAL}}{NSRHP}\right)^{EP}}$$

Equation 14. Shockley-Read-Hall Recombination

where ***ETRAP*** is the difference between the trap energy level and the intrinsic Fermi level, n_{ie} is the intrinsic carrier concentration, T_L is the Lattice temperature, ***TAUN0*** and ***TAUP0*** are the recombination lifetimes, N_{TOTAL} is the local impurity concentration, ***NSRHN*** and ***NSRHP*** are concentration parameters. For 4H-SiC, Table 3 shows the custom parameters that were used [21]

Table 3. Shockley Read Hall Recombination Parameters

PARAMETER	*VALUE*
NSRHN	***3 x 10^{17} cm^{-3}***
NSRHP	***3 x 10^{17} cm^{-3}***
TAUN0	***1 x 10^{-9} s***
TAUP0	***1 x 10^{-9} s***

Default ATLAS values [11] were selected for the parameters which are not mentioned in Table 3.

11.2.2 AUGER RECOMBINATION

In Auger Recombination, the energy and momentum released by the recombination of an electron and hole is transferred to a third mobile particle which may be an electron in case of a heavily doped N-type material or a hole in case of a heavily doped P-type material. This process is only significant at high carrier concentration or high current densities like impact ionization. In Silvaco ATLAS, it is activated via ***AUGER*** parameter in the ***MODEL*** statement and is modeled by the equation

$$R_{AUGER} = AUGN\left(pn^2 - nn_{ie}^2\right) + AUGP\left(np^2 - pn_{ie}^2\right) \quad (15)$$

Equation 15. Auger Recombination

where AUGN and AUGP are user definable parameters.

11.3 INCOMPLETE IONIZATION

At low temperatures the thermal energy within a semiconductor is not high enough to fully activate all of the donor and acceptor impurity atoms. As a result the carrier concentration will not reach the concentration of dopant atoms [22, 23]. SiC distinguishes from narrow Bandgap semiconductors, such as silicon, in that common doping impurities in 4H-SiC have activation energies larger than the thermal energy (k_BT) even at room temperature. This causes the incomplete ionization of such

impurities, which leads to strong temperature and frequency dependence of the semiconductor junction differential admittance [24]

Silvaco ATLAS can account for impurity freeze-out [11] with appropriate degeneracy factors ***GCB*** and ***GVB*** for conduction and valence bands. This model is activated by using the ***INCOMPLETE*** parameter of the ***MODEL*** statement . The ionized donor and acceptor impurity concentrations are then given by the equation

$$N_D^+ = \frac{N_D}{1 + GCB \exp\left(\frac{{}^{\varepsilon}F_n - \left(E_C - EDB\right)}{k_B T_L}\right)}$$

$$N_A^- = \frac{N_D}{1 + GVB \exp\left(\frac{\left(E_V + EAB\right) - {}^{\varepsilon}F_p}{k_B T_L}\right)} \quad (16)$$

Equation 16. Incomplete Ionization

where ***EDB*** and ***EAB*** are dopant activation energies and N_D and N_A are net compensated n-type and p-type doping. For 4H-SiC, Table 4 shows the custom parameters that were used [24]

Table 4. Incomplete Ionization Parameters

PARAMETER	*VALUE*
EDB	***0.08 eV***
EAB	***0.19 eV***

Default ATLAS values [11] were selected for the parameters which are not mentioned in Table 4.

11.4 BANDGAP ENERGY

In this simulation, the Universal Bandgap Energy model was used for 4H-SiC. In Silvaco ATLAS, the temperature dependence of Bandgap energy is modeled using the equation

$$E_g(T_L) = EG300 + EGALPHA\left(\frac{300^2}{300 + EGBETA} - \frac{T_L^2}{T_L + EGBETA}\right) \quad (17)$$

Equation 17. Universal Bandgap Energy Equation

The Universal Bandgap Energy model can be activated by defining ***EG300*** parameter in the ***MATERIAL*** statement. For 4H-SiC, Table 5 shows the custom parameters that were used [21]

Table 5. Bandgap Energy Parameters

PARAMETER	*VALUE*
EG300	***3.26 eV***
EGALPHA	***3.3 x 10^{-4} eV K^{-1}***

Default ATLAS values [11] were selected for the parameters not mentioned in the above Table 5.

11.5 BAND GAP NARROWING

The phenomena involving the shrinkage of semiconductor material Bandgap when the impurity concentration is very high is known as Bandgap Narrowing. This effect becomes significant when the doping concentration typically exceeds 10^{18} cm^{-3}. This band structure is basically altered by three effects which can be summarized as the following [26]

- The interaction between adjacent impurity atoms (due to high concentration) leading to the splitting of the impurity levels into an impurity band.
- The statistical distribution of the dopant atoms in the Lattice introduces point-by-point differences in local doping concentration and Lattice potential causing the formation of band tails. This effect is significant at doping levels approaching a value of 10^{21} cm^{-3}.
- The interaction between the free carriers and more than one impurity atom leads to a modification of density of states at the band edges.

Fig. 12 shows the effects of Bandgap Narrowing.

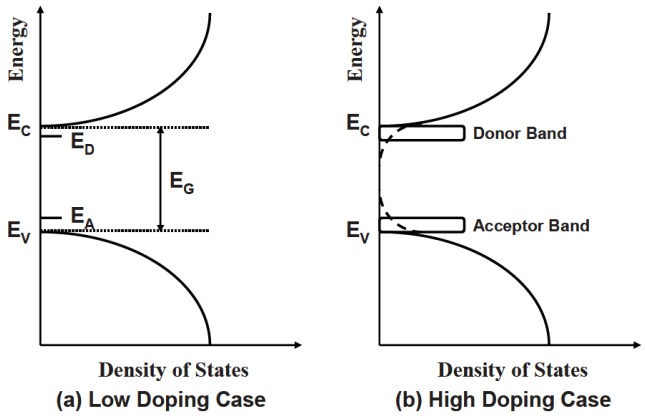

Figure 12. Band Gap Narrowing [26]

In Silvaco ATLAS, the model can be activated using the ***BGN*** parameter in the ***model*** statement. It is defined by the equation

$$\Delta E_g = BGN.E\left\{\ln\left(\frac{N}{BGN.N}\right)+\left[\left(\ln\frac{N}{BGN.N}\right)^2+BGN.C\right]^{\frac{1}{2}}\right\} \quad (18)$$

Equation 18. Bandgap Narrowing

where BGN.E, BGN.N and BGN.C are user definable parameters.

11.6 MOBILITY MODELS

The carrier mobility is primarily dependent on Lattice scattering (phonon scattering) and ionized impurity scattering. The following models were used in the simulation to completely account for factors affecting the mobility of carriers in the MOSFET.

11.6.1 CAUGHEY THOMAS ANALYTIC MODEL

At low electric field, the electron velocity varies almost linearly with the field intensity, The analytical low field mobility model developed by Caughey and Thomas [11] is used to describe this effect. This mobility model takes into account the effect of doping concentration as well as temperature. In Silvaco ATLAS, this model can

activated by using ***ANALYTIC*** parameter in the ***model*** statement. The low field mobility for electrons and holes is described by the equations

$$\mu_{n0} = MU1N.CAUG\left(\frac{T_L}{300K}\right)^{ALPHAN.CAUG} + \frac{MU2N.CAUG\left(\frac{T_L}{300K}\right)^{BETAN.CAUG} - MU1N.CAUG\left(\frac{T_L}{300K}\right)^{ALPHAN.CAUG}}{1+\left(\frac{T_L}{300K}\right)^{GAMMAN.CAUG}\cdot\left(\frac{N}{NCRITN.CAUG}\right)^{DELTAN.CAUG}}$$

$$\mu_{p0} = MU1P.CAUG\left(\frac{T_L}{300K}\right)^{ALPHAP.CAUG} + \frac{MU2P.CAUG\left(\frac{T_L}{300K}\right)^{BETAP.CAUG} - MU1P.CAUG\left(\frac{T_L}{300K}\right)^{ALPHAP.CAUG}}{1+\left(\frac{T_L}{300K}\right)^{GAMMAP.CAUG}\cdot\left(\frac{N}{NCRITP.CAUG}\right)^{DELTAP.CAUG}} \quad (19)$$

Equation 19. Caughey Thomas Low Field Mobility

where ***MUIN.CAUG*** is the mobility of a heavily doped semiconductor and ***MU2N.CAUG*** is the mobility of an un-doped semiconductor. ***BETAN/BETAP*** determines the change in mobility from un-doped condition to doped condition due to Lattice scattering. ***ALPHAN/ALPHAP*** is a constant temperature coefficient. ***DELTAN/DELTAP*** determines the rate of change of mobility from maximum value to minimum [11, 27]. These parameters are set in the ***MOBILITY*** statement. For 4H-SiC, Table 6 shows the custom parameters that were used [21, 27, 28]

Table 6. Caughey Thomas Mobility model Parameters

PARAMETER	*VALUE*
MU2N.CAUG	***1136 $cm^2 V^{-1} s^{-1}$***
MU1N.CAUG	***40 $cm^2 V^{-1} s^{-1}$***
NCRITN.CAUG	***2 x 10^{17} cm^{-3}***
ALPHAN.CAUG	***-3***
BETAN.CAUG	***-3***
GAMMAN.CAUG	***0.0***
DELTAN.CAUG	***0.76***
MU2P.CAUG	***125 $cm^2 V^{-1} s^{-1}$***
MU1P.CAUG	***20 $cm^2 V^{-1} s^{-1}$***
NCRITP.CAUG	***1 x 10^{19} cm^{-3}***
ALPHAP.CAUG	***-3***
BETAP.CAUG	***-3***
GAMMAP.CAUG	***0.0***
DELTAP.CAUG	***0.5***

Default ATLAS values [11] were selected for the parameters which are not mentioned in Table 6.

11.6.2 LOMBARDI MODEL

In order to obtain accurate results for MOSFET simulation, the mobility degradation in the channel must be considered due to high surface scattering at the semiconductor insulator interface. The Lombardi (CVT) model [11] is by default included in the model statement once the parameter ***MOS*** is declared. It can be alternately set in the code by using the parameter ***CVT*** in the ***model*** statement. The CVT model is a complete model which included doping concentration as well as temperature effects and also accounts for transverse electric fields.

Lombardi's formulation adds terms for surface acoustic phonon scattering (μ_{ac}) and surface roughness scattering (μ_{sr}) to the optical intervalley phonon scattering bulk mobility (μ_b) using a Matthiessen's rule

$$\frac{1}{\mu_T} = \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_b} \tag{20}$$

Equation 20. Lombardi's Mobility Model

Due to detailed nature of this model, it will not be discussed in this thesis.

11.6.3 PARALLEL FIELD DEPENDENT MOBILITY

At Low Electric Field magnitude, the relationship between the drift velocity and the applied electric field is almost linear but as the Field intensity increases, the relationship is no longer linear. At High Field, the drift velocity increases and ultimately saturates [11].

$$v_{Drift} = \mu . E \tag{21}$$

Equation 21. Drift Velocity

The saturation of drift velocity occurs due to the heating up of the carriers which in turn increases the scattering process and velocity becomes constant. In Silvaco ATLAS, this model is activated using the parameter ***FLDMOB*** in the ***model*** statement. This model must be included to account for any velocity saturation effect. The following Caughey Thomas equations are used to implement a field dependent mobility [11]

$$\mu_n(E) = \mu_{n0}\left[1 + \left(\frac{\mu_{n0}\,E}{VSATN}\right)^{BETAN}\right]^{-BETAN}$$

$$\mu_p(E) = \mu_{p0}\left[1 + \left(\frac{\mu_{p0}\,E}{VSATP}\right)^{BETAP}\right]^{-BETAP} \quad (22)$$

Equation 22. Caughey Thomas Equation for Field Dependent Mobility

where ***E*** is the parallel electric field, ***VSATN/VSATP*** is the saturation velocity which can either be a constant value provided by the user or can be internally calculated, ***BETAN/BETAP*** are user-definable parameters. These mentioned parameters can be set in the ***MOBILITY*** statement. For 4H-SiC, Table 7 shows the custom parameters that were used [21]

Table 7. High Field Mobility Parameters

PARAMETER	*VALUE*
VSATN	***2.2 x 10^{7} cm s^{-1}***
VSTAP	***2.2 x 10^{7} cm s^{-1}***

Default ATLAS values [11] were selected for the parameters which are not mentioned in Table 7.

11.6.4 ANISOTROPIC MOBILITY

The polytypes of SiC exhibit Anisotropic mobility due to its crystal structure arrangement. This effect is more dominant in the 3C-SiC and 6H-SiC polytypes and less in 4H-SiC [21, 27]. For 4H-SiC

$$\frac{\mu_{n\perp}}{\mu_{n||}} = 0.8 \quad (23)$$

Equation 23. Anisotropic Mobility for 4H-SiC

whereas for 6H-SiC

$$\frac{\mu_{n\perp}}{\mu_{n||}} = 5.0 \tag{24}$$

Equation 24. Anisotropic Mobility for 6H-SiC

where $\mu_{n\perp}$ denotes the mobility perpendicular to the c-axis [1120] and $\mu_{n||}$ denotes mobility parallel to c-axis [0001]. The high ratio of mobility in 6H-SiC has severe impact in current voltage characteristics of a DMOS device (not discussed in this research). Even though the anisotropic nature of mobility is not very significant in 4H-SiC, it has still been included in the simulation to obtain accurate results. In Silvaco ATLAS, Anisotropic Mobility is included by defining separate MOBILITY statements with separate mobility parameters perpendicular and parallel to c-axis [11]. The first statement defines the mobility parallel to c-axis and the second statement configures the mobility perpendicular to c-axis by using parameters ***N.ANGLE = 90°*** and ***P.ANGLE = 90°***. For 4H-SiC, Table 8 shows the perpendicular field mobility parameters that were used [21, 27, 28]

Table 8. Perpendicular Field Mobility Parameters

PARAMETER	*VALUE*
MU2N.CAUG	***947 $cm^2 V^{-1} s^{-1}$***
MU1N.CAUG	***5 $cm^2 V^{-1} s^{-1}$***
NCRITN.CAUG	***2 x 10^{17} cm^{-3}***
ALPHAN.CAUG	***-3***
BETAN.CAUG	***-3***
GAMMAN.CAUG	***0.0***
DELTAN.CAUG	***0.76***
MU2P.CAUG	***20 $cm^2 V^{-1} s^{-1}$***
MU1P.CAUG	***2.5 $cm^2 V^{-1} s^{-1}$***
NCRITP.CAUG	***1 x 10^{19} cm^{-3}***
ALPHAP.CAUG	***-3***
BETAP.CAUG	***-3***
GAMMAP.CAUG	***0.0***
DELTAP.CAUG	***0.5***

Default ATLAS values [11] were selected for the parameters which are not mentioned in Table 8.

11.7 THERMAL SIMULATION MODELS

11.7.1 LATTICE HEATING

Silvaco ATLAS incorporates GIGA© module for thermal simulations. GIGA implements Wachutka's thermodynamically rigorous model of Lattice heating [29], which accounts for Joule heating, heating, and cooling due to carrier generation and recombination, and the Peltier and Thomson effects. GIGA module is enabled by specifying ***LAT.TEMP*** parameter in the model statement. In order to include Generation/Recombination heating, Joule heating and Peltier Thomson effects, ***HEAT.FULL*** parameter is also included along with ***LAT.TEMP***.

Once the Lattice heating model is included with drift diffusion transport model, ATLAS uses the following heat equation two dimensionally [11]

$$C\frac{\partial T_L}{\partial t} = \nabla\left(\kappa \nabla T_L\right) + H \tag{25}$$

Equation 25. Heat Flow Equation

where C is the Heat capacitance per unit volume, κ is the thermal conductivity, T_L is the Lattice temperature and H is the heat generated. This configures the simulator to model the effective density of states for electron and holes as a function of the local Lattice temperature. The inclusion of Lattice Heating model requires at least one thermal boundary condition to be included in the program. It can be set using the ***THERMCONTACT*** statement. ***THERMCONTACT*** statement has parameters which includes the 2D x-y coordinates of the boundary, the temperature of the boundary and the Heat Transfer Coefficient (***ALPHA***). ALPHA is one of the most critical parameters of thermal simulation and its value has to be optimized based on the ambient simulation temperature and the power dissipation of the circuit [11]. A low value of alpha may result in a diverging solution and a very high may provide incorrect heat dissipation results. For this simulation, Table 9 shows the custom parameters that were specified for boundary condition

Table 9. Thermal Boundary Conditions

PARAMETER	*VALUE*
X.MIN	***0.0 µm***
X.MAX	***MAXIMUM WIDTH***
Y.MIN	***0.0 µm***
Y.MAX	***MAXIMUM DEPTH***
EXT.TEMP	***AMBIENT CONDITION***
ALPHA	***OPTIMIZED VALUE***

11.7.2 THERMAL CONDUCTIVITY

Thermal conductivity can be modeled in ATLAS using following techniques.

- Constant Thermal Conductivity
- Power Law: Thermal Conductivity as a function of temperature
- Polynomial Function: Thermal Conductivity as a function of temperature
- Reciprocal Function: Thermal Conductivity as a function of temperature

For this research, the polynomial function for thermal conducted was selected. Since thermal conductivity of 4H-SiC decreases with temperature, it provides a fairly accurate model for simulating heat transfer. The following function defines thermal conductivity [11]

$$\kappa(T_L) = \frac{1}{A_\kappa + B_\kappa T_L + C_\kappa T_L^2} \tag{26}$$

Equation 26. Polynomial Function for Thermal Conductivity

where A_κ, B_κ, C_κ are coefficients dependent on the material. The coefficients used in the above polynomial function for 4H-SiC are similar to 6H-SiC polytype and were selected for this simulation [21]. In Silvaco ATLAS, these coefficients are denoted by ***TC.A***, ***TC.B*** and ***TC.C*** parameters in the ***MATERIAL*** statement. Table 10 shows the custom parameters that were used for 4H-SiC [21]

Table 10. Thermal Conductivity Coefficients for 4H-SiC

PARAMETER	*VALUE*
TC.A	***2.5 x 10^{-3} cm K W^{-1}***
TC.B	***2.75 x 10^{-4} cm W^{-1}***
TC.C	***1.3 x 10^{-6} cm K^{-1} W^{-1}***

11.7.3 HEAT CAPACITY

Heat capacity was included in Silvaco ATLAS simulation via the following polynomial function [11]

$$C(T_L) = A_C + B_C T_L + C_C T_L^2 + D_C T_L^{-2} \quad (27)$$

Equation 27. Polynomial Function for Heat Capacity

where coefficients A_c, B_c, C_c and D_c are material dependent. The coefficients used in the above polynomial function for 4H-SiC are similar to 6H-SiC polytype and were selected for this simulation [21]. In Silvaco ATLAS, these coefficients are denotes by ***HC.A***, ***HC.B***, ***HC.C*** and ***HC.D*** and are used as parameters in the ***MATERIAL*** statement. Table 11 shows the custom parameters that were used for 4H-SiC [21]

Table 11. Heat Capacity Coefficients for 4H-SiC

PARAMETER	*VALUE*
HC.A	***1026 J Kg^{-1} K^{-1}***
HC.B	***0.201 J Kg^{-1} K^{-2}***
HC.C	***0 J Kg^{-1} K^{-3}***
HC.D	***-3.66 x 10^{7} J Kg^{-1} K***

11.8 IMPACT IONIZATION

Impact Ionization is described as the process in which carriers in the space charge region get accelerated by high electric field and they gain enough energy to generate more free carriers by collision with the atoms in the crystal Lattice. This process leads to avalanche breakdown and consequent destruction of power devices. There are several impact ionization models available in Silvaco ATLAS but the most commonly used on is the Selberherr model.

11.8.1 SELBERHERR MODEL

The ionization rate model proposed by Selberherr [30] is a modified version of Chynoweth's Law. The following equations describe the model [11]

$$\alpha_n = AN \exp\left\{-\left(\frac{BN}{E}\right)^{BETAN}\right\}$$

$$\alpha_p = AP \exp\left\{-\left(\frac{BP}{E}\right)^{BETAP}\right\} \quad (28)$$

Equation 28. Selberherr Impact Ionization Model

where E is the electric field in the direction of the current flow and parameters ***AN***, ***AP***, ***BN***, ***BP***, ***BETAN*** and ***BETAP*** are user definable parameters on the ***IMPACT*** statement. In Silvaco ATLAS, the above mentioned parameters can be expressed for a value of electric field ***EGRAN*** (V cm^{-1}) where for electric fields greater than ***EGRAN,*** the parameters are ***AN1***, ***AP1***, ***BN1*** and ***BP1*** and for electric fields less than ***EGRAN***, the parameters are ***AN2, AP2***, ***BN2*** and ***BP2***. In this research, impact parameters for field values both greater and less than ***EGRAN*** are considered to be equal. The impact ionization coefficients are a function of temperature in the Selberherr model as per the equations [11]

$$AN = AN_{1,2}\left(1 + A.NT\left[\left(\frac{T_L}{300}\right)^{M.ANT} - 1\right]\right)$$
$$AP = AP_{1,2}\left(1 + A.PT\left[\left(\frac{T_L}{300}\right)^{M.APT} - 1\right]\right)$$
$$BN = BN_{1,2}\left(1 + B.NT\left[\left(\frac{T_L}{300}\right)^{M.BNT} - 1\right]\right) \quad (29)$$
$$BP = BP_{1,2}\left(1 + B.PT\left[\left(\frac{T_L}{300}\right)^{M.BPT} - 1\right]\right)$$

Equation 29. Impact Ionization Coefficients as a function of Temperature

Since the default options were used for the parameters in Equation 29, it will not be discussed in this thesis. For 4H-SiC, Table 12 shows the impact parameters that were used for this simulation [27]

Table 12. Impact Ionization Coefficients

PARAMETER	*VALUE*
AN1	***3.44 x 10^6 cm^{-1}***
AN2	***3.44 x 10^6 cm^{-1}***
AP1	***2.58 x 10^7 V cm^{-1}***
AP2	***2.58 x 10^7 V cm^{-1}***
BN1	***3.5 x 10^6 cm^{-1}***
BN2	***3.5 x 10^6 cm^{-1}***
BP1	***1.7 x 10^7 V cm^{-1}***
BP2	***1.7 x 10^7 V cm^{-1}***

Default ATLAS values [11] were selected for the parameters which are not mentioned in Table 12.

11.8.2 ANISOTROPIC MODEL

Anisotropic Impact Ionization model for Silicon carbide can be enabled by using ***ANISO*** parameter in the ***IMPACT*** statement. The ionization rate is described by the following equation

$$\alpha\left(E_x\, E_y\right) = a \exp\left(-c \sqrt{1 - A^2 c^2 \left(\frac{E_x\, E_y}{b_x\, b_y} \right)^2} \right) \tag{30}$$

Equation 30. Anisotropic Impact Ionization Equation

where E_x and E_y are electric field magnitudes in x and y directions. The parameters ***a, c, A, b_x*** and ***b_y*** are dependent upon the crystal orientation. The crystal orientation for 4H-SiC can be 0001 (default) or 1120 which can be specified using the parameter ***SIC4H001*** or ***SIC4H1120*** in the ***IMPACT*** statement. For this research, the default ATLAS values were used [11].

CHAPTER 12

10kV 1A 4H-SiC PIN DIODE SIMULATION

Silicon Carbide is a Wide Bandgap semiconductor and in order to optimize the simulation process, it was necessary to simulate a less complex device like PIN diode before simulating a MOSFET cell. This would help in optimizing the simulation parameters which would simplify the subsequent simulations.

12.1 PIN DIODE DESIGN

The PIN diode was designed for a Parallel Plane Blocking voltage of 10kV and a rated forward current of 1A. In a power device, the entire blocking voltage is supported across the drift region, the following equation was used to determine the drift region doping concentration

$$N_{Drift} = \left(\frac{3 \times 10^{15}}{BV_{PP}} \right)^{\frac{4}{3}} cm^{-3} \quad (31)$$

Equation 31. Drift Region Doping Concentration

where BV_{pp} is the parallel plane breakdown voltage [31]. To make the design and simulation simple, the PIN diode had a parallel plane structure. In this case, a parallel plane breakdown voltage of 10kV resulted in a calculated doping concentration value of 2×10^{15} cm^{-3}.

Referring to the basics of a PN junction, the reverse biasing of a PN junction results in the widening of the depletion region. Hence, the drift region in PIN diode structure must be wide enough to support the depletion region while blocking 10kV. The minimum thickness of the drift region can be calculated using the following equation

$$t_{Drift} = \sqrt{\frac{2 * \varepsilon_{SiC} * BV_{PP}}{q_e * N_{Drift}}} \quad (32)$$

Equation 32. Drift Region Thickness

where ε_{SiC} is the permittivity of 4H-SiC, q_e is the electronic charge [31]. For the given parameters of 4H-SiC and the calculated drift region doping concentration, the minimum value of drift region thickness was obtained as 73.34 µm. The P+ Anode and N+ cathode/substrate were heavily doped p-type and n-type semiconductors respectively with a doping concentration of 2×10^{19} cm^{-3}. The doping concentration for the P+ Anode region helps us to calculate the minimum thickness of the P+ region. This is calculated by knowing the maximum width of the depletion region extending into the heavily doped P+ region using the following equation.

$$t_{P+} = \sqrt{\frac{2 * \varepsilon_{SiC} * BV_{PP}}{q_e * N_A}} \tag{33}$$

Equation 33. P+ Region Thickness

This equation is the same which is used for calculating the drift region thickness except for the fact that the Drift region doping concentration is replaced by the P+ region doping concentration [31]. The above equation resulted in a value of 0.735 µm. For Simulation purpose, the extrinsic Debye length [32] was calculated using the following equation to get an estimate for the mesh dimensions for the different regions in the PIN diode structure.

$$L_{Debye} = \sqrt{\frac{\varepsilon k_B T}{q^2 N}} \tag{34}$$

Equation 34. Debye Length

The extrinsic Debye length calculation resulted in a value of 0.836 nm for the P+ region and 0.083 µm for the N- Drift region. However, due to simulation time tradeoff, these values were impractical for actual simulation. In reality, a power device substrate has a thickness of 250 µm to 500 µm to provide mechanical strength to the device and reduce the substrate resistance. In this research simulation, the substrate was given a thickness of 20 µm to reduce the total number of mesh points and increase the simulation speed.

12.2 DEVICE STRUCTURE

For Simulation purpose, the dimensions of the PIN diode were chosen with a small buffer to compensate for variations in actual parameters. The P+ Anode region was 3 µm deep, the N- drift region was 77 µm thick and the N+ substrate was 20 µm thick. Fig. 13 shows a 3D structure of the parallel plane PIN diode. Parameters like the Drift region doping concentration and mesh design had to be optimized to obtain the desired diode rating. The actual optimized value of Drift region doping used in simulation was 1.2 x 10^{15} cm^{-3} and a doping of 2 x 10^{19} cm^{-3} was used for P+ region and substrate.

Since ATLAS 2D simulator was used, the third dimension (in z direction) was used to scale the output current to achieve the designed rating. This was implemented using the *Width* command [11]. It took several simulation cycles to optimize the Width in z direction and obtain 1A Forward current.

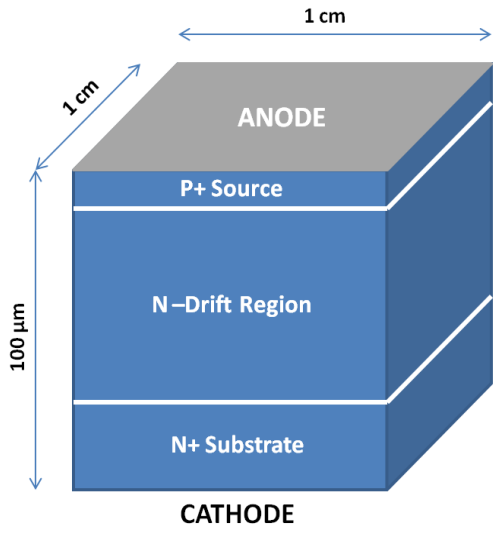

Figure 13. 3D Diagram of 10kV PIN Diode

Fig. 14 structure mesh was created in ATLAS using Deckbuild Graphical User Interface (GUI) program [33]. The mesh was made fine in the critical regions like the junction between the P+ region and the N- drift region and underneath the anode electrode while the drift region and substrate mesh was made coarse.

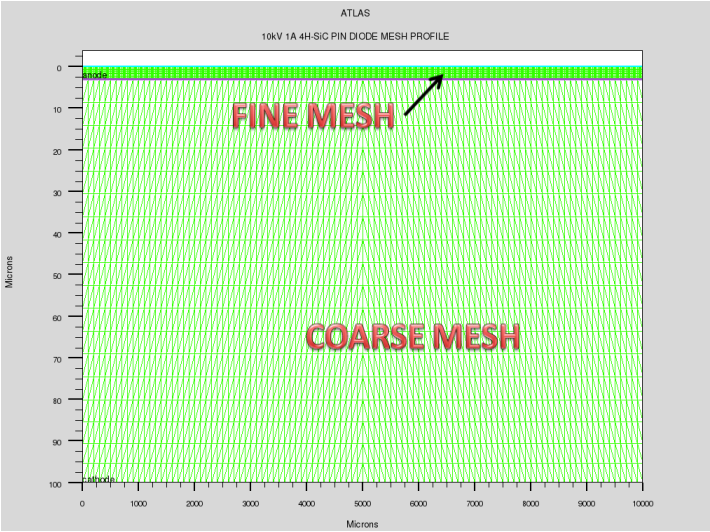

Figure 14. PIN Diode MESH Profile

12.3 DOPING PROFILE

The Doping Profile (Fig. 15) shows the impurity concentration across the device structure. The entire device mesh was first doped with the doping concentration value which covers majority of the device (in this case, it's the N - Drift Region doping). After this, the heavily doped regions were created.

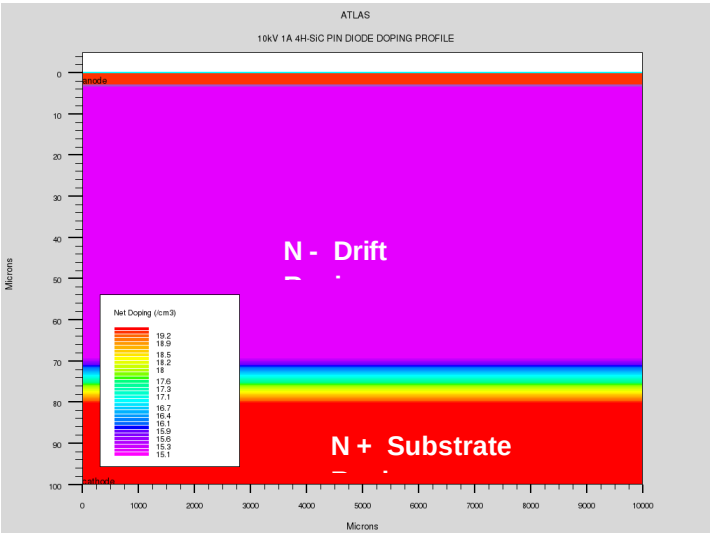

Figure 15. PIN Diode DOPING Profile

The Contour plot is color coded where Red color indicates the maximum doping concentration regions (P+ Anode and the N+ Substrate) and Purple indicates the least doping concentration area (N - Drift Region). The discontinuity of doping at the junction between the N- Drift Region and N+ Substrate is due to the coarse mesh distribution in that area.

12.4 BREAKDOWN SIMULATION

The initial Breakdown simulation was carried out using the default simulator settings. As discussed before, due to the low simulator precision issues, the device never underwent overvoltage breakdown. The following plot (Fig. 16) shows the Breakdown curve with the low precision error.

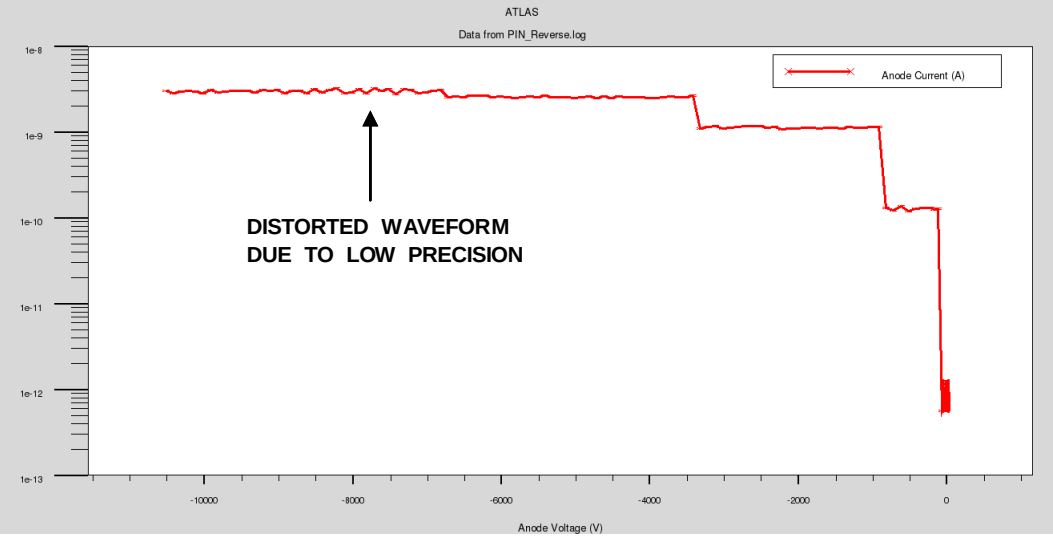

Figure 16. Low Precision Breakdown Simulation

This error was rectified by configuring the simulator to use 128-bit extended precision. Fig. 17 plot was obtained by simulating the Breakdown characteristics for 27°C, 150°C and 250°C (Displayed on Kelvin scale). This was done using the ***solve*** statement in ATLAS [11]. The negative anode voltage was increased in proper bias steps which increases the reverse bias on the diode.

It can be observed in the plot that once the anode voltage reaches -1200V (or cathode voltage of 1200V), the magnitude of anode current shoots up which indicates breakdown. The breakdown simulation can be extended to demonstrate higher current magnitudes post breakdown but at the expense of long simulation time. The anode current is shown on a logarithmic scale.

Normally the impact ionization coefficient for electron is higher than holes but for Silicon Carbide, holes have a higher impact ionization coefficient which results in a positive temperature gradient for breakdown voltage [3, 34]. The results show that even at elevated temperature, the breakdown voltage is almost constant but the device leakage current increases by several orders of magnitude. The stability of breakdown voltage at elevated temperature is a desirable feature for Power Devices.

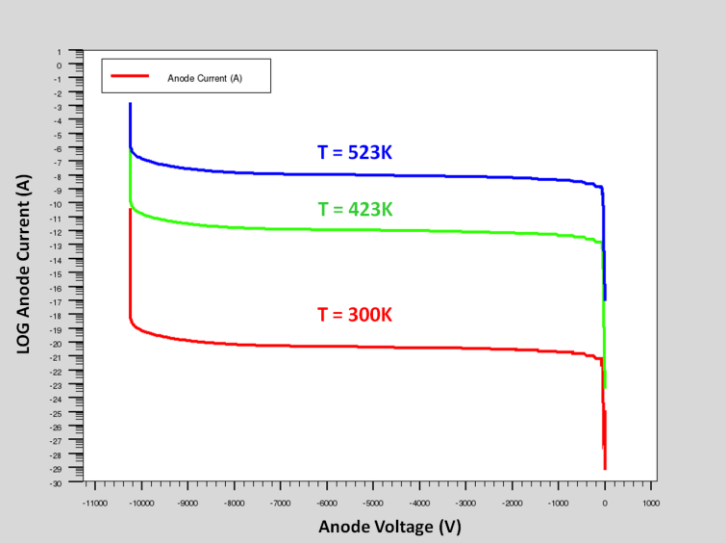

Figure 17. Extended Precision Breakdown Voltage Simulation

The Critical Electric Field for 4H-SiC Silicon Carbide is in the range of 2 - 3 MV cm^{-1}. The breakdown simulation program was configured to save the simulation data into a structure file after the simulation is complete. This enables the user to analyze the various electrical quantities which got altered after the simulation. Fig. 18 shows the electric field intensity contour plot for the device post breakdown.

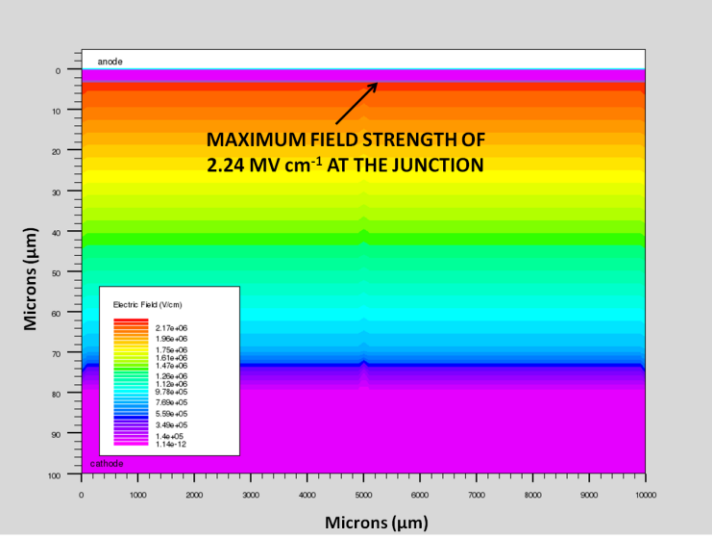

Figure 18. PIN Diode Breakdown Electric Field

12.5 FORWARD CHARACTERISTICS

The PIN diode Forward Characteristics were simulated using the solve statement. The positive anode voltage was slowly increased in proper bias steps to forward bias the diode and obtain the I-V characteristics. Fig. 19 shows the various regions in the on-state characteristics of a PIN rectifier

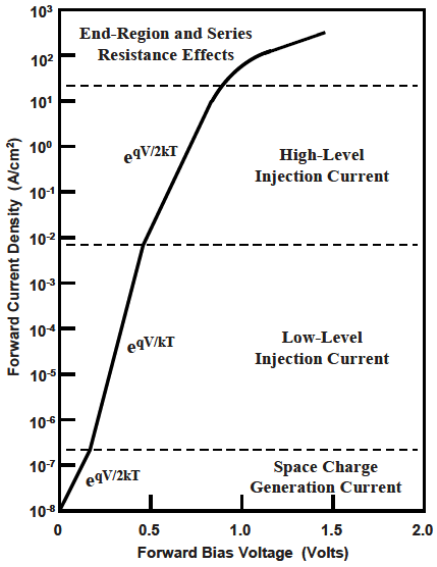

Figure 19. On-State Characteristics for PIN Rectifier [35]

The plot was configured to show anode current on logarithmic scale. This was done as the log scale gives more detailed information about the on state device characteristics including the High Level injection Current and the End Region and Series resistance effects [35]. By comparing the simulation results of Fig. 20 with the on state characteristics in Fig. 19, it can be observed that once the diode forward current magnitude exceeds the rated 1A, the end region series resistance effect becomes significant and the on state voltage drop increases with any further increase in forward current resulting in high on state power dissipation.

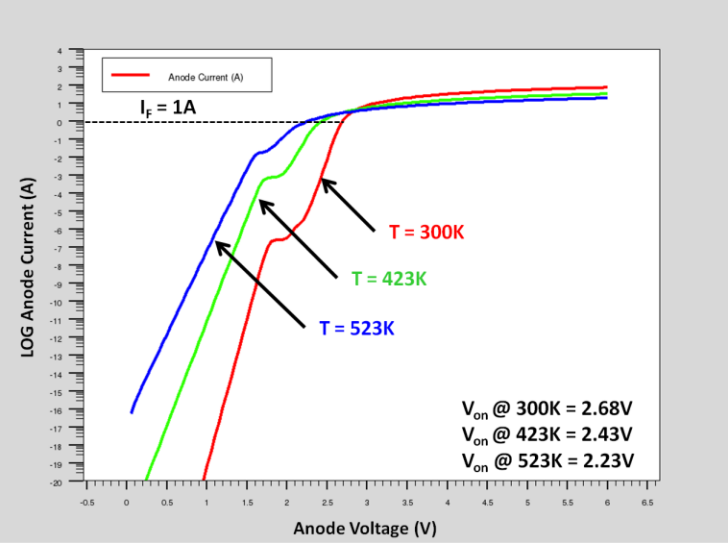

Figure 20. PIN Diode Forward Characteristics

The forward characteristics were simulated for ambient temperature conditions of 27°C, 150°C and 250°C (Displayed on Kelvin scale). The on-state voltage for a PIN diode is given by the equation

$$V_{ON} = \frac{k_B T}{q} \ln\left(\frac{n(+d) \cdot n(-d)}{n_i^2}\right) \tag{35}$$

Equation 35. 4H-SiC PIN Diode On-State Voltage

where n(+d) and n(-d) are the injected carrier concentrations which can be assumed to be similar and equal to the drift region doping concentration mentioned in section

12.1 [35]. Using the value of intrinsic concentration calculated in section 3.4, the on state voltage of 4H-SiC PIN diode is calculated to be 3.00V at 27°C which is about four times the on state voltage drop for silicon. At 150°C, the calculated on state voltage drop was 2.73V and at 250°C the calculated on state voltage was about 2.5V. As the ambient temperature increases, the on state voltage drop gets slightly reduced at the same magnitude of 1A forward current due to increase in the intrinsic carrier concentration. The maximum on state voltage of 2.68V was obtained after simulation at 27°C which is much larger than the Silicon counterpart. At elevated temperatures of 150°C and 250°C, the obtained values of on state voltage drop were 2.43V and 2.23V.

12.6 LATTICE HEAT SIMULATION UNDER STEADY STATE

In order to understand the Lattice heating effects on Silicon Carbide, the PIN diode was simulated for the forward characteristics as in section 12.4 but this time, the Lattice heating models were added. Models ***LAT.TEMP*** and ***HEAT.FULL*** were added to the program code and a value of 10 W cm^{-2} K^{-1} was selected for heat transfer coefficient (***ALPHA***) [11]. This value of heat transfer coefficient was optimized after several execution iterations. The boundary condition/Heat sink was placed on the entire 2D device structure. Fig. 21 shows the formation of a hot spot on the device Lattice once the forward current exceeds the rated current and the end region series resistance becomes significant.

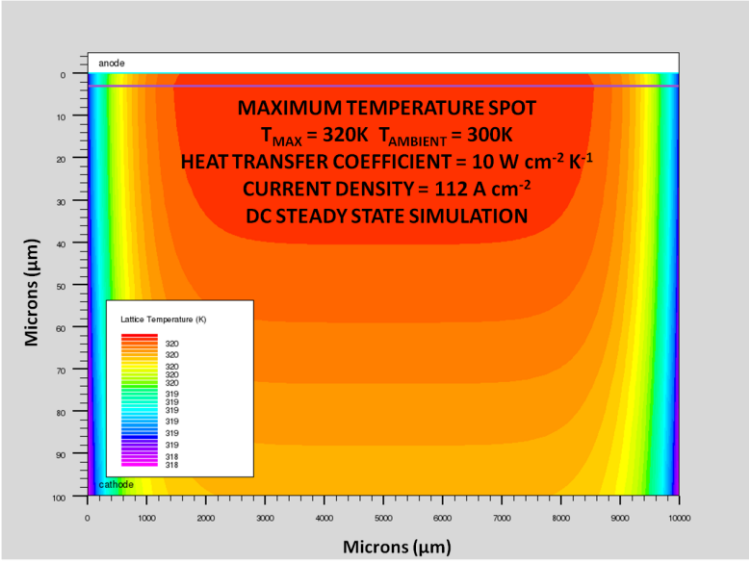

Figure 21. PIN Diode Lattice Heating

At a current density of 112A cm^{-2}, the maximum observed Lattice temperature was 320K and the minimum Lattice temperature was 318K given the ambient condition to be 300K. The Lattice temperature simulation was performed under steady state when the heat dissipated is continuous in nature and not for a short period of time as in the scenario of transient simulation. The maximum temperature rise is concentrated in the region directly below the electrode and the temperature gradient reduces thereafter. This happens due to the variation in the value of thermal conductivity at

elevated temperature. At 300K, 4H-SiC has a thermal conductivity of 4.95 W $cm^{-1} K^{-1}$ (calculated using Equation 26).

Fig. 22 shows the variation in thermal conductivity for the same simulation. The maximum thermal conductivity (4.51 W $cm^{-1} K^{-1}$) is closer to the vertical edges of the device and it keeps decreasing towards the inner region of the Lattice to a minimum (4.47 W $cm^{-1} K^{-1}$) where the temperature is maximum. These values can be verified using Equation 26.

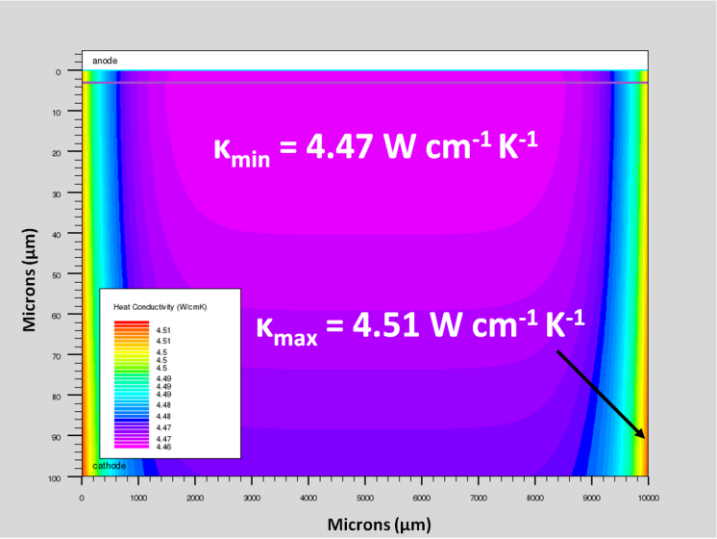

Figure 22. Thermal Conductivity Variation in PIN Diode Lattice Heating

CHAPTER 13

1200V 1A 4H-SiC N-CHANNEL D-MOSFET

The 4H-SiC PIN diode simulation helped in overcoming some major issues related to wide Bandgap semiconductor simulation. One of the major challenges with MOSFET simulation is the fact that a Power MOSFET consists of millions of cells which renders it almost impossible to simulate a complete device. However, it is feasible to simulate fewer number of cells (much less than 10) to understand the behavior of the device. In this thesis, a two dimensional half cell D-MOSFET was simulated considering the computational speed and simulation resources.

13.1 HALF CELL DESIGN

The Power MOSFET cell had to be designed for a blocking voltage of 1200V and a maximum drain current of 1A at current density of 100A cm^{-2}. Unlike the parallel plane PIN diode breakdown voltage, in case of a MOSFET, due to edge terminations, the breakdown voltage is related to the parallel plane breakdown voltage via the following equation [36]

$$BV_{Actual} = 0.8\left(BV_{PP}\right) \tag{36}$$

Equation 36. MOSFET Breakdown Voltage

Since the actual breakdown voltage is only 80% of the parallel plane breakdown voltage, the parallel plane breakdown voltage was considered to be 1500V in order to obtain a breakdown voltage of 1200V.

Equation 31 was used to calculate the required doping concentration of the drift region to support the blocking voltage. The drift region doping concentration was calculated 2.52 x 10^{16} cm^{-3}. Equation 32 was used to calculate the drift region thickness required to support the blocking voltage. The calculated value corresponds to a thickness of 8.02 µm. The P-Base region doping was calculated and optimized after considering the following tradeoff

- Increasing the P-Base region doping concentration results in a rapid increase in the gate threshold voltage since higher gate voltage is required to attract electrons (minority carriers) from the heavily doped p-type semiconductor to form the channel. Due to heavy doping in P-Base region, the depth of the P-Base region can be made small as the depletion layer would extend mainly into the drift region during blocking state. This reduced depth, reduces the channel length thereby reducing the on state resistance.

- Decreasing the P-base region doping decreases the threshold voltage since lower gate voltage is required to pull electrons (minority carriers) from the lightly doped p-type semiconductor to form the channel. However, the reduced threshold voltage is obtained at the expense of reduced breakdown voltage. The reduced P-Base region doping favors the extension of the depletion region into the P-Base region and causes punch through breakdown. This can be avoided by increasing the depth of the P-Base region but at the expense of increased channel length and hence on state resistance.

Hence the P-Base region doping has to be designed considering the breakdown voltage, threshold voltage and the on state resistance. The half cell was designed for a threshold voltage of 6V and the following equation was used to optimize the threshold voltage by varying the P-Base Region doping [36].

$$V_{th} = \frac{t_{OX}}{\varepsilon_{OX}} \sqrt{4 \varepsilon_{SiC} k_B T_L N_A \ln\left(\frac{N_A}{n_i}\right)} \tag{37}$$

Equation 37. Gate Threshold Voltage

For an oxide layer thickness of 30nm, a P-Base doping concentration of 5.3 x 10^{17} cm^{-3} was calculated. Using Equation 33, the minimum thickness of P-Base region was calculated as 1.75 µm.

13.2 HALF CELL STRUCTURE

For Simulation purpose, the design parameters of the MOSFET were chosen with a small buffer to compensate for variations in actual parameters. The N- Drift region doping value was optimized to 2.1 x 10^{16} cm^{-3} and a value of 5 x 10^{17} cm^{-3} was used for the P-Base region doping concentration. The N+ source and substrate were heavily doped to a concentration value of 1 x 10^{19} cm^{-3}. The physical dimensions of the cell were designed after referring to various designs in the Silicon Carbide Power Devices textbook [37]. The cell pitch for half cell was selected as 4 µm, the width of the gate electrode was selected to be 3µm which is the same as the width of the polysilicon window, the width of the contact window to N+ source and P-base region is 0.75 µm. The P-Base region width and depth was chosen to be 3 µm each which gave a desired channel length of 2 µm. The JFET region was selected to be 1 µm wide. The depth of the N+ source region and Substrate were 1 µm and the 10 µm respectively. The Drift region thickness was optimized to 12 µm.

The electrode material was configured to be Aluminum. The D-MOSFET structure inherently gives rise to a parasitic NPN Bipolar Junction Transistor (BJT) between the Source region, the P-Base region and the Drift region where the Source forms the Emitter, the P-base region forms the Base and the Drain/Substrate forms the Collector. If this BJT turns ON, the gate will lose control over the drain current and can lead to device destruction. This process is called Latch-up [38]. In order to prevent this, the Source and electrode and the p-Base region are shorted together which in turn shorts the emitter and base of the parasitic BJT thus preventing Latch-up Fig. 23 shows the physical dimensions of the cell. The mesh profile for the MOSFET cell is shown in Fig. 24.

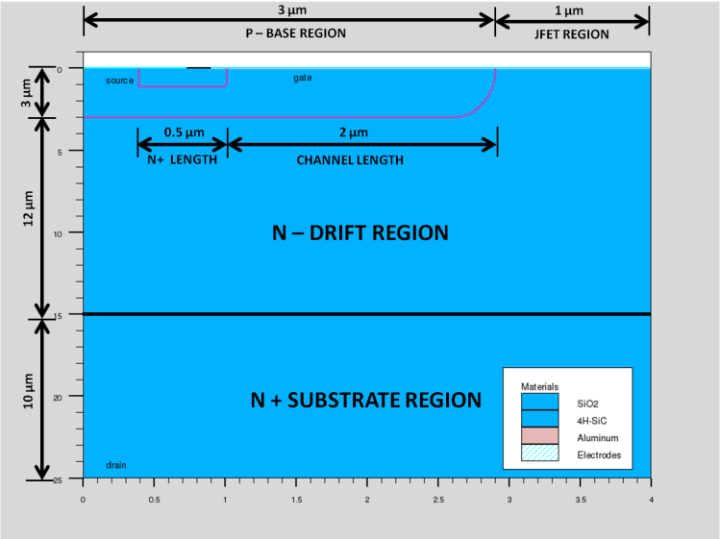

Figure 23. MOSFET Cell Dimensions

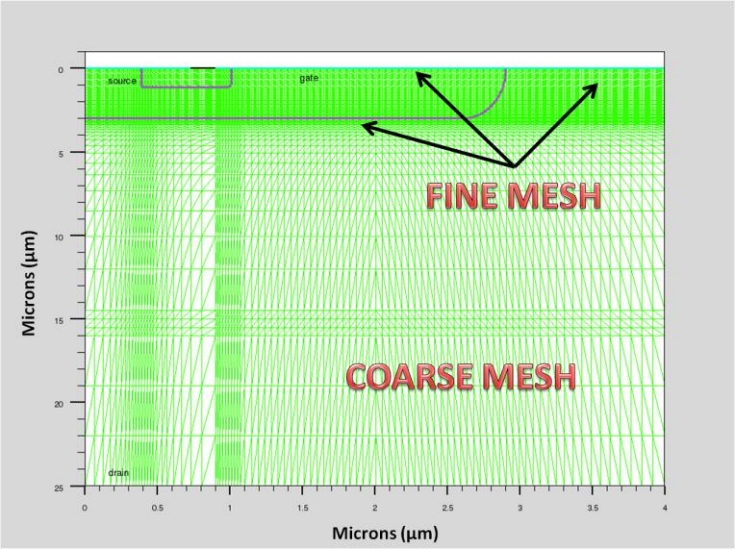

Figure 24. MOSFET Cell MESH Profile

The mesh profile was optimized after several iterations to have maximum simulation efficiency. The mesh profile had zero obtuse triangles and was made fine in the critical regions including the channel, JFET region and the junction between P-Base region and Drift region. The Gate oxide region is shown in Fig. 25 (enlarged view). The thickness of 30 nm was selected after considering the design tradeoffs.

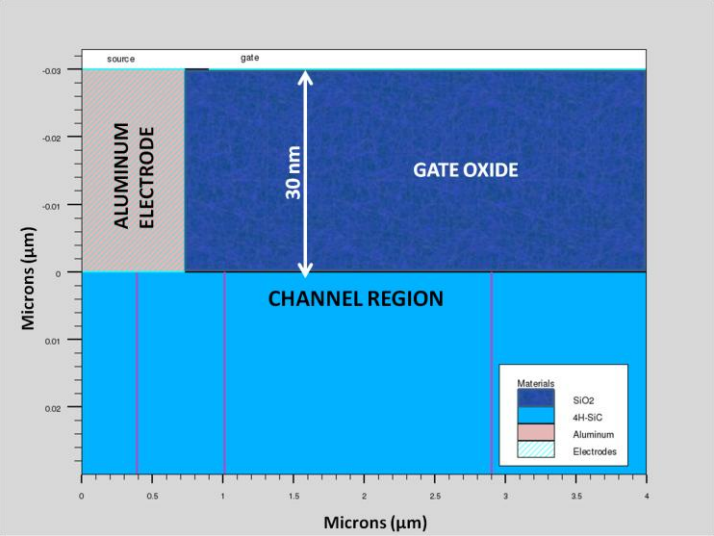

Figure 25. MOSFET Gate Oxide

13.3 DOPING PROFILE

Fig. 26 shows the doping profile for the MOSFET cell. The N+ source, N - Drift and Substrate regions were uniformly doped and the P-Base region was doped using Gaussian profile.

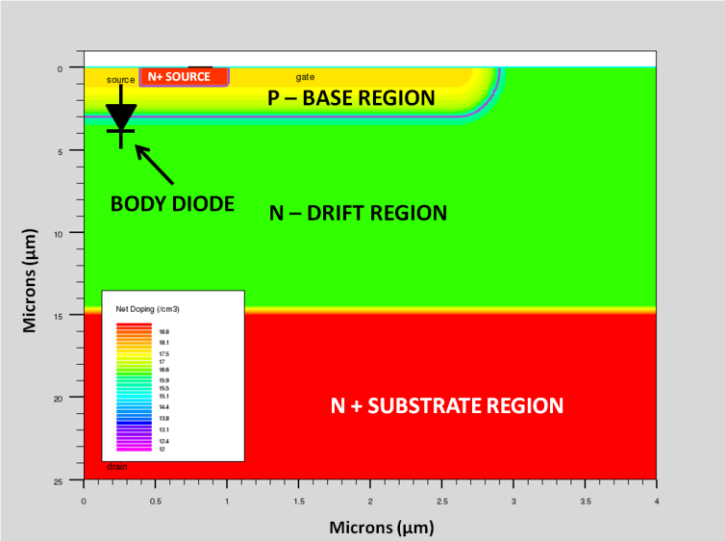

Figure 26. MOSFET Doping Profile

13.4 BREAKDOWN SIMULATION

The breakdown simulation (Fig. 27) for Power MOSFET was done using 128-bit extended precision. The simulation was performed at ambient temperatures of 27°C, 150°C and 250°C using a cell width (along z-axis for 2D simulation) of 4 µm. Since holes have a higher impact ionization rate than electron in Silicon Carbide, the breakdown voltage almost remains constant even at elevated temperatures. This is due to the positive temperature coefficient of holes in case of Silicon Carbide [3, 34].

The Maximum electric field of 2.7MV cm^{-1} during breakdown simulation at 300K, is centered at the junction between the P-base region and the drift region. As it can be observed in the Electric Field plot (Fig. 28), that the electric field extends into the P-Base region, which was why the depth of the P-base region was selected more than the calculated value.

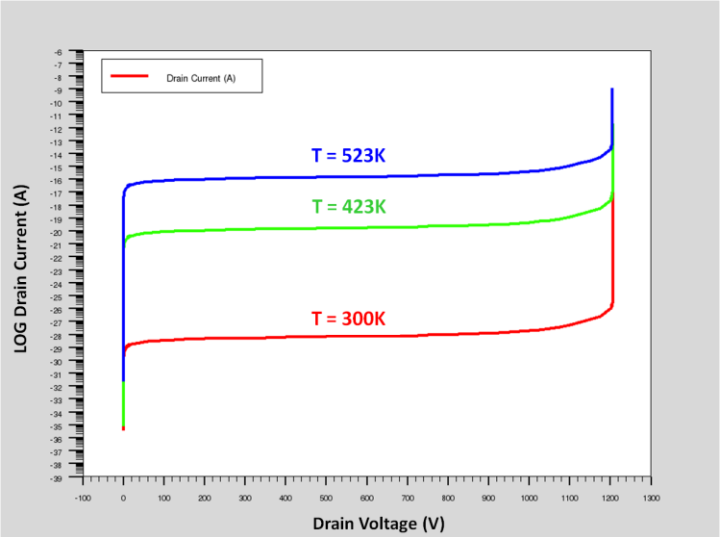

Figure 27. MOSFET Breakdown Simulation

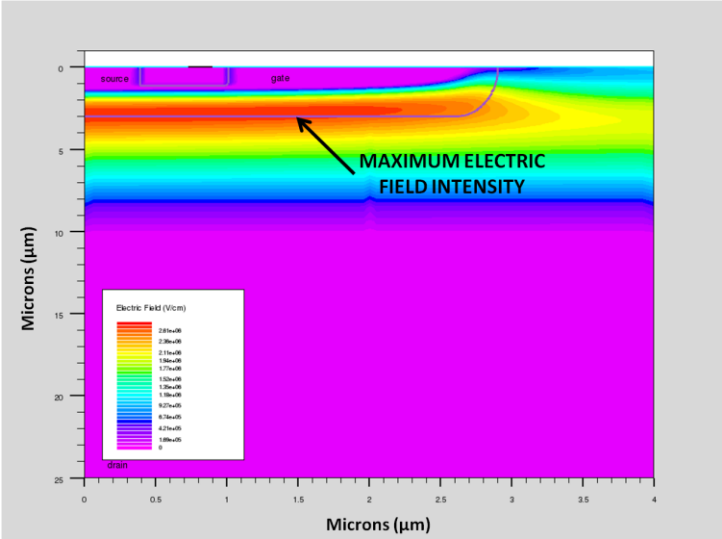

Figure 28. Breakdown Electric Field

The Impact generation plot (Fig. 29) shows the Lattice location where maximum carriers are generated due to impact ionization at 300K. The maximum value of impact generation rate (α) was obtained as 10^{18} cm^{-3} s^{-1}.

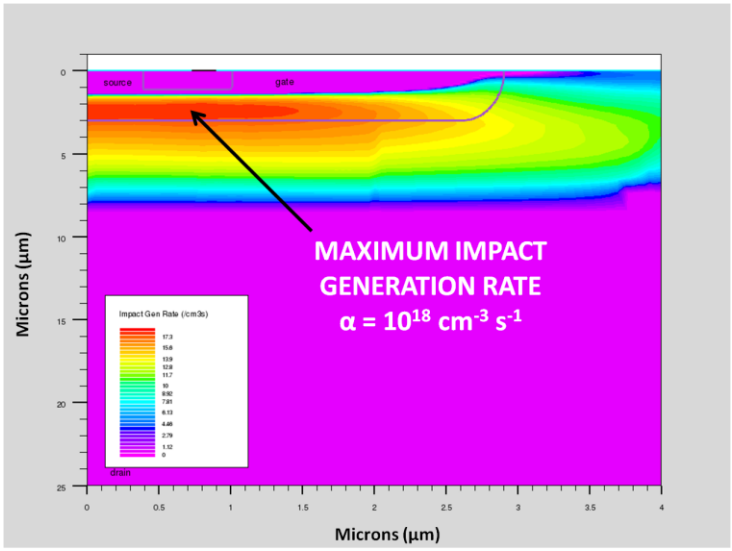

Figure 29. Impact Generation Rate

13.5 I_D VS V_{DS} CHARACTERISTICS

One of the most important characteristics for a MOSFET is the Drain Current vs. Drain Voltage (at constant Gate to Source voltage) family of curves. The family of curves was obtained for ambient temperature conditions of 27°C, 150°C and 250°C using a cell width (along z-axis for 2D simulation) of 4 µm. Fig. 30, 31 and 32 show the Current Voltage characteristics for D-MOSFET.

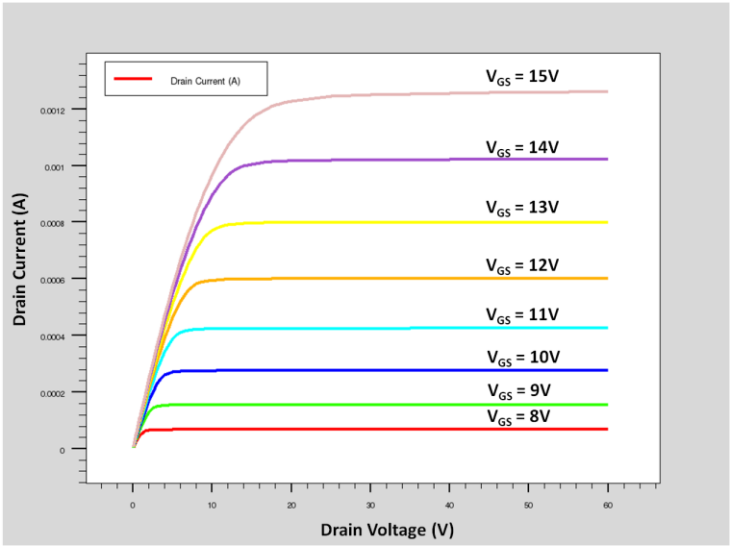

Figure 30. Current Voltage Characteristics @ 300K

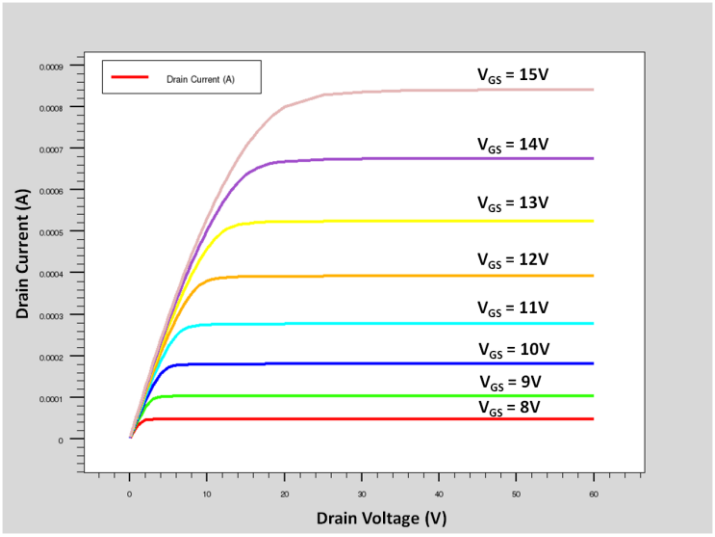

Figure 31. Current Voltage Characteristics @ 423K

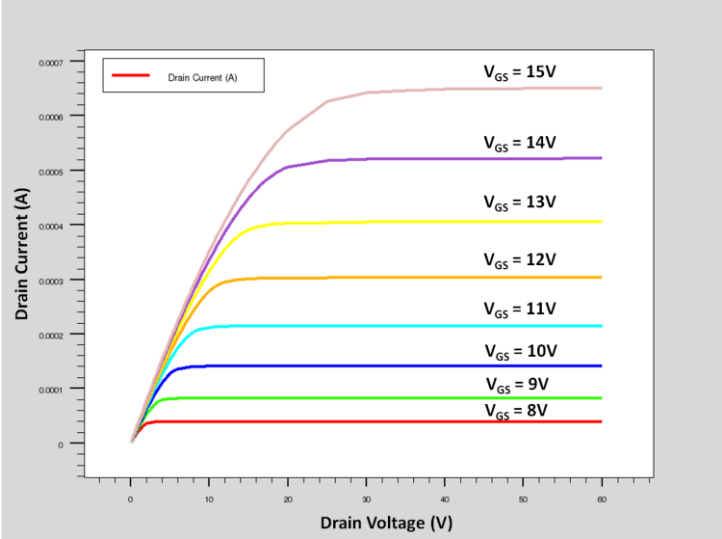

Figure 32. Current Voltage Characteristics @ 523K

The Device threshold voltage was observed to be 6V hence, in this simulation, the gate voltage was varied linearly in steps of 1V starting from 8V. As the ambient temperature increases, the device on state resistance increases and the current decreases. This is a favorable feature for MOSFETs as it automatically regulates current when multiple devices are used in parallel.

13.6 I_D VS V_{GS} CHARACTERISTICS

The transfer characteristics (Drain Current vs. Gate to Source voltage) were simulated in ATLAS for ambient temperature conditions of 27°C, 150°C and 250°C using a cell width (along z-axis for 2D simulation) of 4 µm. Figures 33, 34 and 35 shows the transfer characteristics for D-MOSFET for Drain to Source voltage of 20V, 40V and 60V.

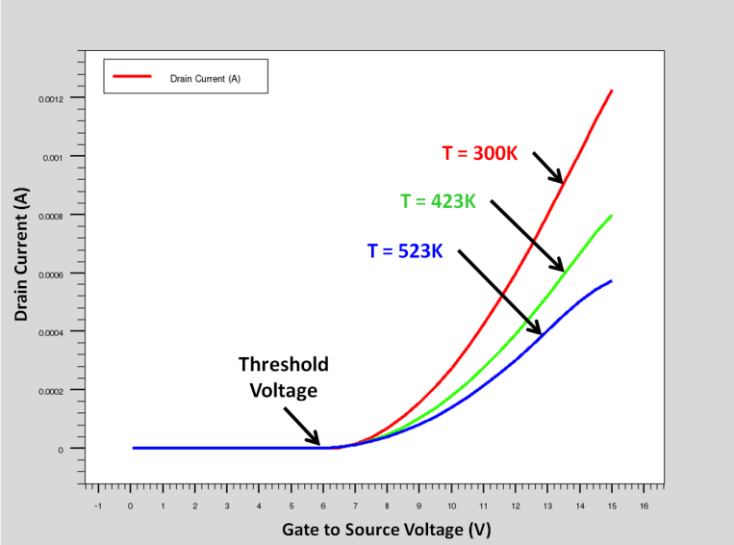

Figure 33. Transfer Characteristics @ V_{ds}=20V

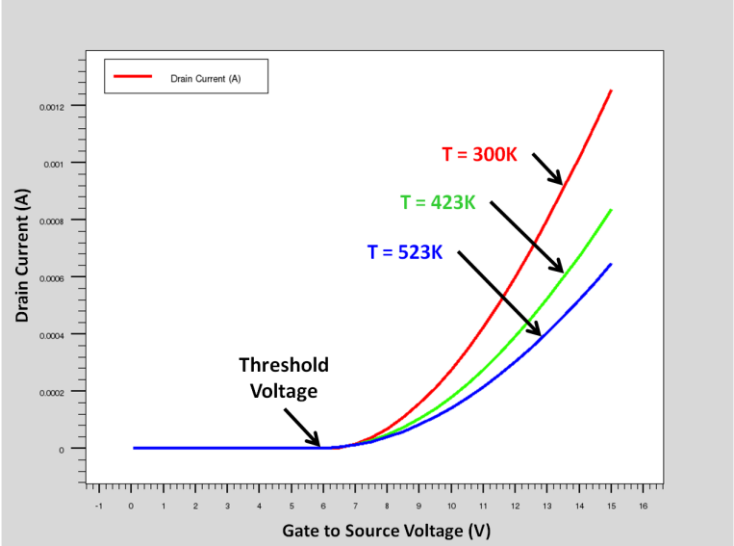

Figure 34. Transfer Characteristics @ V_{ds}=40V

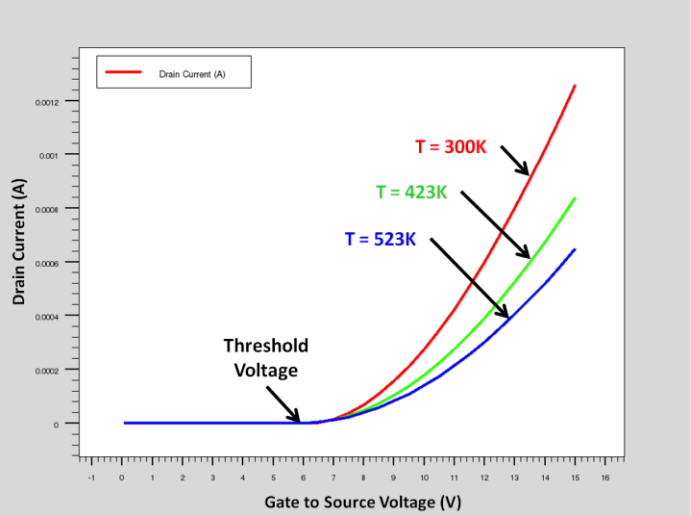

Figure 35. Transfer Characteristics @ V_{ds}=60V

13.7 BODY DIODE CHARACTERISTICS

The D-MOSFET design inherently creates a parasitic PN junction in its structure. This PN junction is formed between the P-Base region and the drift region. This gives rise to an integral PIN Body diode within the MOSFET with its cathode connected to the N-MOSFET Drain and the Anode connected to the N-MOSFET source. This diode is useful when the MOSFET is used in H-bridge configuration. Hence it is important to study the characteristics of this parasitic diode. Fig. 36 shows the Current Flowlines plot when the body diode is conducting [11]. The Current Flowlines plot generated by Silvaco© ATLAS (by specifying ***FLOWLINES*** parameter in the ***OUTPUT*** statement) is a normalized plot where the color coded intensity of current flow in the semiconductor Lattice is shown.

In Fig. 36, the path of current is maximum where the P-base region aligns with the Drain. However, the characteristics of the body diode are not similar to the MOSFET characteristics as the current flow is though the bulk of the semiconductor and not through the channel.

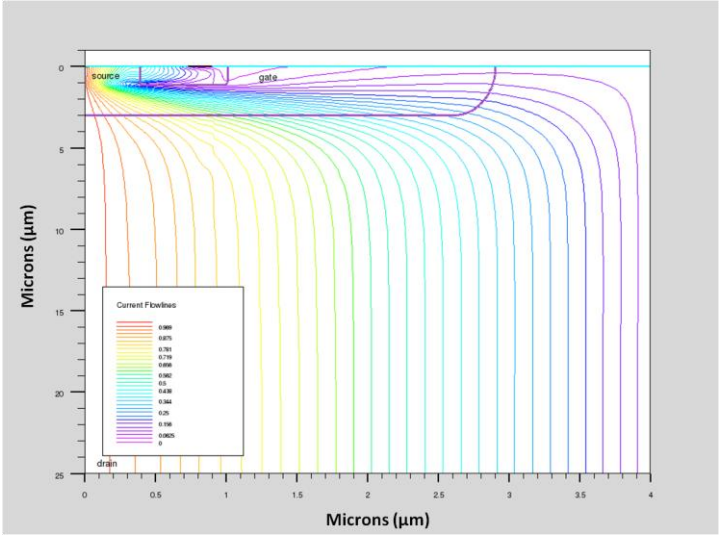

Figure 36. Body Diode Current Flowlines

Fig. 37 shows the forward characteristics of the body diode simulated for ambient temperature conditions of 27°C, 150°C and 250°C. This was simulated by increasing the Source voltage linearly while the Drain was grounded. The Source current is shown on a logarithmic scale in order to analyze the various regions of operation of a PIN diode as compared to Fig. 19. The results obtained for the body diode are similar to the results obtained for the 10kV 1A PIN diode characteristics in Fig. 20. However the current magnitude is less as the body diode was simulated using cell width (scaling factor along z-axis for 2D simulation) of 4 µm.

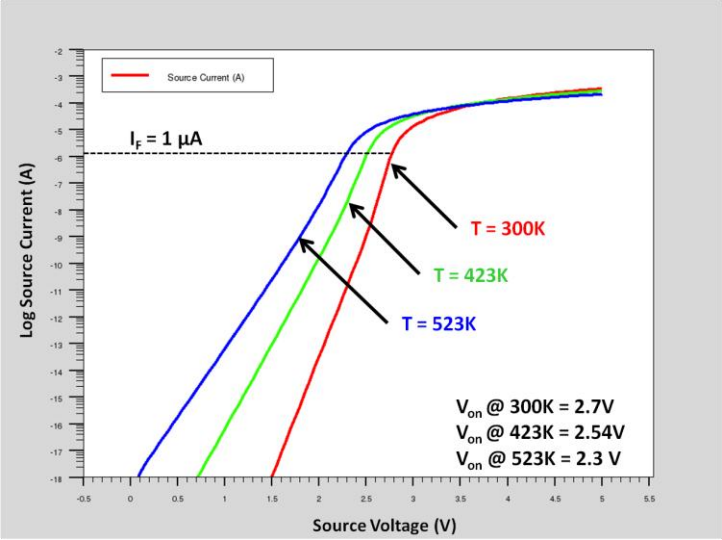

Figure 37. Body Diode Forward Characteristics

13.8 DESIGN FOR CURRENT DENSITY 100 A cm^{-2}

As per the Design requirements of this research, the rated current density of the MOSFET had to be 100A cm^{-2} at the rated Drain current of 1A. In ATLAS 2D simulations, the third dimension or the z-axis is by default 1 µm long. This results in unrealistically high current densities since the area for vertical current flow devices is x (length) times the z (length). For the MOSFET half cell, the x is 4µm long, y is 25 µm long and z is default. In Silvaco ATLAS, a parameter called ***WIDTH*** in the ***AMOSFET*** mixed mode statement can be used to increase the z axis length to obtain the 3D effect [11]. The width parameter scales the terminal quantities like current, contact resistance etc.. When Silvaco Tonyplot is used to view the structure file for current density distribution, the area used to calculate the current density, gets scaled by the number specified in the width parameter. The value of width parameter was used in this research to obtain the required current density.

In order to obtain 100A cm^{-2} current density at 1A drain current, the circuit shown in Fig. 38 was simulated in Silvaco ATLAS in DC mixed mode. In the circuit, the Device Under Test (D.U.T) is the D-MOSFET. It is simple circuit where a constant 1A drain current will flow through the MOSFET once it turns on.

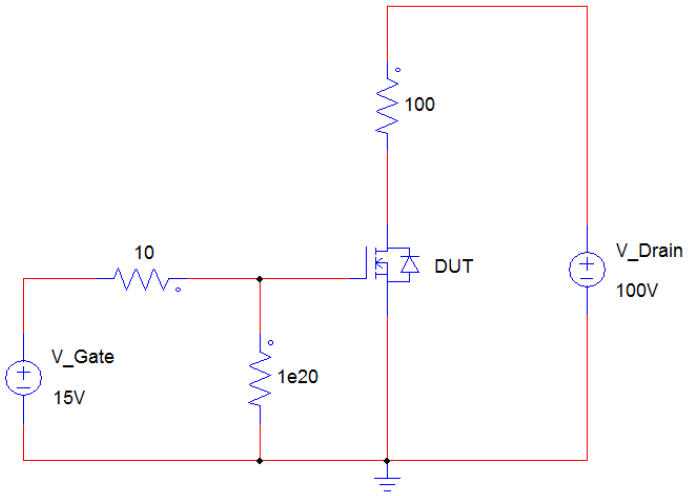

Figure 38. Circuit to Set Current Density

Since the maximum current density for a MOS device is at the channel region, the channel current density was monitored after each program execution. The value of width parameter was altered each time until the channel current density was 100A cm^{-2} when 1A current is flowing through the device. A width parameter value of 5.75 x 10^7 resulted in the required current density. This value of width was used in the transient analysis. Fig. 39 shows the channel current density at 100A cm^{-2} extracted using the PROBE feature of Tonyplot.

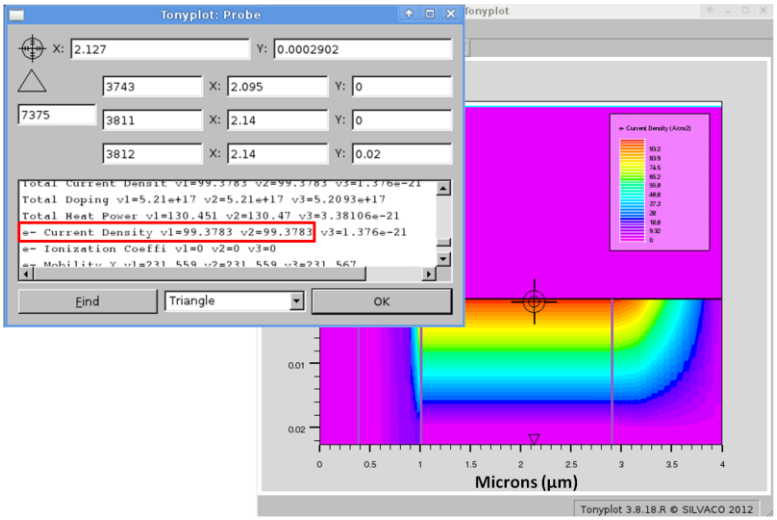

Figure 39. 100A cm^{-2} Current Density

CHAPTER 14

TRANSIENT ANAYLYSIS OF D-MOSFET

The transient analysis was performed using an series RLC ring down circuit to generate the required current pulse. Since a Power device can handle about ten times the rated current in pulsed state, the transient analysis was performed at five times as well as ten times the rated current density i.e. 500A cm^{-2} and 1000A cm^{-2} respectively. To understand the effect of ambient temperature, the simulations were performed at 27°C and 150°C.

14.1 PSPICE SIMULATION OF RLC RING DOWN CIRCUIT

In the initial phase of transient analysis, the series RLC ring down circuit was simulated using PSPICE student version. Equation 38 was used to calculate the required frequency of the pulse.

$$f_{RLC} = \frac{1}{2\pi\sqrt{LC}} \tag{38}$$

Equation 38. Frequency of RLC circuit

In order to obtain a critically damped waveform, the combination of R, L and C should be selected such that the damping coefficient is one as per equation 39.

$$\zeta\left(Damping\ Coefficient\right) = \frac{R}{2}\sqrt{\frac{C}{L}} = 1 \tag{39}$$

Equation 39. Damping Coefficient

Table 13 shows the values of L and C required to obtain various current pulse width at different peak current levels.

Table 13. RLC Ring Down Circuit Parameters

PULSE WIDTH	*PEAK CURRENT*	*R*	*L*	*C*	*V*
50 µs	***5 A***	***4 Ω***	***40 µH***	***10 µF***	***28V***
100 µs	***5 A***	***4 Ω***	***80 µH***	***20 µF***	***28V***
200 µs	***5 A***	***4 Ω***	***160 µH***	***40 µF***	***28V***
500 µs	***5 A***	***4 Ω***	***400 µH***	***100 µF***	***28V***
1 ms	***5 A***	***4 Ω***	***800 µH***	***200 µF***	***28V***
50 µs	***10 A***	***4 Ω***	***40 µH***	***10 µF***	***56V***
100 µs	***10 A***	***4 Ω***	***80 µH***	***20 µF***	***56V***
200 µs	***10 A***	***4 Ω***	***160 µH***	***40 µF***	***56V***
500 µs	***10 A***	***4 Ω***	***400 µH***	***100 µF***	***56V***
1 ms	***10 A***	***4 Ω***	***800 µH***	***200 µF***	***56V***

Fig. 40 shows the circuit diagram for the generation of a 1ms pulse @ 10A peak current. Simulation for the other values of pulse width and peak current (provided in Table 12) follow the same procedure as in the given circuit diagram. An ideal switch is used in the place of DUT (in this case, MOSFET). This was done to avoid the ringing in the output current waveform due to the reverse recovery of the MOSFET body diode.

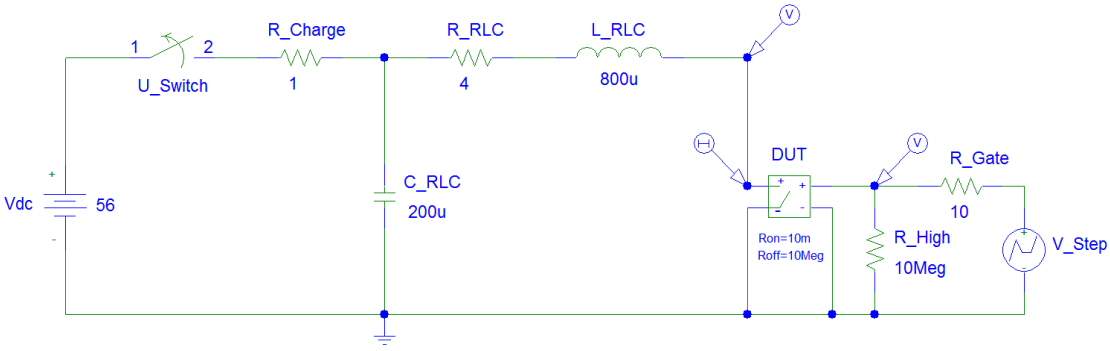

Figure 40. PSPICE RLC Ring Down circuit

The circuit was simulated to obtain the waveforms in Fig. 41. Due to the critically damped nature of the current pulse, there is no ringing in the current waveform. In the output waveform, it can be noticed that there is negligible overlap between the Drain to Source voltage of the DUT and the Drain current due to which the switching losses are negligible and the conduction losses are dominant. The maximum power dissipation was little over 1W. This is due to the nature of the RLC circuit where the

current starts rising after the drain voltage becomes close to zero. The above circuit was designed for 10A current pulse with 1 ms pulse width measured at 50% of the total magnitude.

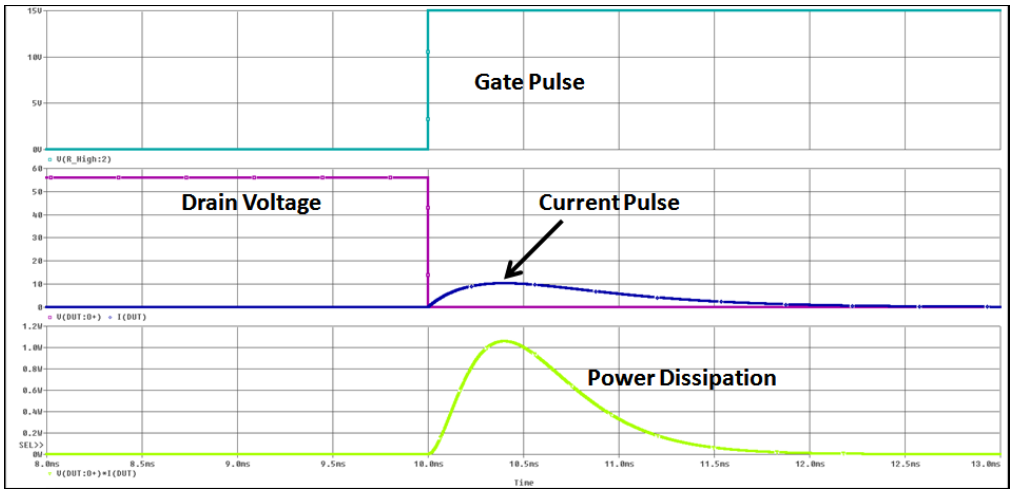

Figure 41. RLC Ring Down Circuit Waveforms

14.2 SILVACO ATLAS TRANSIENT ANALYSIS PROGRAM

The transient analysis was performed using both DC and Transient blocks in the program code. The circuit parameters were entered into the program in PSPICE netlist format where each component is associated with nodes depending on the number of terminals on the component. The program execution starts with DC steady state where the simulator tries to obtain node voltages. Capacitors are considered as open circuit and Inductors are considered as short circuits. For the circuit in Fig. 40, the simulator ramps up the voltage across the drain of the MOSFET and stores the various electrical parameters in a binary file.

In the transient phase of simulation, the binary file generated during the DC steady state simulation is used as an input. The transient simulation was performed for current pulses 50 µs, 100 µs, 200 µs, 500 µs and 1ms wide. Due to the volume of data, this thesis will be discussing the extreme pulse width cases and a summary of all the scenarios.

14.3 MOSFET TURN ON

MOSFET is a voltage controlled device where the drain current is controlled by the gate voltage. Since an oxide layer isolates the gate with rest of the semiconductor, in DC steady state, the gate current is negligible. However, during switching applications, the current required to charge/discharge the gate capacitor can be high depending upon the switching frequency and the magnitude of the gate capacitance. A simple analysis can be done using the basic capacitor equation

$$I = C\left(\frac{dV}{dt}\right) \tag{40}$$

Equation 40. Capacitor Current Equation

If the voltage across the capacitor has to raised (above the threshold voltage) in a short interval of time, the current requirement will be very high which requires the use of a gate driver circuit. Since this research is based on the transient performance of the MOSFET, it is very important to analyze the turn on characteristics.

14.3.1 THEORY

Fig. 42 shows the typical waveforms during the turn on of a MOSFET.

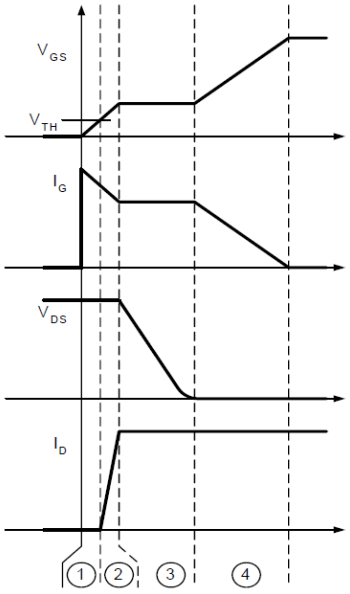

Figure 42. MOSFET Turn ON [39]

The capacitance of a MOSFET can be classified into Gate to Source Capacitance (C_{GS}), Gate to Drain Capacitance or Miller Capacitance (C_{GD}) and Drain to Source Capacitance (C_{DS}) of the body diode. C_{GD} and C_{DS} are a function Drain to Gate voltage and Drain to Source Voltage respectively. Since C_{GD} and C_{DS} are dependent on the width of space charge region, higher the voltage, lower the capacitance [39].

In the time interval 1, the gate to source capacitor is charged from 0V to threshold voltage, V_{TH}. During this interval, most of the gate current is charging C_{GS} while a small current flows through C_{GD}. As the voltage increases at the gate terminal, the C_{GD} capacitor's voltage gets slightly reduced [39].

In the time interval 2, the gate voltage is rising from V_{TH} to the Miller plateau level, $V_{GS,Miller}$. This is the linear operation of the device when current is proportional to the gate voltage. The current is flowing into the C_{GS} and C_{GD} capacitors and the V_{GS} voltage is increasing. The drain current increases while the drain-to-source voltage stays at the previous level ($V_{DS,OFF}$). This can be understood by considering the integral body diode in the MOSFET. Until all the current is transferred into the MOSFET and the diode is turned-off completely to be able to block reverse voltage across its PN junction, the drain voltage must stay at the output voltage level [39].

In the time interval 3 of the turn-on process, the gate voltage remains at a constant level ($V_{GS,Miller}$) and the device is on to carry the entire load current and the body diode is turned off. This causes the drain voltage to fall across the device while the gate to source voltage stays steady. This is the Miller plateau region in the gate voltage waveform. The Miller Gate Plateau voltage is given by the equation

$$V_{GP} = V_{TH} + \sqrt{\frac{J_{ON} W_{CELL} L_{CH}}{2 \mu_{ni} C_{OX}}} \tag{41}$$

Equation 41. Gate Plateau Voltage

where J_{ON} is the on-state current density, W_{cell} is the cell width, L_{CH} is the channel length, μ_{ni} is the inversion layer mobility and C_{ox} is the gate oxide capacitance [40]. The entire gate current is diverted to discharge the C_{GD} capacitor (or charge the

capacitor in the opposite direction) to facilitate the rapid voltage change across the drain-to-source terminals. The drain current of the device stays constant since it is now limited by the external circuitry [39].

The last step of the turn-on is to fully enhance the conducting channel of the MOSFET by applying a higher gate drive voltage. The final amplitude of V_{GS} determines the ultimate on-resistance of the device during its on-time. Therefore, in this fourth interval, V_{GS} is increased from $V_{GS,Miller}$ to its final value. This is accomplished by charging the C_{GS} and C_{GD} capacitors, thus gate current is now split between the two components. While these capacitors are being charged, the drain current is still constant, and the drain-to source voltage is slightly decreasing as the on resistance of the device is being reduced [39].

14.3.2 SIMULATION RESULTS

The RLC ring down circuit was simulated in ATLAS for current densities of 500A cm^{-2} and 1000A cm^{-2} for ambient temperature condition of 300K and 423K. This thesis will consider the case when the current density is 500A cm^{-2} and temperature is 300K. In an RLC ring down circuit, the current waveform rises after the voltage across the switch goes down due to the nature of the circuit. Hence, the MOSFET turn on results vary from Fig. 42 which considers a simple square wave switching circuit.

During time interval t_1 to t_2, the Gate to Source voltage (Fig. 43) starts rising from 0V to V_{TH} (in this case, 6V). The Drain to Source voltage (Fig. 44) almost remains at the blocking voltage of 56V. There is a slight change in the Drain to Gate voltage (Fig. 45) which shows that there is a current flow through the Miller Capacitor C_{GD}. The Drain Current Density (Fig. 46) is almost zero since the MOSFET is not turned on yet and the net Gate current waveform (Fig. 47) shows the charging up C_{GS}. The Gate current first reaches a peak value of 270 mA and then starts reducing. The charge accumulated during this interval is Q_{GS} and is mainly used to energize C_{GS}.

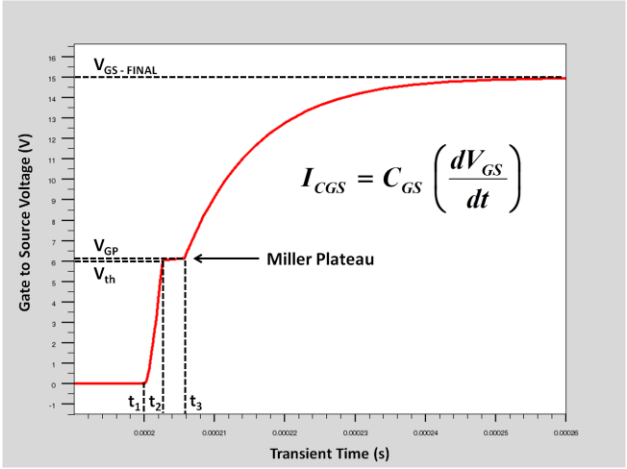

Figure 43. Gate to Source Voltage (Turn ON)

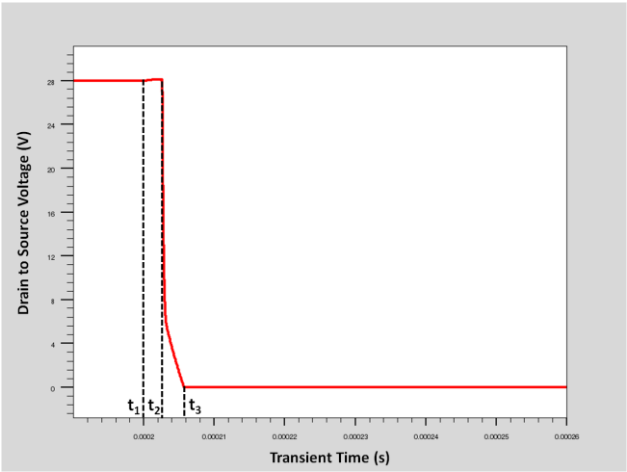

Figure 44. Drain to Source Voltage (Turn ON)

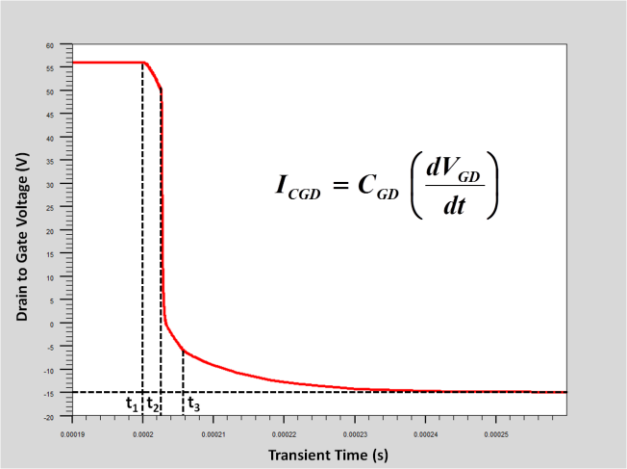

Figure 45. Drain to Gate Voltage (Turn ON)

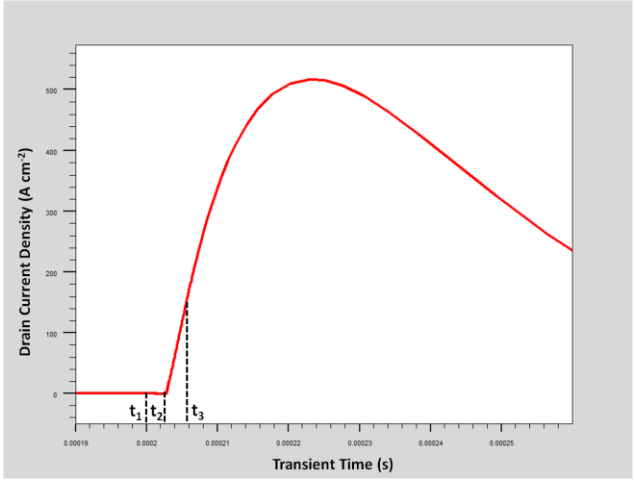

Figure 46. Drain Current Density (Turn ON)

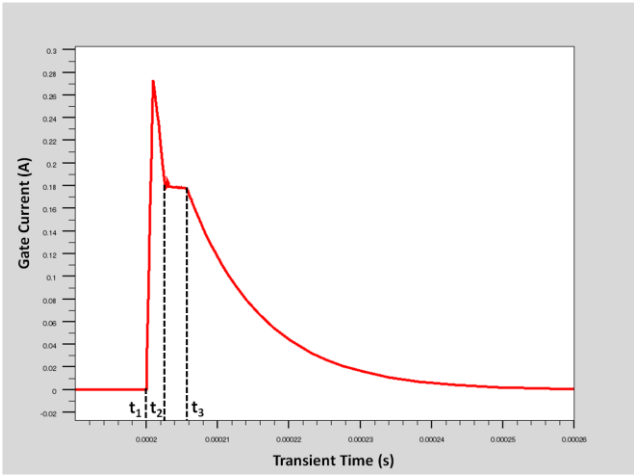

Figure 47. Gate Current (Turn ON)

During time interval t_2 to t_3, the Gate to Source voltage (Fig. 43) remains at a constant voltage level known as Gate Plateau Voltage. In the Miller Plateau region, the Gate to Source voltage waveform has zero slope. The presence of a slope indicates change in voltage and hence, current flow into C_{GS}. Since V_{GP} is a function of the on-state current density (Eq. 41), in this simulation, the magnitude of V_{GP} and V_{TH} are almost the same since the current density is very low due to the nature of the circuit. The Drain to Source voltage (Fig. 44) starts decreasing in a non linear manner until it reaches on-state voltage drop. C_{GD} is discharged by the gate current which causes a reduction in the Drain to Gate voltage (Fig. 45) which shows that there is a considerable current flow through the C_{GD} (via Eq. 40). Since Gate to Source voltage

is constant, there is no current flow into C_{GS}. The Drain Current Density (Fig. 46) starts rising depending on the nature of the circuit as the threshold voltage is attained. The net Gate current waveform (Fig. 47) shows constant current charging of C_{GD}. The charge accumulated during this interval is Q_{GD} and is used to energize C_{GD}.

After time t_3, the Gate to Source voltage (Fig. 43) again starts rising from Miller plateau to the final magnitude of the Gate voltage at a slower rate. This voltage is also known as overdrive voltage as it is used to fully enhance the conducting channel of the MOSFET and further reduce the on-state resistance. In this regime, the Drain to Gate voltage (Fig. 45) also decreases at a slower rate indicating current flow into C_{GS} and C_{GD}. The net Gate current (Fig. 47) starts decreasing and gate charge is again shared between C_{GS} and C_{GD}. Figures 48-51 show an enlarged version of the above discussed process. Since the Current Density waveform is more dependent on the external circuit post threshold voltage, it is not shown in the group of figures below.

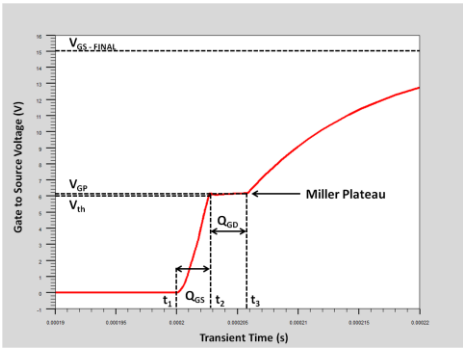

Figure 48. Gate to Source Voltage (Zoom)

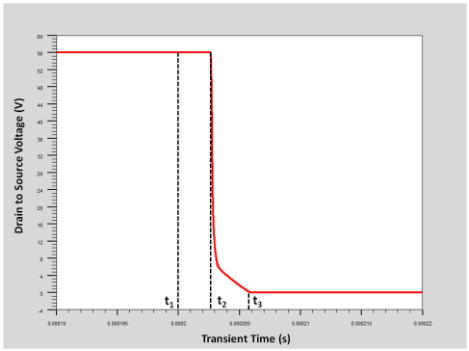

Figure 49. Drain to Source Voltage (Zoom)

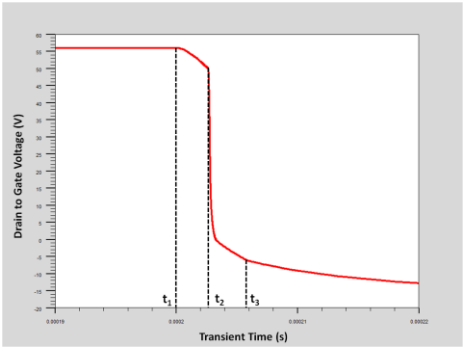

Figure 50. Drain to Gate Voltage (Zoom)

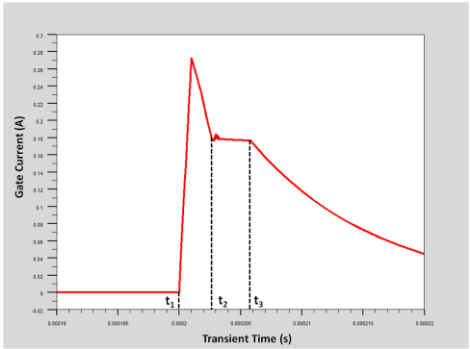

Figure 51. Gate Current (Zoom)

14.3 PEAK CURRENT = 5A PULSE WIDTH = 50 µs $T_{AMBIENT}$ = 300K

In this simulation, a single shot current pulse with peak current of 5A is passed through the device. A current amplitude of 5A corresponds to a current density of 500A cm^{-2}. Fig. 52 shows the current pulse waveforms for a pulse width of 50 µs.

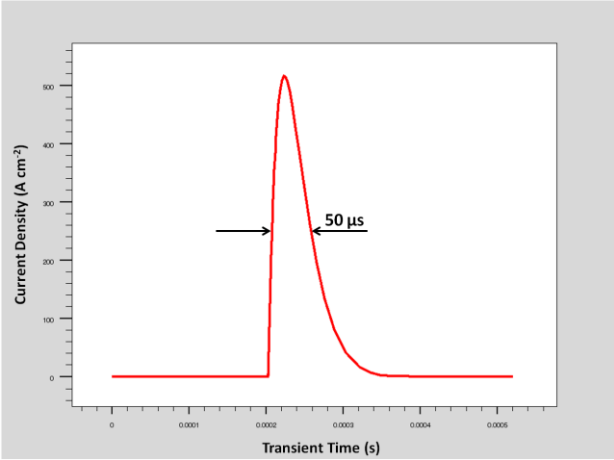

Figure 52. 500A cm^{-2} 50 µs Current Pulse

The current pulse had a di/dt of 0.4 A/µs measured between 10% and 90% of the total current density magnitude (in case of 500A cm^{-2}, it was measured from 50A cm^{-2} to 450A cm^{-2}). Fig. 53 shows the maximum current density in the MOSFET structure. This was achieved using the PROBE feature of Tonyplot [41]. After selecting this feature, the pointer was placed in the channel region of MOSFET where the current density was maximum. A measured value of 504.45A cm^{-2} was obtained in the channel region. This magnitude was also verified in the contour plot display scale. This contour plot was obtained by saving the transient simulation results in a structure file at regular transient time intervals. This was done because the final plot will not contain the required data as the current pulse waveform dies out.

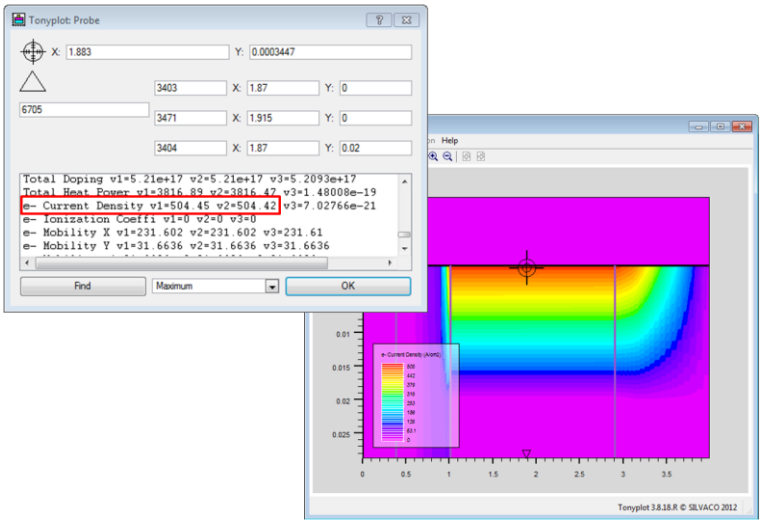

Figure 53. Maximum Current Density of 500A cm^{-2} in the MOSFET Channel

The Power dissipation for any switching device depends on the overlap between the voltage and current waveforms. In this research, the focus is on the overlap between the Drain to Source voltage and Drain current. Fig. 54 shows the overlap between the voltage and current for the MOSFET at 50 µs pulse width .

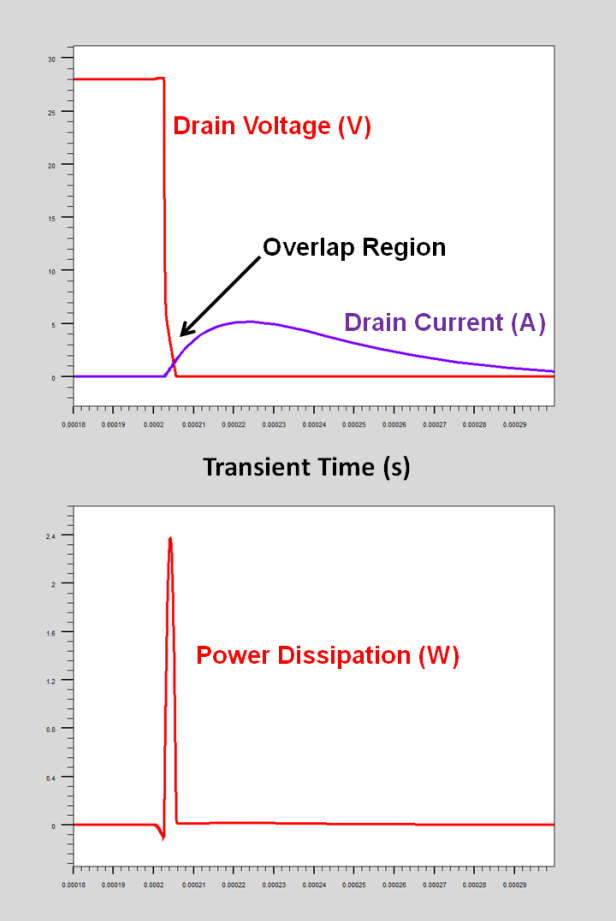

Figure 54. Power Dissipation due to Voltage - Current Overlap

Fig. 55 displays the Switching Power Dissipated during the turn on of the device. The Peak power dissipated is 2.37W and the power pulse duration is 2 µs. In order to calculate the energy dissipated during this interval, the integration option available in Tonyplot is used [41].

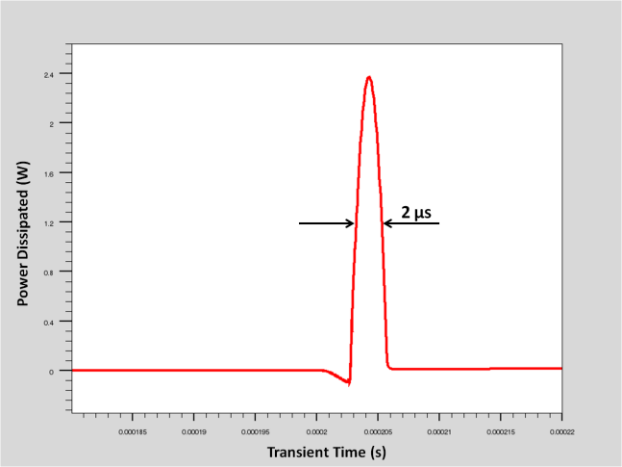

Figure 55. Switching Power Loss for 5A 50 µs Current Pulse @ 300K

Upon integrating the power waveform, an energy dissipation of 4.7 µJ is obtained. the integration process is shown in Fig. 56.

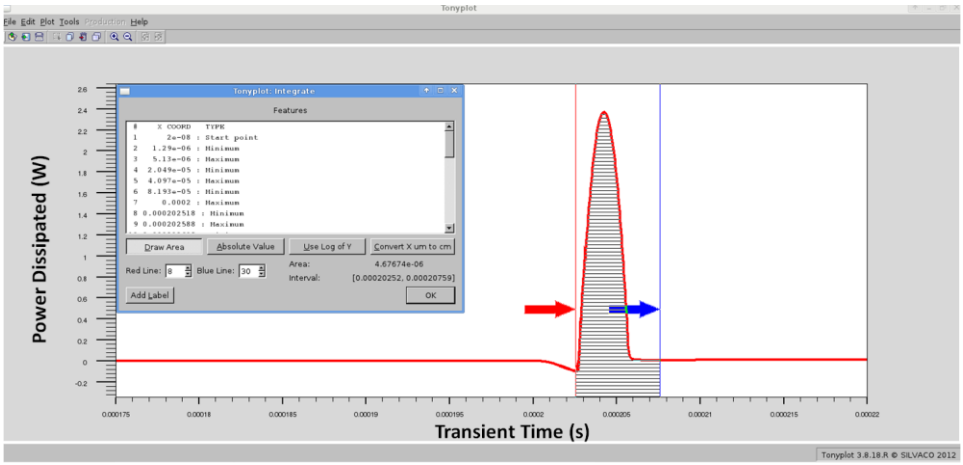

Figure 56. Integrating Power waveform to obtain Energy

Since the Lattice heating models were enabled during the transient simulation, Fig. 57 shows the Lattice temperature rise due to the above energy dissipation.

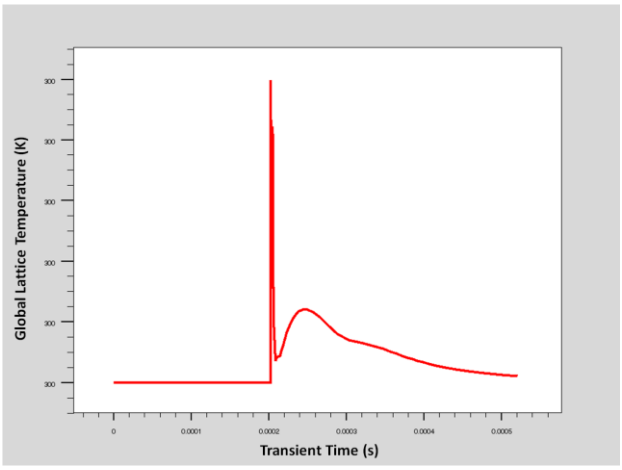

Figure 57. Lattice Temperature for 5A 50 µs Current Pulse @ 300K

Even though the plot show a temperature rise, the temperature scale remain the same which means that the rise in temperature is minuscule.

14.4 PEAK CURRENT = 5A PULSE WIDTH = 1 ms $T_{AMBIENT}$ = 300K

Fig. 58 shows the current pulse waveforms for a pulse width of 1 ms and current density of 500A cm^{-2}.

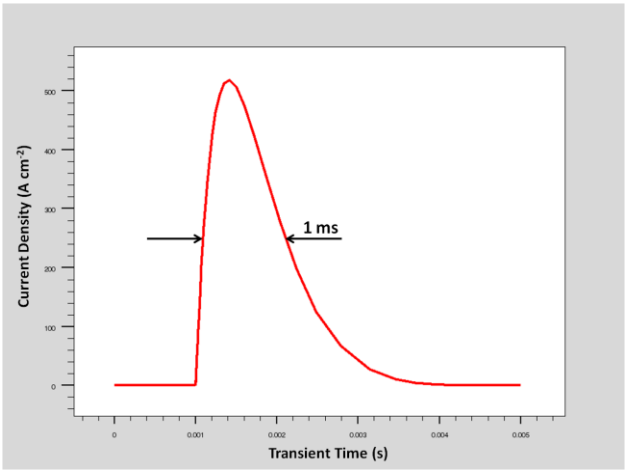

Figure 58. 500A cm^{-2} 1 ms Current Pulse

The current pulse had a di/dt of 0.02 A/µs measured between 10% and 90% of the total current density magnitude (in case of 500A cm^{-2}, it was measured from 50A cm^{-2}

to 450A cm^{-2}). Fig. 59 shows the overlap between the voltage and current for the MOSFET at 1ms pulse width.

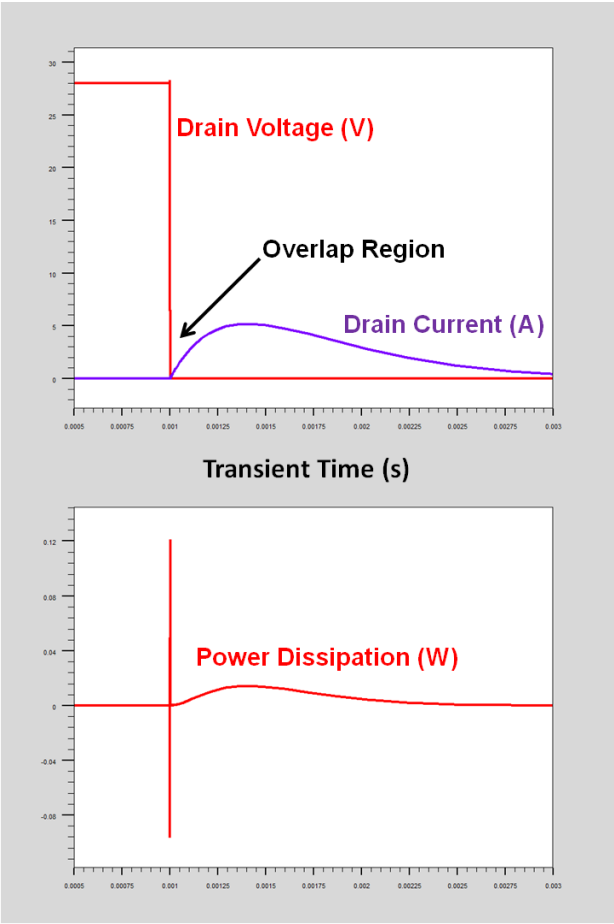

Figure 59. Power Dissipation due to Voltage - Current Overlap

Fig. 60 displays the Switching Power Dissipated during the entire pulse width. The Peak power dissipated is 0.12W. But as the pulse width increases, the conduction losses dominate more than the switching loss.

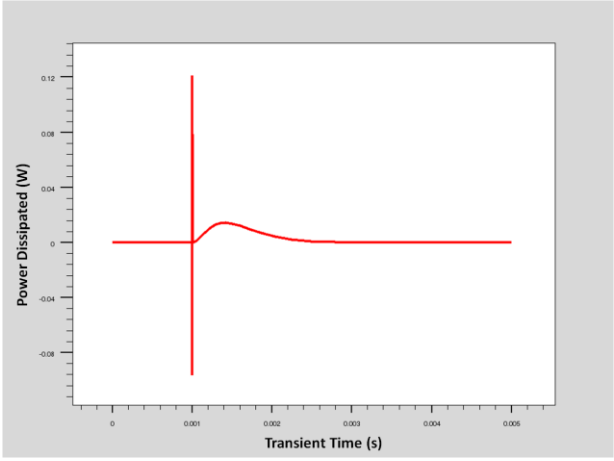

Figure 60. Total Power Dissipation for 5A 1 ms Current Pulse @ 300K

On integration, the total dissipated energy is 11 µJ out of which 0.22 µJ is dissipated during the turn on of the device and 10.78 µJ is the conduction loss. The Lattice temperature plot in Fig. 61 shows a minuscule change in temperature.

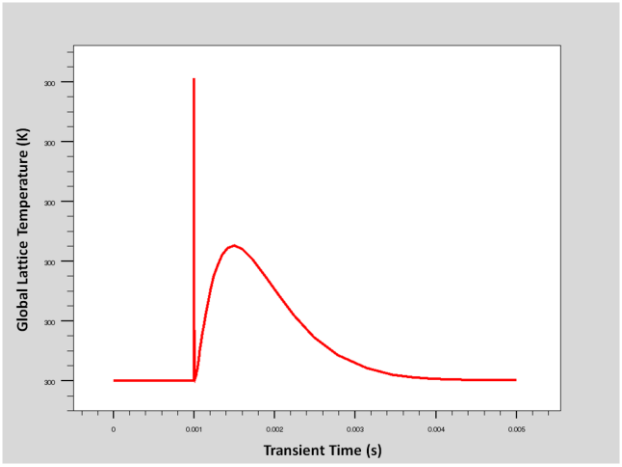

Figure 61. Lattice Temperature for 5A 1 ms Current Pulse @ 300K

14.5 PEAK CURRENT = 5A PULSE WIDTH = 50 µs $T_{AMBIENT}$ = 423K

The current density pulse is same as in section 14.3 Fig. 52. The increase in ambient temperature has caused some variation in the switching power loss but overall the power dissipation waveform (Fig. 62) looks similar to one at 300K. Fig. 63

shows the overlap between the voltage and current for the MOSFET at 50 µs pulse width.

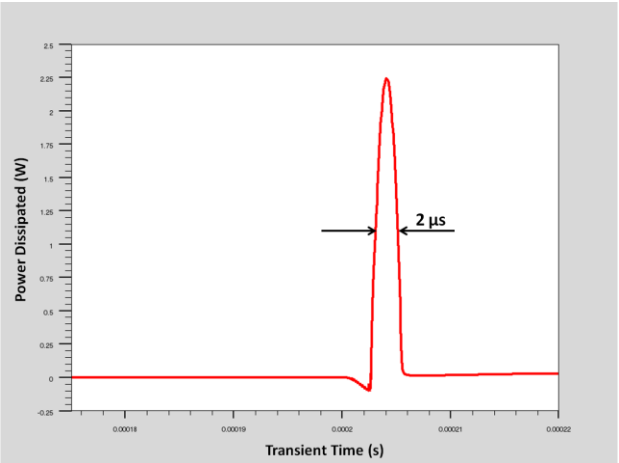

Figure 62. Switching Power Loss for 5A 50 µs Current Pulse @ 423K

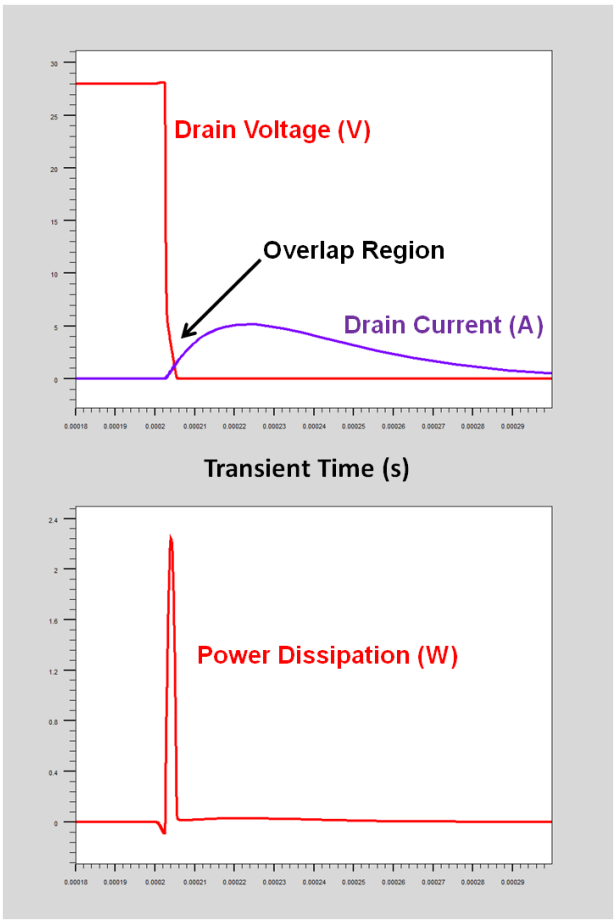

Figure 63. Power Dissipation due to Voltage - Current Overlap

The peak power dissipated is 2.24W and the energy dissipated during turn on is 5.3 µJ which is almost similar to the results obtained for 300K ambient temperature. The global Lattice temperature plot (Fig. 64) shows no significant temperature rise.

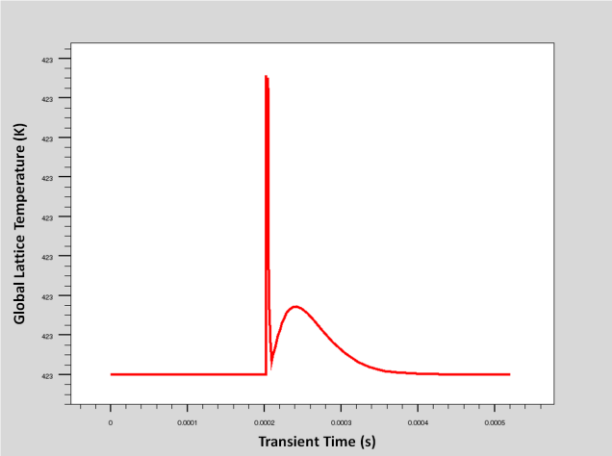

Figure 64. Lattice Temperature for 5A 50 µs Current Pulse @ 423K

14.6 PEAK CURRENT = 5A PULSE WIDTH = 1 ms $T_{AMBIENT}$ = 423K

The current density pulse is same as in section 14.4 Fig. 58. The increase in ambient temperature did not make any significant change to the Switching Power loss but the conduction losses increased as per Fig. 65 and 66.

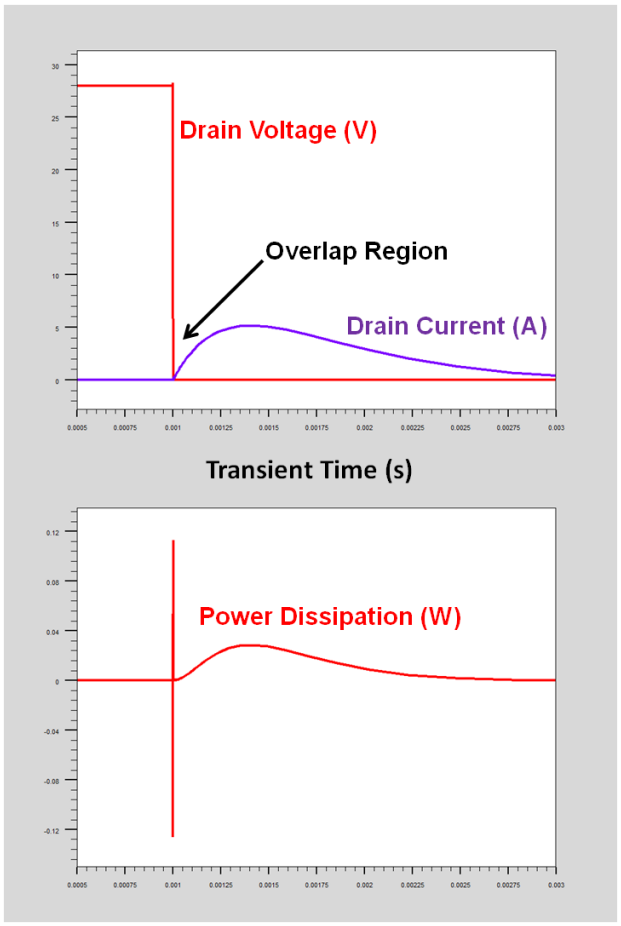

Figure 65. Power Dissipation due to Voltage - Current Overlap

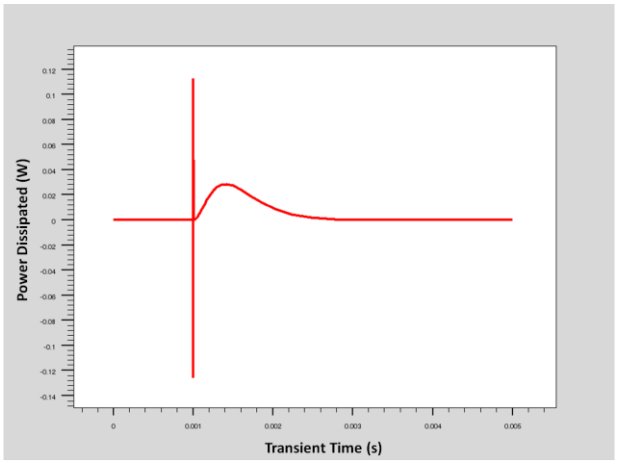

Figure 66. Total Power Dissipation for 5A 1 ms Current Pulse @ 423K

The peak power dissipated is 0.11W and the energy dissipated during turn on is 0.2 µJ. On integration, the total dissipated energy is 21.5 µJ out of which 0.2 µJ is dissipated during the turn on of the device and 21.3 µJ is the conduction loss which is almost double the loss at 300K. The Lattice temperature plot in Fig. 67 shows a insignificant change in Lattice temperature.

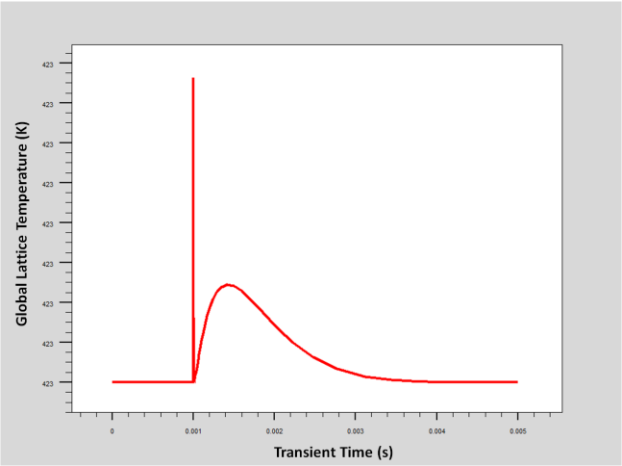

Figure 67. Lattice Temperature for 5A 1 ms Current Pulse @ 423K

14.7. PEAK CURRENT = 10A PULSE WIDTH = 50 µs $T_{AMBIENT}$ = 300K

In this simulation, a single shot current pulse with peak current of 10A is passed through the device. A current amplitude of 10A corresponds to a current density of 1000A cm^{-2}.

Fig. 68 shows the current pulse waveforms for a pulse width of 50 µs. The current pulse had a di/dt of 0.8 A/µs measured between 10% and 90% of the total current density magnitude (in case of 1000A cm^{-2}, it was measured from 100A cm^{-2} to 900A cm^{-2}).

Fig. 69 shows the maximum current density in the MOSFET structure. This was achieved using the PROBE feature of Tonyplot [41]. After selecting this feature, the pointer was placed in the channel region of MOSFET where the current density was maximum. A measured value of 1024.18A cm^{-2} was obtained in the channel region. This magnitude was also verified in the contour plot display scale.

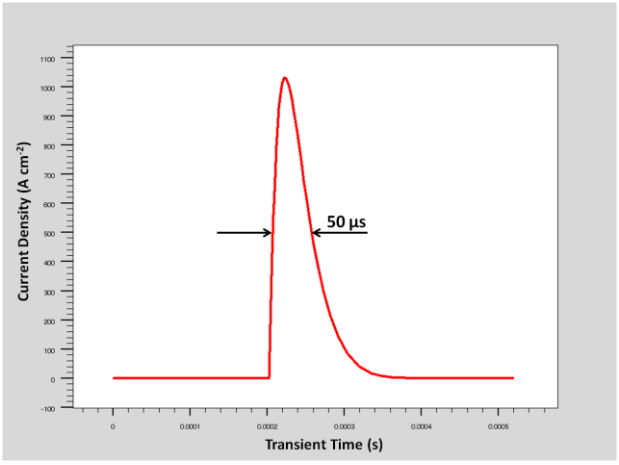

Figure 68. 1000A cm^{-2} 50 µs Current Pulse

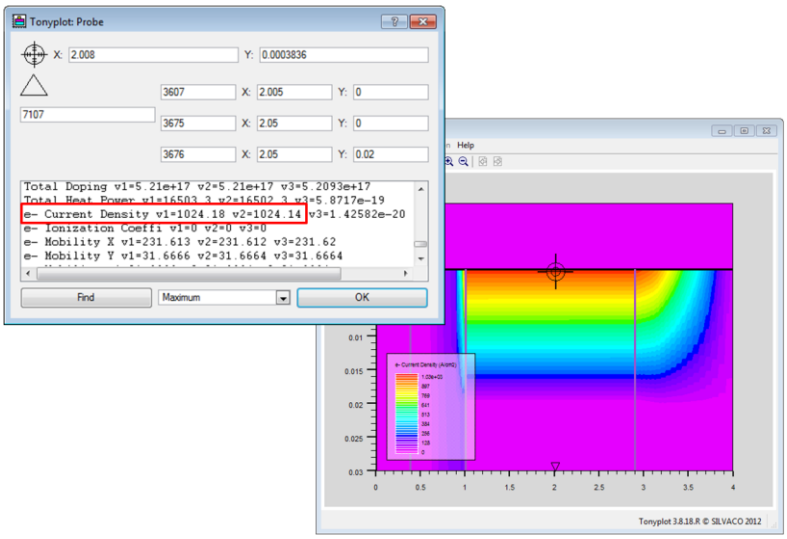

Figure 69. Maximum Current Density of 1000A cm^{-2} in the MOSFET Channel

Fig. 70 shows the overlap between the voltage and current for the MOSFET at 50 µs pulse width. Fig. 71 shows the switching power loss waveform. The switching power loss pulse has a maximum power dissipation of 5.7W and a pulse width of 2 µs.

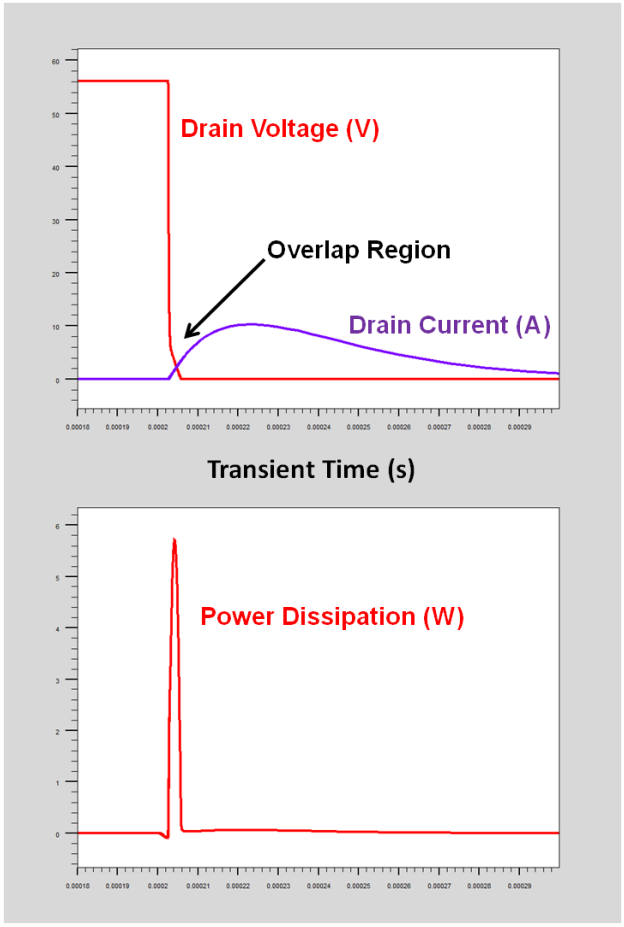

Figure 70. Power Dissipation due to Voltage - Current Overlap

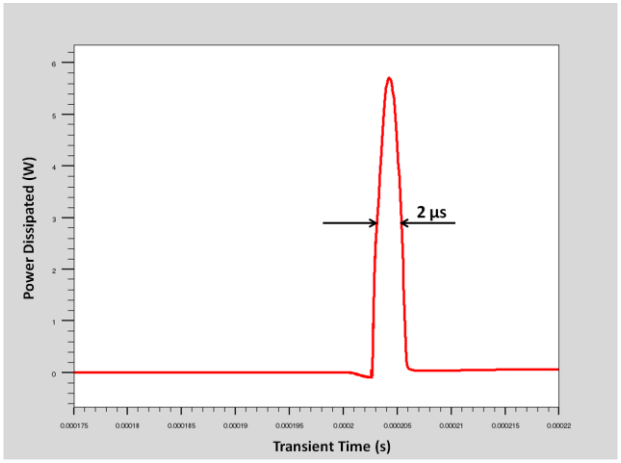

Figure 71. Switching Power Loss for 10A 50 µs Current Pulse @ 300K

On integrating the power loss waveform (Fig. 72), the total energy loss is 14 µJ out of which 12 µJ is contributed by the switching loss and 2 µJ is the conduction loss.

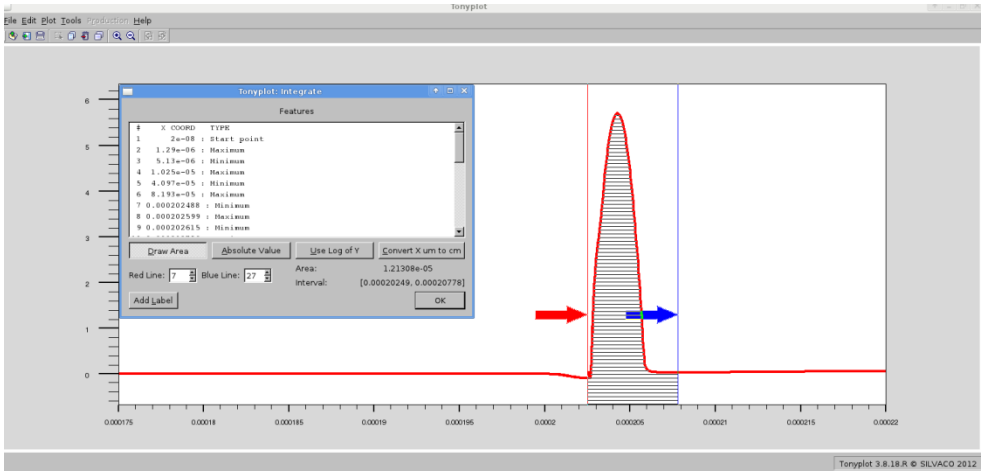

Figure 72. Integrating Power waveform to obtain Energy

The Lattice temperature plot in Fig. 73 shows a insignificant change in Lattice temperature.

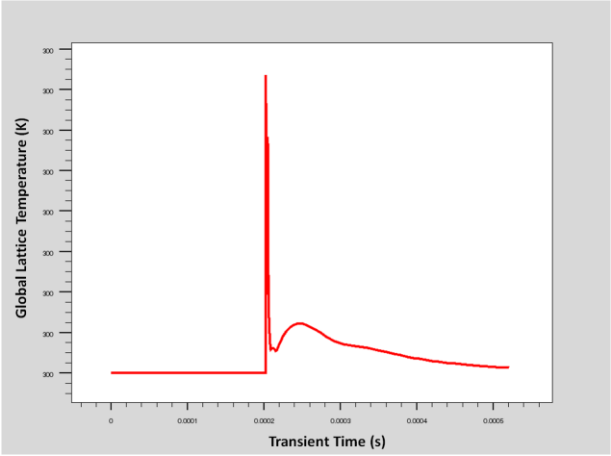

Figure 73. Lattice Temperature for 10A 50 µs Current Pulse @ 300K

14.8 PEAK CURRENT = 10A PULSE WIDTH = 1 ms $T_{AMBIENT}$ = 300K

Fig. 74 shows the current pulse waveform for a pulse width of 1 ms and current density of 1000A cm^{-2}. The current pulse had a rate of current change of 0.04 A/µs measured between 10% and 90% of the total current density magnitude (in case of 1000A cm^{-2}, it was measured from 100A cm^{-2} to 900A cm^{-2}).

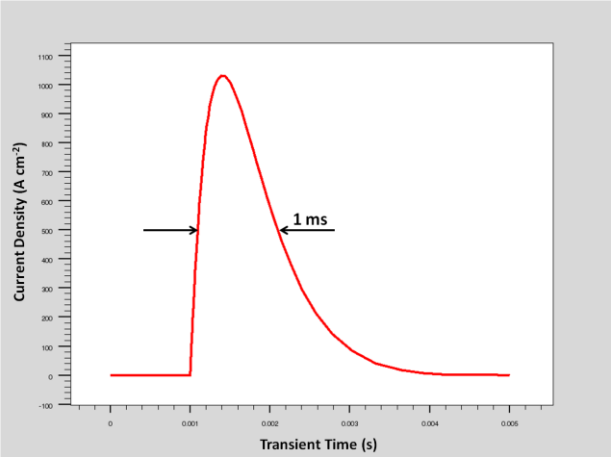

Figure 74. 1000A cm^{-2} 1 ms Current Pulse

Fig. 75 shows the overlap between the voltage and current for the MOSFET at 50 µs pulse width

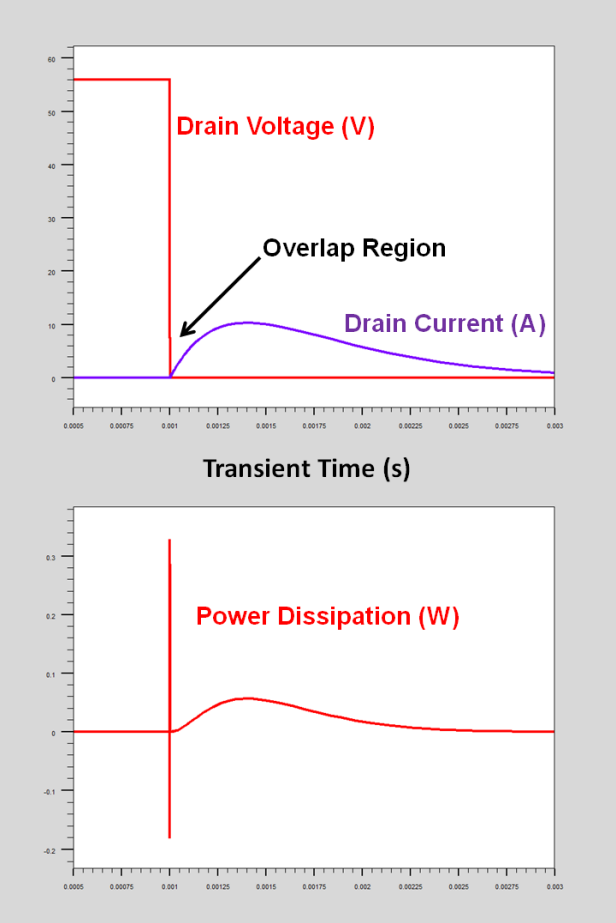

Figure 75. Power Dissipation due to Voltage - Current Overlap

Fig. 76 displays the Switching Power Dissipated during the entire pulse width. The Peak power dissipated is 0.27W. But as the pulse width increases, the conduction losses dominate more than the switching loss.

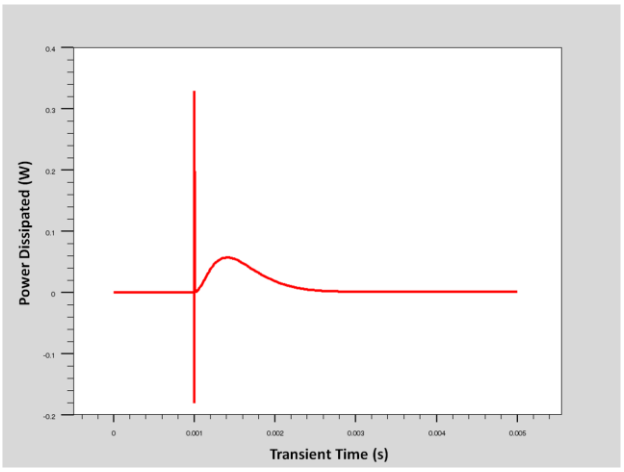

Figure 76. Total Power Dissipation for 10A 1 ms Current Pulse @ 300K

On integration, the total dissipated energy is 43 µJ out of which 0.6 µJ is dissipated during the turn on of the device and 42.4 µJ is the conduction loss. The Lattice temperature plot in Fig. 77 does not show a significant rise in temperature.

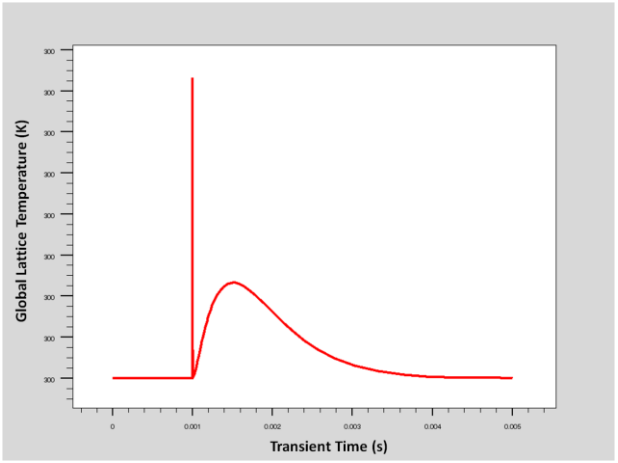

Figure 77. Lattice Temperature for 10A 1 ms Current Pulse @ 300K

14.9. PEAK CURRENT = 10A PULSE WIDTH = 50 µs $T_{AMBIENT}$ = 423K

The current density pulse is same as in section 14.7 Fig. 68. The Power loss waveform indicated in Fig. 78 and 79 shows that the Power loss is almost the same as for 300K ambient temperature.

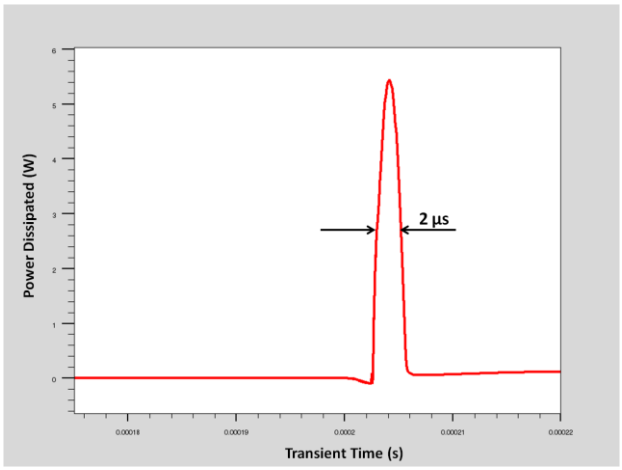

Figure 78. Switching Power Loss for 10A 50 µs Current Pulse @ 423K

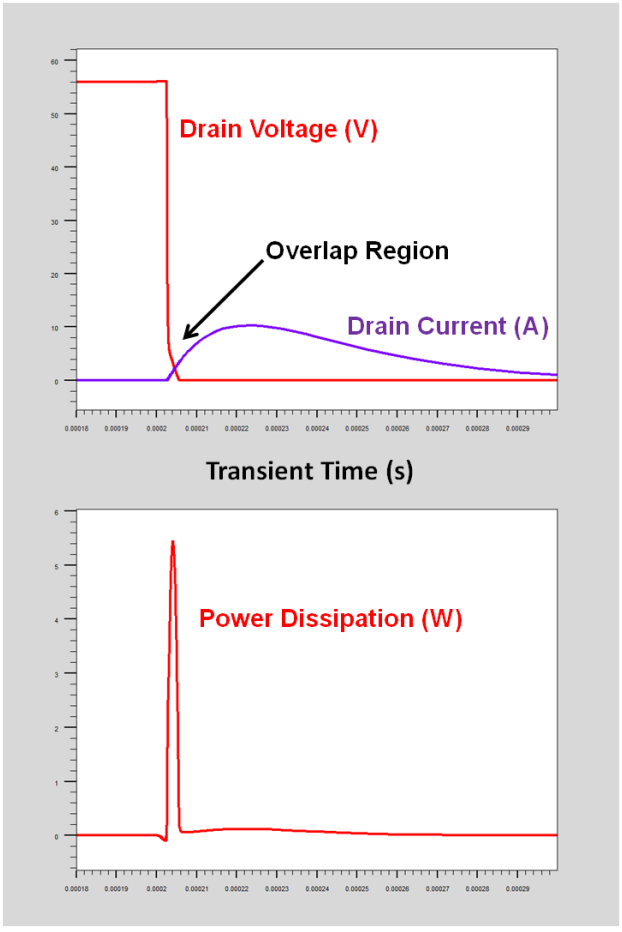

Figure 79. Power Dissipation due to Voltage - Current Overlap

The peak power dissipated is 5.43W and the energy dissipated during turn on is 11 µJ which is almost similar to the results obtained for 300K ambient temperature. The global Lattice temperature (Fig. 80) shows no significant temperature rise.

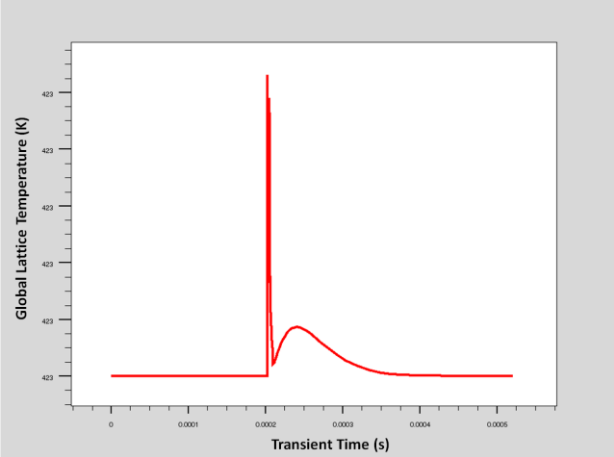

Figure 80. Lattice Temperature for 10A 50 µs Current Pulse @ 423K

14.10 PEAK CURRENT = 10A PULSE WIDTH = 1 ms $T_{AMBIENT}$ = 423K

The current density pulse is same as in section 14.8 Fig. 74. The increase in ambient temperature did not make any significant change to the Switching Power loss but the conduction losses increased as per Fig. 81 and 82.

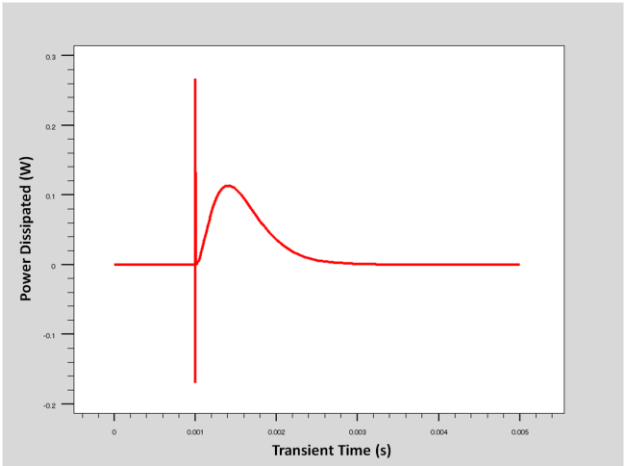

Figure 81. Total Power Dissipation for 10A 1 ms Current Pulse @ 423K

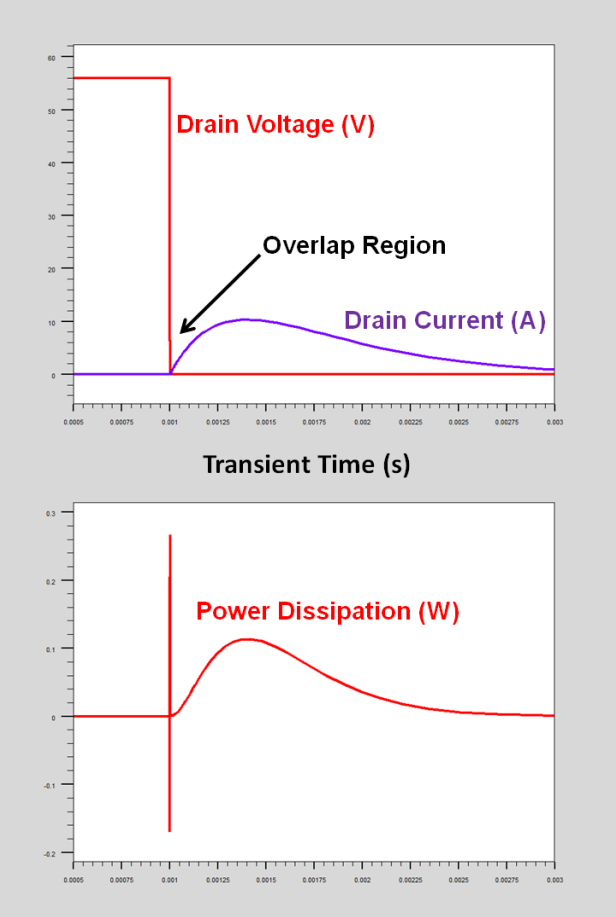

Figure 82. Power Dissipation due to Voltage - Current Overlap

On integration, the total dissipated energy is 84.7 µJ out of which 0.5 µJ is dissipated during the turn on of the device and 84.2 µJ is the conduction loss which is almost double the losses at 300K. The Lattice temperature plot in Fig. 83 does not show a significant rise in temperature.

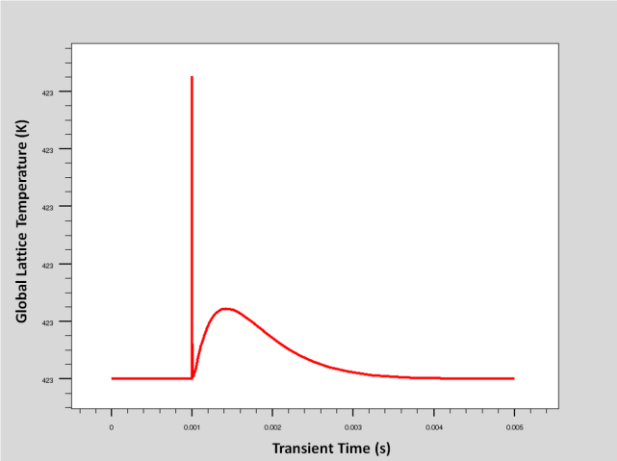

Figure 83. Lattice Temperature for 10A 1 ms Current Pulse @ 423K

14.11 TRANSIENT ANAYLYSIS SUMMARY

Table 14 shows the summary of various parameters on the basis of the transient simulation using current pulses of varying pulse width for Peak Current of 5A at 300K ambient temperature.

Table 14. Transient Analysis Summary for 5A at 300K

	PEAK CURRENT = 5A AMBIENT TEMPERATURE = 300K				
Pulse Width (µs)	***50***	***100***	***200***	***500***	***1000***
di/dt (A/µs)	***0.4***	***0.2***	***0.1***	***0.04***	***0.02***
Peak Power Dissipated (W)	***2.37***	***1.2***	***0.61***	***0.24***	***0.12***
Power Pulse Width (µs)	***2***	***2***	***2***	***2***	***2***
Switching Energy Loss (µJ)	***4.7***	***2.3***	***1.2***	***0.45***	***0.22***
Conduction Energy Loss (µJ)	***0.5***	***1.1***	***2.1***	***5.35***	***10.78***
Total Energy Loss (µJ)	***5.2***	***3.4***	***3.3***	***5.8***	***11***

Table 15 shows the summary of various parameters on the basis of the transient simulation using current pulses of varying pulse width for Peak Current of 5A at 423K ambient temperature.

Table 15. Transient Analysis Summary for 5A at 423K

	PEAK CURRENT = 5A AMBIENT TEMPERATURE = 423K				
Pulse Width (µs)	***50***	***100***	***200***	***500***	***1000***
di/dt (A/µs)	***0.4***	***0.2***	***0.1***	***0.04***	***0.02***
Peak Power Dissipated (W)	***2.24***	***1.13***	***0.57***	***0.23***	***0.11***
Power Pulse Width (µs)	***2***	***2***	***2***	***2***	***2***
Switching Energy Loss (µJ)	***4.3***	***2.1***	***1***	***0.4***	***0.2***
Conduction Energy Loss (µJ)	***1***	***2.1***	***4.3***	***10.6***	***21.3***
Total Energy Loss (µJ)	***5.3***	***4.2***	***5.3***	***11***	***21.5***

Fig. 84 shows the plot of Energy Dissipation as a function of the current pulse width for 500A cm^{-2} current density.

T=300K

T=423K

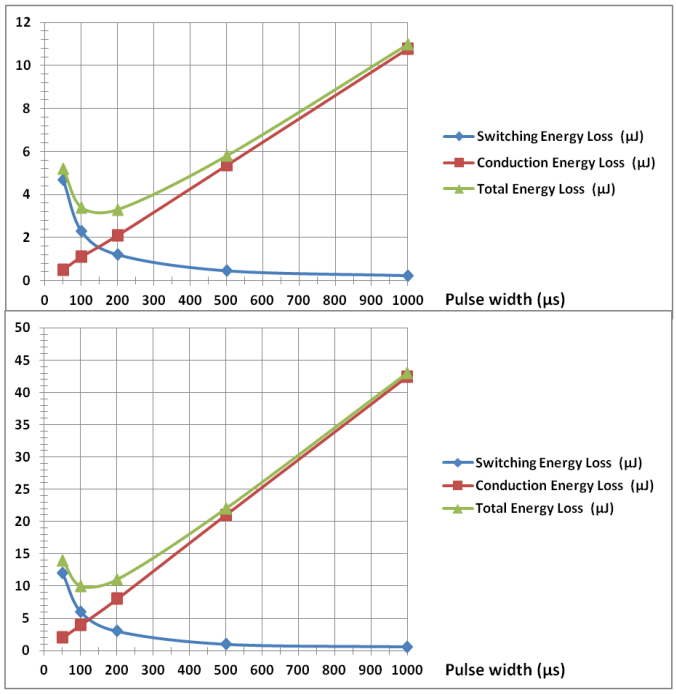

Figure 84. Energy Dissipation Summary for 500A cm^{-2}

Table 16 shows the summary of various parameters on the basis of the transient simulation using current pulses of varying pulse width for Peak Current of 10A at 300K ambient temperature.

Table 16. Transient Analysis Summary for 10A at 300K

	PEAK CURRENT = 10A AMBIENT TEMPERATURE = 300K				
Pulse Width (µs)	***50***	***100***	***200***	***500***	***1000***
di/dt (A/µs)	***0.8***	***0.4***	***0.2***	***0.08***	***0.04***
Peak Power Dissipated (W)	***5.7***	***2.9***	***1.45***	***0.58***	***0.27***
Power Pulse Width (µs)	***2***	***2***	***2***	***2***	***2***
Switching Energy Loss (µJ)	***12***	***6***	***3***	***1***	***0.6***
Conduction Energy Loss (µJ)	***2***	***4***	***8***	***21***	***42.4***
Total Energy Loss (µJ)	***14***	***10***	***11***	***22***	***43***

Table 17 shows the summary of various parameters on the basis of the transient simulation using current pulses of varying pulse width for Peak Current of 10A at 423K ambient temperature.

Table 17. Transient Analysis Summary for 10A at 423K

	PEAK CURRENT = 10A AMBIENT TEMPERATURE = 423K				
Pulse Width (µs)	***50***	***100***	***200***	***500***	***1000***
di/dt (A/µs)	***0.8***	***0.4***	***0.2***	***0.08***	***0.04***
Peak Power Dissipated (W)	***5.43***	***2.72***	***1.36***	***0.54***	***0.27***
Power Pulse Width (µs)	***2***	***2***	***2***	***2***	***2***
Switching Energy Loss (µJ)	***11***	***5.5***	***2.7***	***1***	***0.5***
Conduction Energy Loss (µJ)	***4.6***	***8.5***	***16.8***	***42***	***84.2***
Total Energy Loss (µJ)	***15.6***	***14***	***19.5***	***43***	***84.7***

Fig. 85 shows the plot of Energy Dissipation as a function of the current pulse width for 1000A cm^{-2} current density.

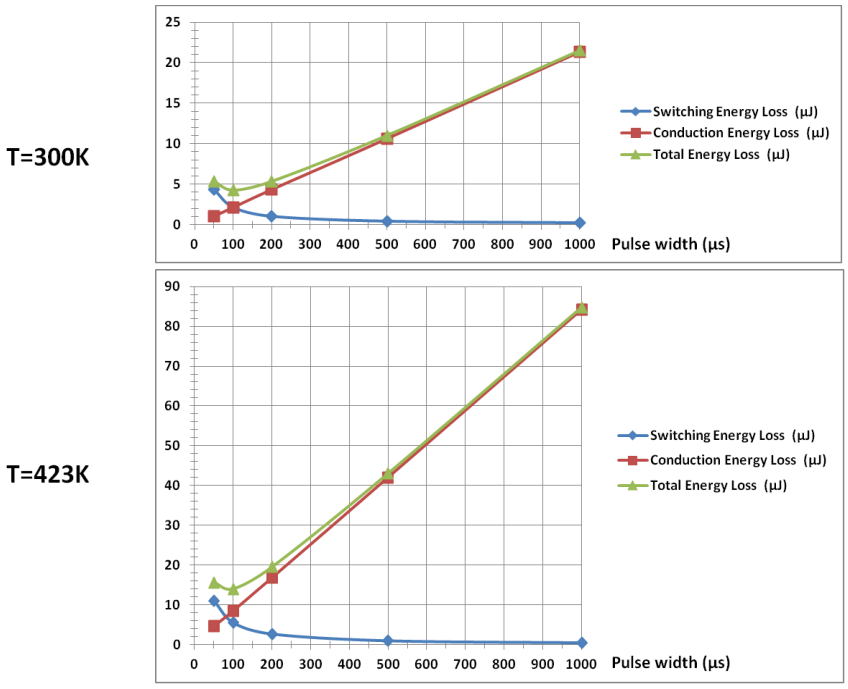

Figure 85. Energy Dissipation Summary for 1000A cm^{-2}

CHAPTER 15

TRANSIENT THERMAL SIMULATION USING RC LUMPED MODEL

As per the results of the transient simulation, it can be inferred that with the selected pulse widths and current densities, the Lattice temperature rise is negligible. This is because of the very small magnitude of energy dissipation (of the order of μJ). However, this must be verified to check if the simulation results were correct. In order to simplify things, this thesis will use RC Lumped model for the transient thermal analysis of D-MOSFET.

Transient thermal simulation requires the design of thermal model representing the device under test. In the RC Lumped model, the device is modeled in terms of thermal resistor and thermal capacitor. In order to understand this concept, the relationship between thermal and electrical equivalent must be known. Table 18 gives the electrical and thermal equivalence [42].

Table 18. Electrical Thermal Equivalence

THERMAL		*ELECTRICAL*	
Temperature	***T in K***	*Voltage*	***U in V***
Heat Flow	***P in W***	*Current*	***I in A***
Thermal Resistance	***Rth in K W-1***	*Resistance*	***R in V A-1***
Thermal Capacitance	***Cth in J K-1***	*Capacitance*	***C in A s V-1***

Fig. 86 gives a general description of a RC Lumped model. In this schematic, the T_{case} can be represented by a voltage source whose magnitude is the ambient temperature. The Heat dissipation is modeled using an equivalent current source. The RC ladder can have multiple stages based on the number of interfaces through which heat energy has to pass. In this research, it is assumed that the junction is directly exposed to the ambient condition without any heat sink or other interfaces. This was done to simplify the simulation process.

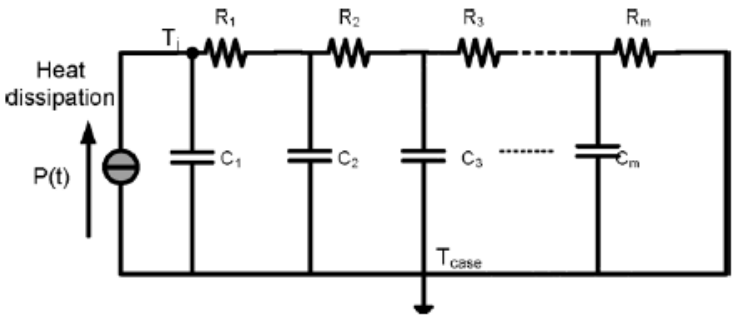

Figure 86. Schematic for Equivalent Thermal RC Ladder [43]

Since the junction is directly exposed to ambient condition, the RC network will have only one stage. In order to simulate the transient thermal model of the device, the thermal resistance and thermal capacitance values must be calculated. The equations for thermal resistance and thermal capacitance is given by

$$R_{TH} = \frac{1}{\alpha \cdot Area} \tag{43}$$

Equation 42. Thermal Resistance

$$C_{TH} = \rho \cdot V_S \cdot C_P \tag{44}$$

Equation 43. Thermal Capacitance

where α is the Heat Transfer Coefficient, Area is the surface area through which heat is dissipated from the semiconductor, ρ is the density of the semiconductor, V_s is the volume of the semiconductor and C_p is the specific heat of the semiconductor material [42].

Using the physical, thermal and simulation parameters for 4H-SiC, for an ambient temperature of 300K, the calculated value of thermal resistance was 2.17 x 10^{-3} K W^{-1} and the thermal capacitance value was 0.013 J K^{-1}. This gave an RC time constant of 28.2 microseconds. For an ambient temperature of 423K, the calculated value of thermal resistance was 87μ K W^{-1} and the thermal capacitance value was 0.013 J K^{-1}. This gave an RC time constant of 1.11 microseconds The value of the RC time constant gives a firsthand information about response of the system.

The Transient Thermal Simulations were performed using B2 SPICE A/D LITE simulation tool. In order to simulate the thermal circuit, it is required to replicate the exact Power Dissipation waveform (obtained from Silvaco) into a piecewise current source in B2 spice (since power dissipation in thermal domain is equivalent to current in electrical domain). This was accomplished using the export feature in Tonyplot. This feature extracts all the data points from the waveforms and exports it into a Comma Separated Value (CSV) file which can be easily manipulated using Microsoft© Excel. B2 spice accepts piecewise data in the form of a text file. The data from the csv file was transferred into a text file used for the simulation. The following sections will discuss the simulation results.

15.1 SIMULATION OF 10A 50 µs PULSE AT 300K

The Power Dissipation data obtained from Tonyplot was used to create a piecewise current source. The following circuit (Fig. 87) was developed in B2 spice to simulate the transient thermal effects at 300K ambient temperature.

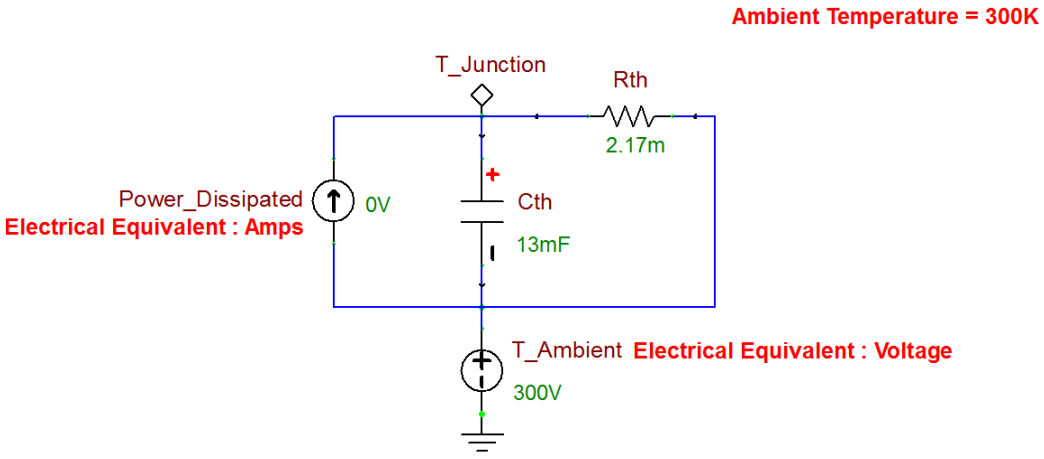

Figure 87. Thermal Circuit at Ambient Temperature = 300K

In order to simulate a different power dissipation waveform for the same ambient temperature, only the piecewise current source needs to be changed. All the other components will remain the same. In the above circuit, the voltage at the node named ***T_Junction*** gives the junction temperature change under transient conditions. Fig. 88 shows the Power Dissipation waveform replicated in B2 spice.

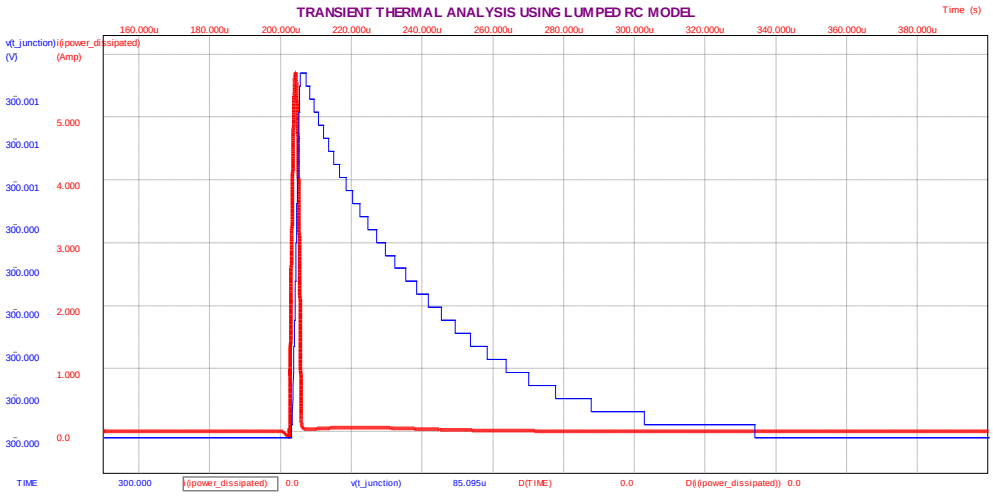

Figure 88. Power Dissipation Pulse (RED)

Fig. 89 shows the simulated temperature rise waveform. It can be observed that the temperature rise is happening only at the third decimal place and the temperature is rising from 300.000K to 300.001K. This was the reason why Tonyplot was showing Lattice temperature waveform but at the same ambient temperature.

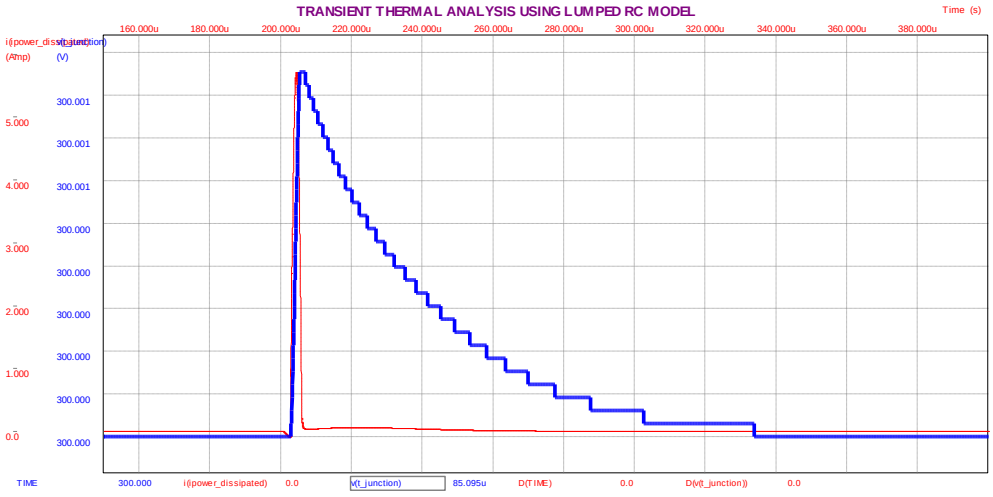

Figure 89. Junction Temperature Rise (BLUE)

15.2 SIMULATION OF 10A 1 ms PULSE AT 300K

The same circuit as in Fig. 87 was used to simulate the 1 ms pulse width current pulse data. Fig. 90 shows the Power Dissipation waveform replicated in B2 spice.

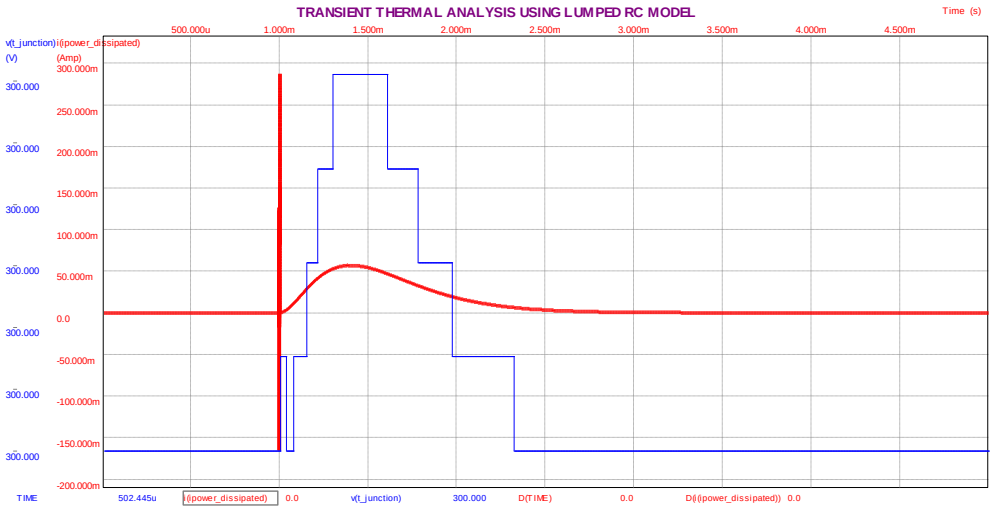

Figure 90. Power Dissipation Pulse (RED)

Fig. 91 shows the simulated temperature rise waveform. It can be observed that the temperature rise is happening only at the third decimal place and the temperature is rising from 300.000K to 300.003K.

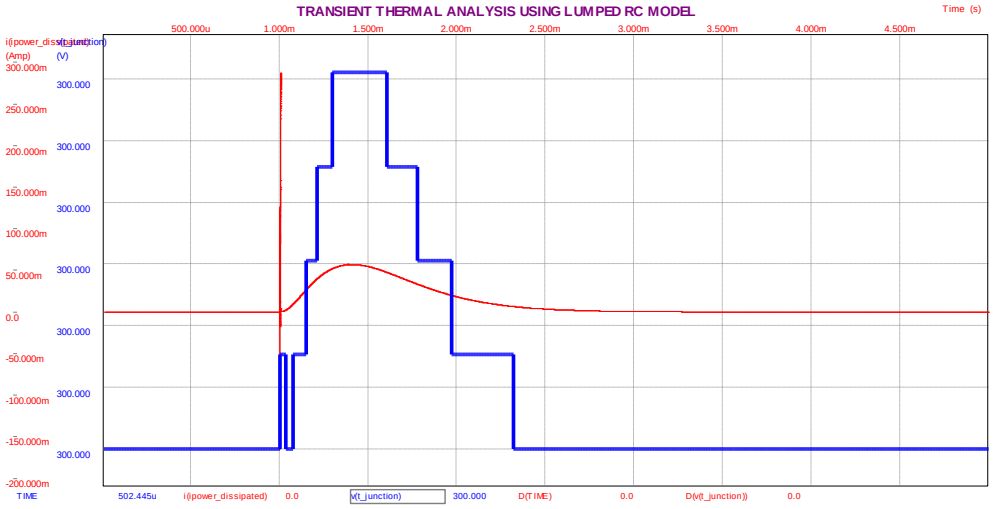

Figure 91. Junction Temperature Rise (BLUE)

15.3 SIMULATION OF 10A 50 µs PULSE AT 423K

The Power Dissipation data obtained from Tonyplot was used to create a piecewise current source. The following circuit (Fig. 92) was developed in B2 spice to simulate the transient thermal effects at 423K ambient temperature.

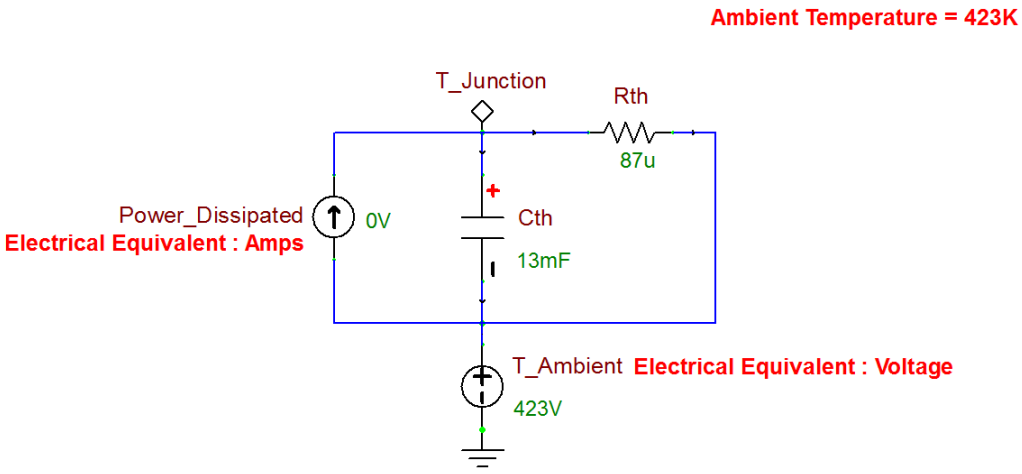

Figure 92. Thermal Circuit at Ambient Temperature = 423K

Fig. 93 shows the Power Dissipation waveform replicated in B2 spice.

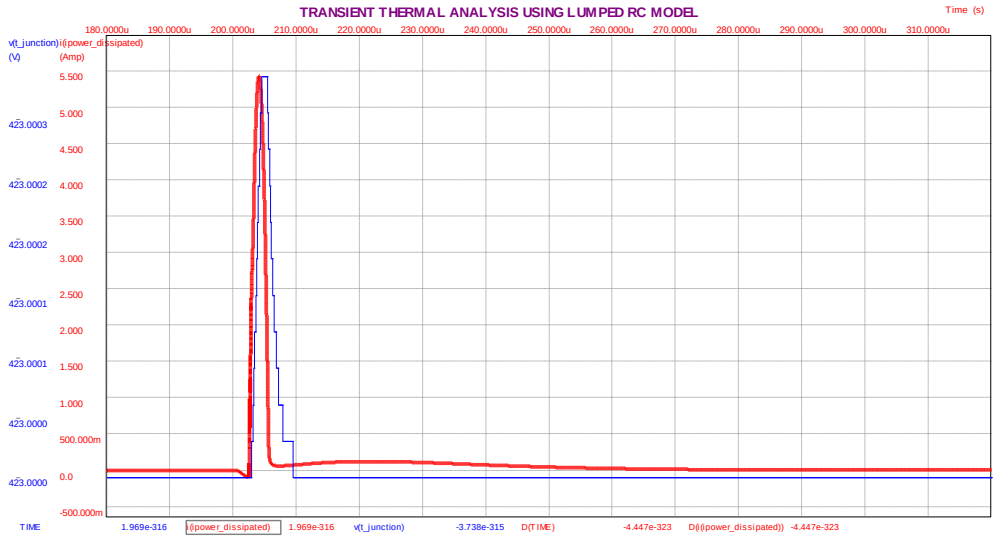

Figure 93. Power Dissipation Pulse (RED)

Fig. 94 shows the simulated temperature rise waveform. It can be observed that the temperature rise is happening at the fourth decimal place and the temperature is scaled from 423.0001K to 423.0003K.

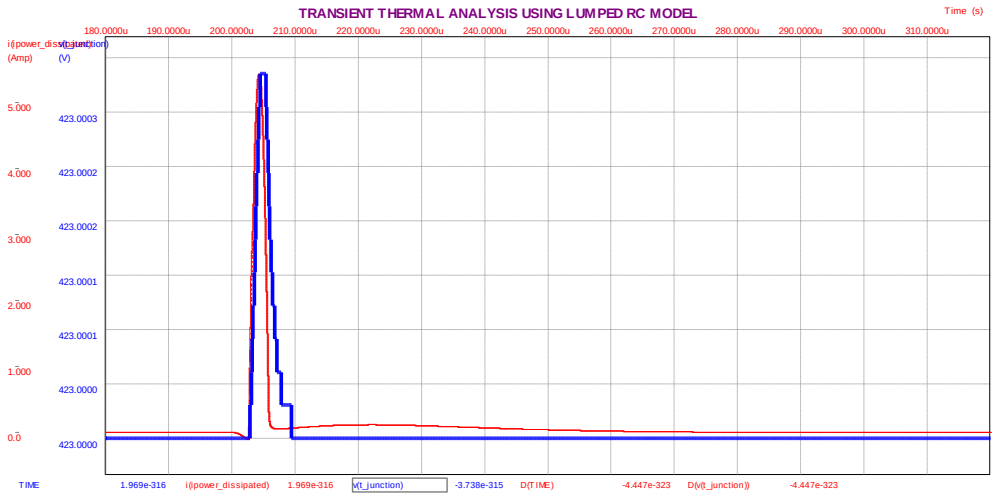

Figure 94. Junction Temperature Rise (BLUE)

15.4 SIMULATION OF 10A 1 ms PULSE AT 423K

The same circuit as in Fig. 92 was used to simulate the thermal circuit for 1 ms pulse width 10A current pulse data. Fig. 95 shows the Power Dissipation waveform replicated in B2 spice. As the pulse width of the current pulse increases, the conduction losses are more dominant.

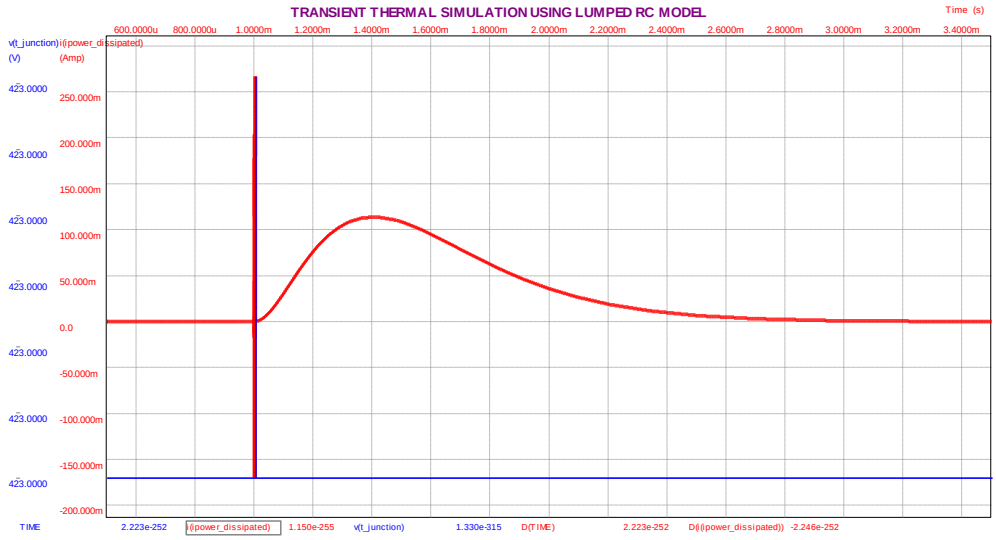

Figure 95. Power Dissipation Pulse (RED)

Fig. 96 shows the simulated temperature rise waveform. It can be observed that the temperature rise is happening beyond fourth decimal place and the temperature is scaled from 423.0000K to 423.0000K.

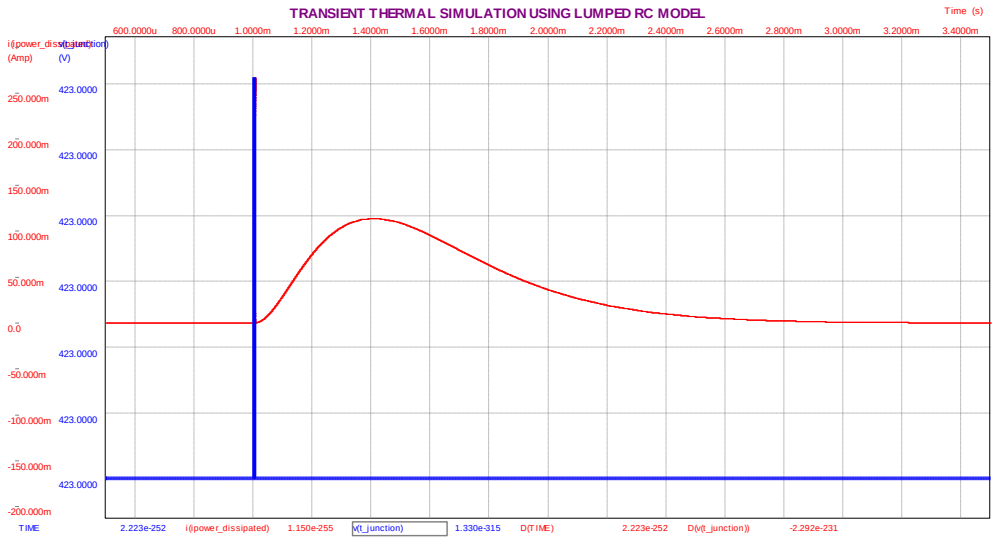

Figure 96. Junction Temperature Rise (BLUE)

CHAPTER 16

SUMMARY/CONCLUSION

A 2D model for 4H-SiC N-Channel D-MOSFET was designed using Silvaco ATLAS. The device breakdown characteristics were generated without artificially altering the intrinsic concentration of the material. This was accomplished using 128-bit extended simulation precision. The device breakdown voltage did not get altered even at 250°C. The MOSFET characteristics including the Drain Current vs. Drain Voltage and transfer characteristics were verified at elevated ambient temperature.

The Transient analysis of the D-MOSFET was carried out using current pulses designed for five and ten times the rated current density of 100A cm^{-2} at 27°C and 150°C ambient temperature conditions. The pulse width of the current pulses were varied to understand the transient performance. The results showed that switching losses were dominant when the current pulse widths were narrow and the conduction losses were dominant as the current pulse width increased. It was observed that as the ambient temperature increased the conduction losses increased due to the increasing on state resistance. Under all the simulation conditions including the worst case power dissipation, the energy dissipated was not sufficient enough to raise the Lattice temperature of the device.

Due to computational speed limitations, only half a cell was simulated for this thesis. Hence, future work on Silicon Carbide (4H-SiC)will consist of simulating multiple MOSFET cells on a single substrate, simulating a 3D MOSFET cell, plotting the Safe Operating Area (SOA) of the device via clamped inductive switching circuit simulation and moving on to high voltage IGBT .

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