Thermal Systems Modeling of Chemical Heat Integrated Power Source (CHIPS) to Survive Lunar Night Environments

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Nomenclature

c_p	=	heat capacitance
f	=	friction factor
G	=	thermal conductance
h	=	heat transfer coefficient
k	=	thermal conductivity
P	=	power
P_{ELEC}	=	power from Stirling Device
Pr	=	Prandtl number
$Q_{STIRING}$	=	heat input into Stirling Device
Q_{TANK}	=	heat input from reactor tank
Q_{THRM}	=	heat output from Stirling Device
$Q_{ALT,LOSS}$	=	alternator thermal loss
q	=	heat exchanger flow rate
Re	=	Reynolds number
T	=	temperature
T_h	=	Stirling device hot side temperature
T_c	=	Stirling device cold side temperature
ε^*	=	MLI effective emissivity
η	=	Stirling device conversion efficiency

I. Introduction

This paper presents the results of the systems level thermal modeling for a conceptual Chemical Heat Integrated Power Source (CHIPS). This proposed system offers a combined thermal and electrical power source to support survival of spacecraft operating in extreme low temperature lunar environments, without the use of radioisotope-based sources. A conceptual design study has been completed for this system, that uses heat generated by an exothermic chemical reaction in place of radioisotope or electrical heat sources. The goal of the study was to evaluate the feasibility of such a system through thermodynamic and chemical analysis and thermal modeling, and to identify technology gaps to inform a technology development and maturation plan. The specific technical objectives focused on delivery of 90 to 100 W_{th} thermal power and 30 to 40 W_e electrical power for 336 hours to a representative Commercial Lunar Payload Services (CLPS) lander, to support lunar surface survival and limited operations through a lunar night. The total system mass was targeted at ≤50 kg. A highly exothermic chemical reaction system is used to generate on-board electrical power for spacecraft systems, and thermal power to maintain critical spacecraft/lander systems within their allowable flight temperature (AFTs). Based on the very high energy content of the chemical

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reaction system, a much higher amount of heat per unit mass can be delivered to the spacecraft, relative to a rechargeable lithium-ion battery and electrical heater(s). Since radioisotope heaters or generators are not used, the system will be orders of magnitude lower in cost than a radioisotope heating/power unit, without the attendant regulatory complexities. As part of the CHIPS concept, a fraction of the thermal power generated is converted to electrical power via an appropriate thermal-to-electric converter technology (such as a free piston Stirling converter or a thermoelectric generator module), to provide power to critical loads. This approach is ideally suited to support operation of commercial landers (e.g., via the CLPS program). In most cases, these landers are only designed to operate during a portion of the lunar day, with no provision for survival through the lunar night. By supporting lunar night survival, a mission can be extended through the lunar night and at least into another lunar day, thus turning a nominal eight-day mission into a 36-day mission. Therefore, the current system demonstration will focus on scalability to support at least 336 hours (one lunar night) of continuous thermal and electrical power generation. Although initially targeted to support lunar equatorial landings, the technology is extensible to missions at the lunar poles, other extreme environments in the Solar System or even air-independent applications on Earth (e.g., ocean exploration).

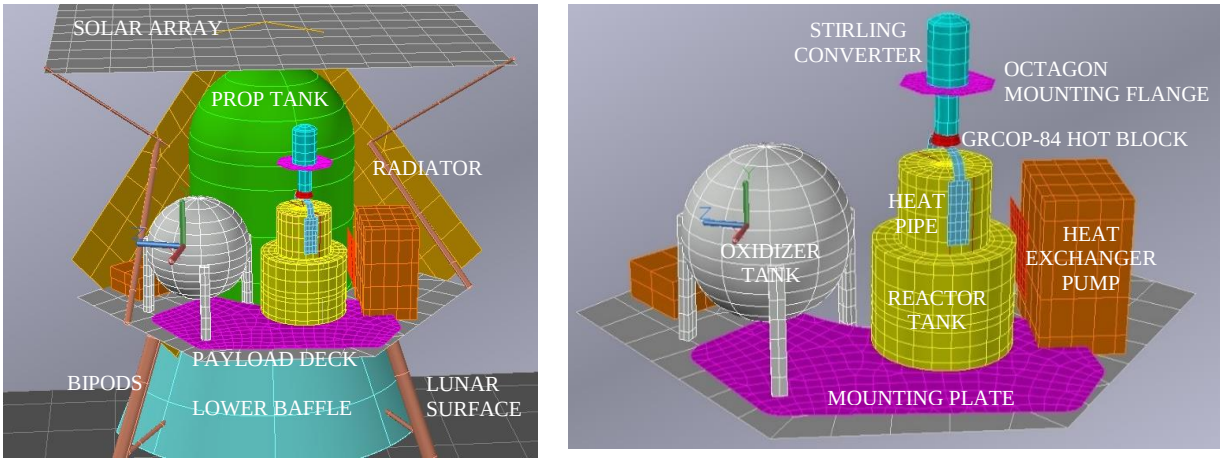
II. Thermal Modeling Methodology

This section describes the thermal systems modeling for a conceptual CHIPS design, supporting lunar night survival. To support the engineering trades studies needed to converge on a feasible conceptual design, developing an understating of the key heat flows, system temperatures, and key thermal system design sensitivities and tradeoffs using thermal modeling was critical. The objective guiding this modeling was the delivery of 90 to 100 W_{th} and 30 to 40 W_e for 336 hours (14 Earth days or one lunar night). The design is based on the use of the Li/ SF_6 reaction,

$$8Li + SF_6 \rightarrow 6LiF + Li_2S + 14{,}575 \text{ kJ/kg (reactants)} \quad (1)$$

yielding a reaction specific energy of 4,049 Wh/kg (based on reactant masses)[1-3]. The overall thermal system architecture is comprised of an oxidizer tank, an Li/SF_6 reactor tank, a Stirling converter[4-5], sodium heat pipes and a heat exchanger (HX) which interfaces with a lunar lander (See Figure 1). Typical hot (T_h) and cold (T_c) side Stirling converter temperatures are targeted-for 650 °C and 20 °C, respectively. Stirling conversion efficiencies are approximately 30%, based on prior testing of representative units at NASA GRC under similar operating conditions. The CHIPS system components have a mass of 71 kg. The lunar lander surface payload delivery capacity is 100 kg[6]. The mass breakdown of major system components that comprise the 71 kg CHIPS system are 34% reactor tank, 23% oxidizer tank, 21% heat exchanger/pump, 10% thermal isolation plate, 7% Stirling device, 4% electronics, and 1% heat pipe subassemblies, respectively. The CHIPS combined energy levels are expected to be in the 600 to 1000 Wh/kg range, placing the CHIPS technology above the best primary batteries, which are estimated to be in the 500 to 575 Wh/kg range at the pack level, whereas state-of-the-art lithium battery packs are estimated at 180 to 225 Wh/kg. The primary thermal system design challenge became matching the reactor and Stirling hot side temperatures and thermal flows because the Stirling conversion efficiency is highly temperature dependent. This was accomplished using sodium heat pipes. The systems level thermal model of the CHIPS concept was created in Thermal Desktop. The reactor tank was modeled as a volumetric heat source, and internal tank fins were included in the top segment to enhance the heat transfer from the reactant vapor volume to the reactor walls. Stirling converter performance data were implemented as a look-up function using FORTRAN based SINDA logic, within the framework of Thermal Desktop. The SINDA logic developed herein iterates to automatically compute the correct internal conductance values and power output/efficiency of the Stirling converter, thus providing a robust model which can be implemented parametrically in support of design trade studies. Key thermal interfaces include the heat pipe evaporator to tank wall, and the heat pipe condenser to Stirling hot side. Details of the design of these interfaces using metal foams and high thermal conductivity alloys are discussed below. Figure 1(a) shows the CHIPS thermal systems model and the neighboring lunar lander interfaces while Figure 1(b) shows the CHIPS hardware components. The interfaces for the lander were taken from public domain and vendor supplied data regarding the Astrobotic Peregrine Lander, since this lander design was the most well defined at the time of the study. Application to other CLPS landers will be evaluated in the future, as details of their configurations emerge. Boundary conditions for the surfaces of the lander were taken from conversations and data provided by CLPS vendor Astrobotic, regarding their Peregrine Lander. Key interface temperature boundary conditions for a lunar night scenario for the lunar lander include the following: Solar Array = 173.15 K, radiators = 298.15 K, propellant tank = 280.15 K, payload deck = 113.15 K, lower baffle = 228.15 K, bipods = 303.15 K, lunar regolith surface = 150 K. The 150 K regolith temperature refers to a local regolith temperature under the influence of lander hardware. The aforementioned temperatures are typical of a lunar night steady state

environment. Herein only steady state modeling was performed in support of the conceptual design phase of the project. The far-field regolith temperature was not considered for the preliminary steady-state thermal analysis. Future work necessarily will encompass the transient simulation of the CHIPS sub-system in start-up mode, and the influence of lunar lander components under various landing scenarios, capturing shadowing effects of the radiative and environmental heat loads imposed onto the CHIPS payload via the lunar regolith. For the present analysis, neither solar environmental loads or far field regolith effects were considered, but may be incorporated into future analyses. Figure 2 shows the overall thermal network of the CHIPS thermal sub-system.



(a) (b)

Figure 1. CHIPS Thermal System Level Model (a) CHIPS and Lander, (b) CHIPS Components.

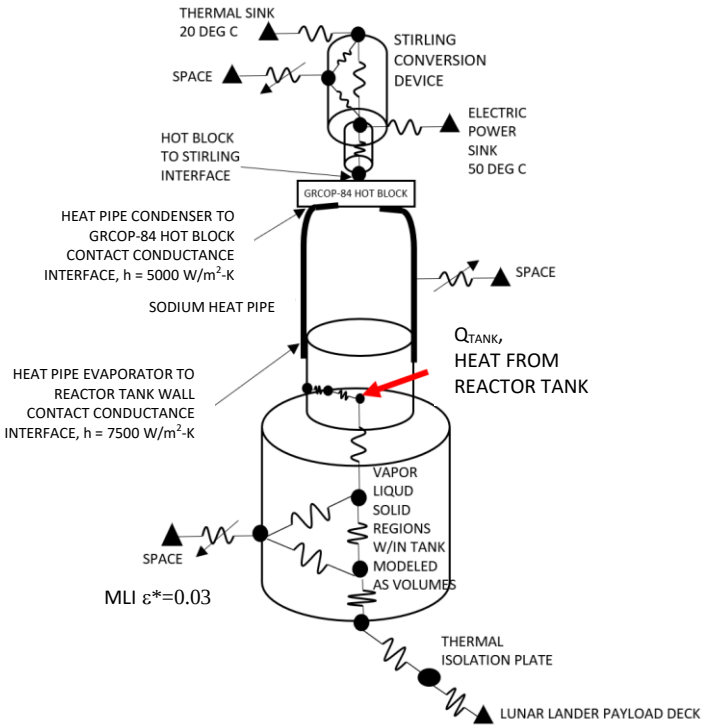


Figure 2. CHIPS Thermal System Level Model Network Diagram.

From Figure 2, it can be seen the heat flow path originates at the applied heat from the chemical reaction (chamber), which is modeled as a volumetric heat source within the Thermal Desktop model. The heat from the chemical reaction reaches the outer tank reactor wall via internal fin-enhanced conduction from the vapor region, and thermal energy

conducted through the tank wall is then picked up by the sodium heat pipe evaporator flange. The sodium heat pipes transport the thermal energy to the GRCOP-84 copper alloy hot head block (attached to the Stirling hot side), which is thermally tied to the heat pipe condenser flanges via a metal foam thermal interface. The sodium heat pipes are configured such that they are approximately 0.304 m (1 foot) long and operate in a performance-enhancing thermosyphon mode (i.e., vertical, evaporator down) relative to the moon's gravity vector. They could operate horizontally as well. The system is not anticipated to operate in a heat-pipe-condenser-down orientation, unless there is an unintended event creating such an off-nominal configuration. The GRCOP-84 material was selected based upon its temperature dependent thermal conductivity characteristics, structural properties and coefficient of thermal expansion (CTE). The hot side of the Stirling converter is tied to the GRCOP-84 copper alloy hot head with a metal-to-metal thermal interface. The heat input to the Stirling converter is then allocated into thermal power and converted to the appropriate electric power in the model using SINDA logic, as discussed below. Boundary nodes were used to mimic the thermal energy sink and the electric power sink, respectively. The thermal sink was based on information from Astrobotic regarding the operational temperature for their thermal bus. The electrical power sink conditions were estimated based on analogy with similar thermal systems. The base of the reactor tank is mounted to the CHIPS thermal isolation plate, which in turn is mounted to the Astrobotic payload deck (with representative conductor values for the various fasteners/bolts). Radiation was modeled using Monte Carlo ray tracing. In order to accurately model the Stirling converter, a detailed sub-model of the converter was developed as shown in Figure 3. The thermal/structural mounting plate serves as the interface to the thermal sink on the lander (i.e., its thermal bus). The heat input to the Stirling converter, $Q_{STIRING}$ (W_{th}) is converted to electrical power P_{ELEC} (W_e) which is routed to the power sink boundary node at 50 °C. The Stirling unit cold-side thermal power Q_{THRM} (W_{th}) is routed to the thermal sink boundary node at 20 °C.

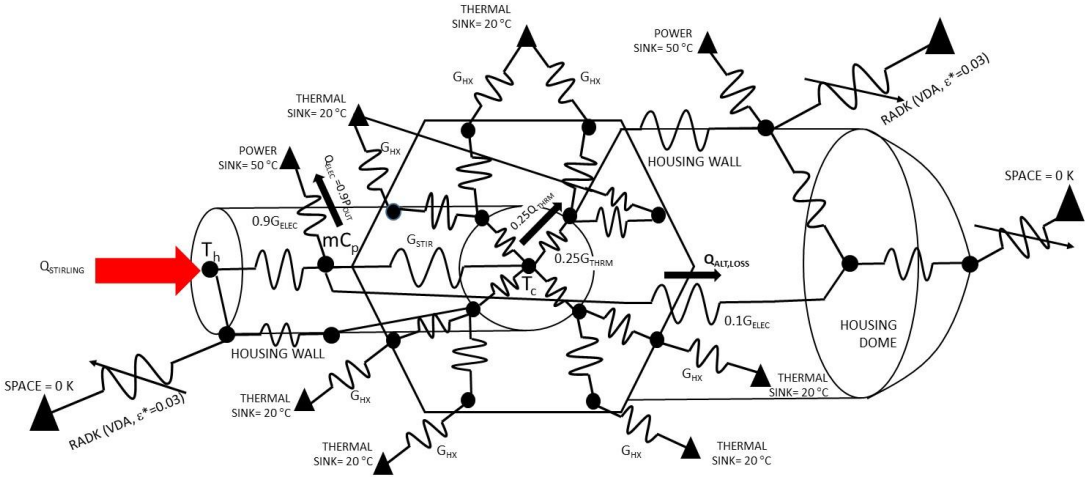


Figure 3. CHIPS Stirling Converter Device Thermal Network Diagram.

III. Stirling Converter Thermal Sub model

Next, details of the JPL developed SINDA logic to model the internal heat transfer of the Stirling converter are presented. Performance data of the Stirling converter was provided to the JPL team by the NASA Glenn Research Center. Typical performance data for a hot side temperature of 600 °C are shown in Figure 4. The thermal model for the CHIPS effort utilizes SINDA logic within the Thermal Desktop model. Figure 5 shows the flowchart used to implement the tri-variate array interpolation of the Stirling Converter performance data as a look-up function within VARIABLES 1 (wherein various values of hot side temperature and corresponding cold-side, throttling and efficiency such as those shown in Figure 4 are implemented). The if-then-else statements of Figure 5 are provided in order to allow the model to self-initialize. The logic uses intermediate variables *QSTIR1, QSTIR2, QSTIR3, QSTIR4* to model the heat *Q* input as *QSTIR* as listed in Figure 5.

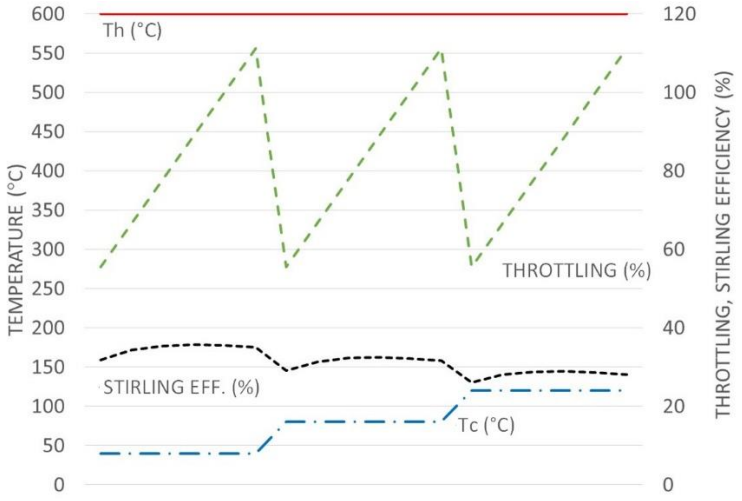


Figure 4. GRC Stirling Converter Performance Data for Hot side of 600 °C

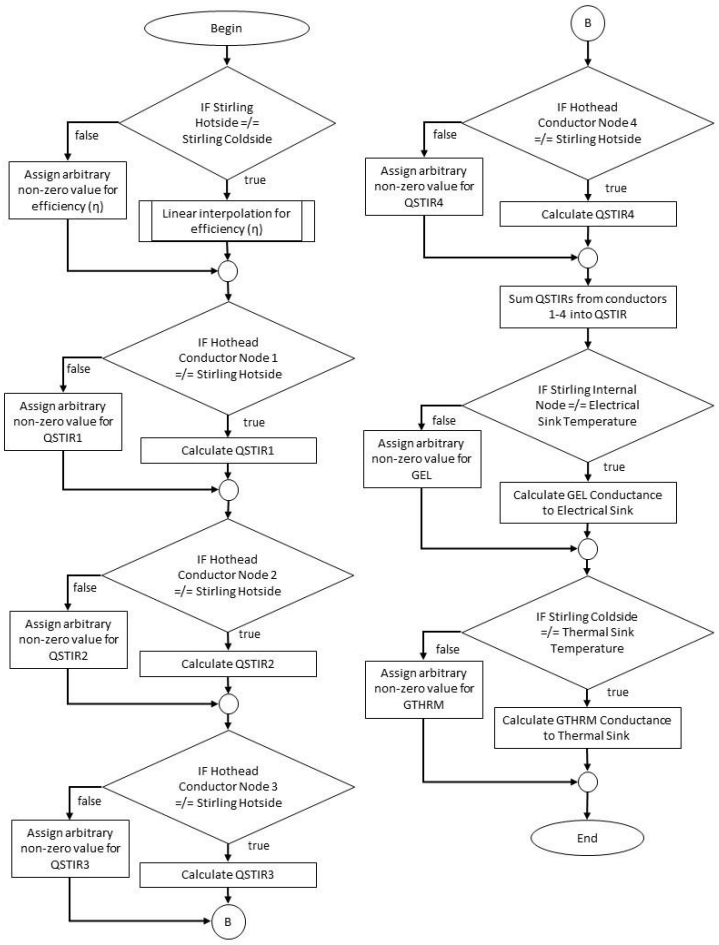


Figure 5. Stirling Efficiency and Thermal Conductor VARIABLES 1 SINDA Logic Flowchart.

The following energy balance is enforced across the thermal sub-model of the Stirling converter:

$$Q_{STIRLING} = Q_{THRM} + Q_{ALT,LOSS} + P_{ELEC} \quad (2)$$

where $Q_{STIRLING}$ (as shown in Figure 3) denotes the total hot-side thermal energy supplied to the Stirling converter from the heat pipes/hot head interface, Q_{THRM} denotes the Stirling system cold-side thermal heat flow (W_{th}), P_{ELEC} denotes the Stirling system electric power (W_e) and $Q_{ALT,LOSS}$ denotes the alternator thermal loss (W_{th}). The thermal logic used in SINDA VARIABLES1 is used to assign the thermal conductors G_{TRHM}, and G_{ELEC} for the thermal network model shown in Figure 3. Again, the various if-then-else statements are provided in order to allow the model to be self-initialized. The values of conductance (G_{ElEC} and G_{THRM}) shown in Figure 3 are computed internally within the solutions algorithms to give self-consistent heat flows and efficiencies during solution convergence according the following expressions. The following expression is used for the Stirling system electric power conductance

$$G_{ELEC} = \eta Q_{STIRLING}/\Delta T_{ELEC} \quad (3)$$

where η is the vendor provided value of the thermal efficiency of the Stirling converter, $Q_{STIRLING}$ is the heat flow (W_{th}) into the Stirling converter, and ΔT_{ELEC} is the temperature delta from the converter to the electric power interface boundary condition of the lunar lander. Thus, the Stirling converter efficiency is defined as follows

$$\eta = (G_{ELEC}/\Delta T_{ELEC})/Q_{STIRLING} = P_{ELEC}/Q_{STIRLING} \quad (4)$$

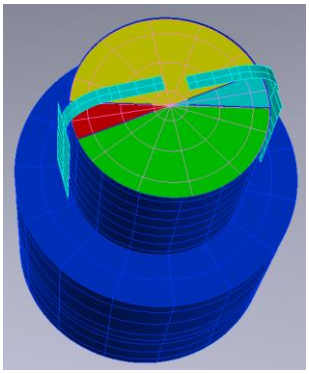
The Stirling system cold-side thermal heat flow conductance, G_{THRM} is given as follows

$$G_{THRM} = (1-\eta)Q_{STIRLING}/\Delta T_{THRM} \quad (5)$$

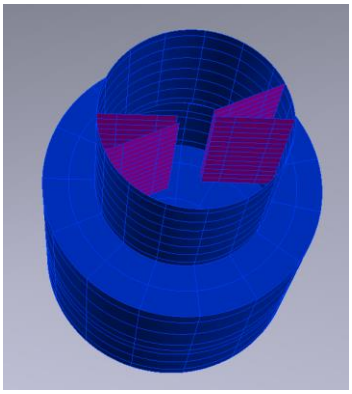
where ΔT_{THRM} is the temperature difference from the Stirling converter to the thermal loop interface boundary condition of the lunar lander. The alternator thermal loss $Q_{ALT,LOSS}$ is modeled as 10% of the overall electric power.

IV. Thermal Model Interfaces

As noted earlier, the heat input from the chemical reaction is modeled as a volumetric heat source. The details of the thermal model of the reactor tank, internal fins, internal reactor volume regions and heat pipe interfaces are shown in Figure 6.



(a) Vapor Volume Regions, Fins, Tank Wall, Heat Pipe Thermal Model Geometry

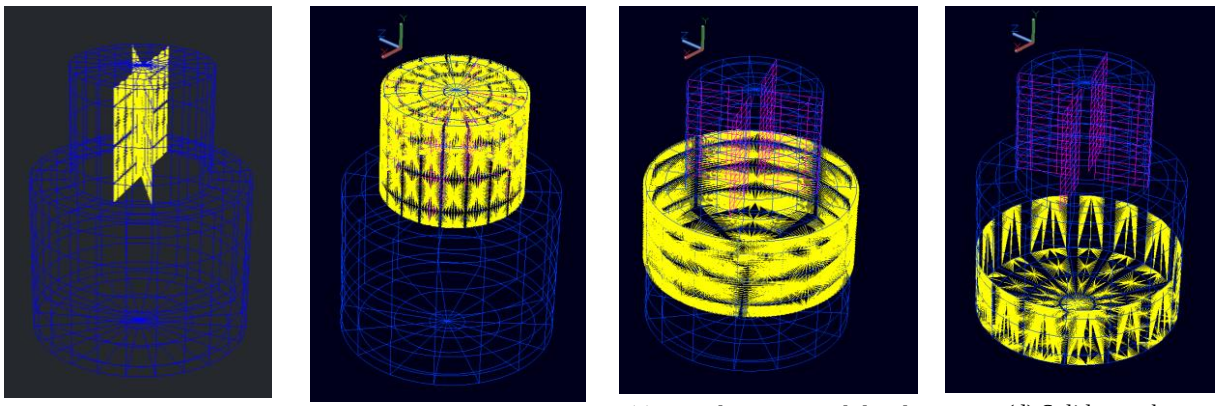


(b) Tank Wall, Fins, Thermal Model Geometry

Figure 6. CHIPS Thermal Model of Reactor Tank, Fins, Internal Volume Regions and Heat Pipe Interfaces.

Typical chemical-reaction-generated heat values based on 230 W_{th} input are given in terms of a volumetric heat generation rate of $\dot{q}$ = 8.62×10^{-5} W/mm^3 for the baseline tank volume considered in the conceptual design phase of the study. The vapor volume is modeled as a series of regions which are coupled to the liquid and solid and tank wall

regions within the reactor chamber. The left-hand panel of Fig. 6 shows a rendering of four tank vapor volume regions, showing their location in the vicinity of the internal tank fins. The tank internal fins were situated within the tank to carry heat from the vapor volume to the reactor tank walls, and subsequently to the heat pipe evaporator flanges. Figure 7 shows the various contact conductors associated with the volumetric discretization of the reactor tank. The vapor regions are connected to the fins via Thermal Desktop contactors. The lower region of the tank containing liquid and solids are modeled as volumetric regions, each interface (vapor-liquid, liquid-solid, vapor-walls, vapor-fins, liquid-walls, solid-walls) being assigned a contact conductance value in ranges: $5000 < h < 10000$ W/m^2-K. The values of contact conductance used were estimated by analogy with similar chemical systems and supporting bounding hand calculations guided by the handbook of Rohsenow *et al.*[7] Note, that no attempt has been made thus far to account for mass transfer across the interfaces.



(a) Fins to vapor (b) Vapor to tank (c) Liquid to vapor, solid and tank (d) Solid to tank

Figure 7. Reactor Tank Internal Vapor, Liquid, Solid Volume Regions and Contact Conductor Interfaces.

The thermal model was exercised in order to gain an understanding of the effect of reaction heat load on the tank wall temperatures, and subsequent thermal impacts (i.e., temperatures and heat flows) on components throughout the thermal model including the critical Stirling power converter. The key conclusions drawn from this exercise were that for a typical tank heat input of 230 W_{th}, the average temperature of the vapor region within the reactor tank will be on the order of 1000°C, while the tank wall will be on the order of 625°C. These temperatures are the primary drivers for selection of the Inconel tank reactor wall material and the use of the 12.7 mm diameter stainless steel sodium heat pipes, as baselined in the thermal design discussed herein.

The heat pipes were modeled using the industry-standard-practice systems-level approach, whereby an arithmetic vapor node is created in SINDA and tied to the surfaces mimicking the heat pipe internal two-phase heat transfer. The surface area and aspect ratio for the heat pipes is based upon 12.7 mm diameter stainless steel sodium heat pipes. The thermal conductivity of the heat pipe wall material is assigned as a value, in order to mimic the enhanced heat flow of the vapor front along the centerline of the heat pipe. This value of thermal conductivity is adjusted to match the vendor supplied performance data of the temperature drop across the evaporator to condenser end of the heat pipe. This is done in lieu of more complicated heat pipe subroutine-based modeling approaches, in order to retain the robustness of this systems-level conceptual model presented herein. The heat pipe surfaces are wrapped with 60 mm of Min-K TE-1400, 25.4 mm Aerogel, and MLI $\varepsilon^* = 0.03$, to mitigate parasitic heat losses. For the heat pipe condenser side to the Stirling hot head, an interface using a thermal contact conductance value of $h = 5000$ W/m^2-K is nominally used. For the heat pipe evaporator to reactor tank wall, an interface using a thermal contact conductance value of h = 7500 W/m^2-K is nominally used.

For the interface of the Stirling converter to the heat pipe condenser flanges, a hot block constructed from GRCOP-84 copper alloy was used. Based upon its thermal conductivity versus temperature characteristics, the GRCOP-84

copper alloy was selected as the interface material, in order to match the heat pipe condenser temperature to the acceptable hot head temperature of the Stirling converter. This thermal modeling effort highlighted the importance and impact of the reaction-chamber-to-heat-pipe evaporator thermal interface and the heat-pipe-condenser-to-Stirling-hot-head thermal interface on electrical power generation and thermal energy supplied to the lander for heating. These thermal interfaces inherently control the system electrical and thermal performance and dictate whether system requirements are satisfied. Another key thermal system parameter, parasitic heat loss mitigation, was found to be a key thermal design driver during the conceptual design phase. In order to mitigate parasitic T^4 radiative losses from the reactor tank walls, aerogel foam and Min-k insulation were added to the outer wall of the reactor tank, and subsequently covered with MLI Vapor Deposited Aluminum with an effective emissivity of $\varepsilon^* = 0.03$. The insulation consists of a Min-k inner layer, a 25.4 mm aerogel middle layer, and an MLI blanket outer layer.

V. Heat Exchanger Thermal Hydraulic Modeling

In this section of the paper we outline the thermal modeling of the Stirling Converter Cold-Side Heat Exchanger. Figure 8 shows the thermal network rendering of the heat exchanger thermal-hydraulic model.

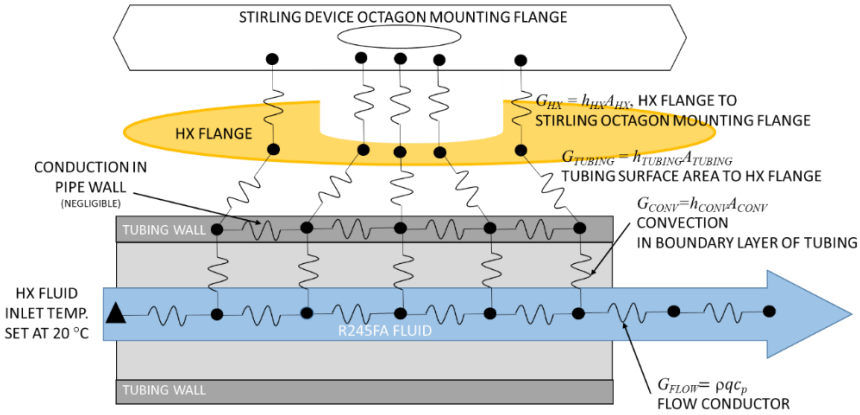


Figure 8. Heat Exchanger Thermal-Hydraulic Flow Network.

The VARIABLES 1 SINDA Logic flowchart for the thermal-hydraulic flow sub model is shown in Figure 9.

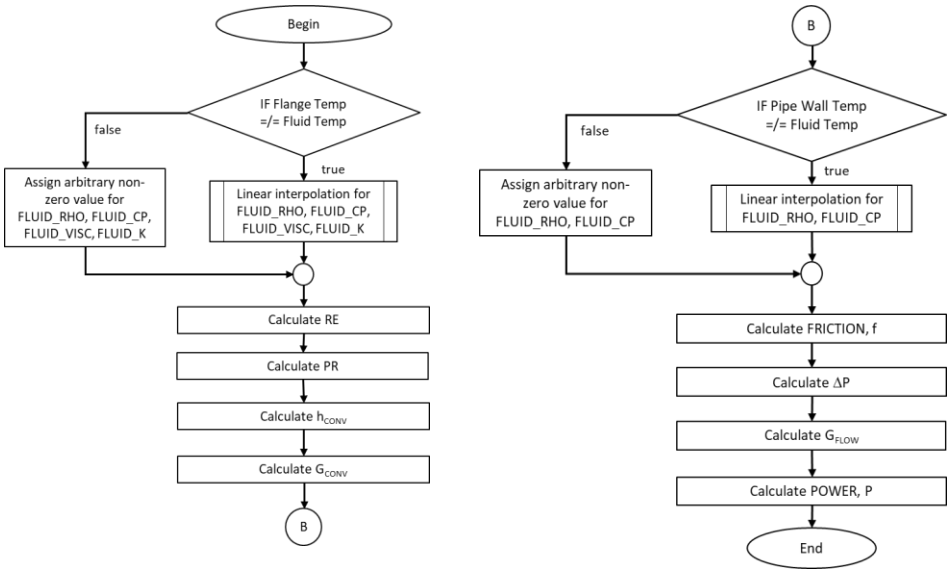


Figure 9. Heat Exchanger Thermal-Hydraulic VARIABLES 1 SINDA Logic Flowchart.

The logic of Figure 9 was developed in order to model the heat transfer and fluid flow characteristics of the Stirling converter cold-side heat exchanger interface to the lander thermal sink temperature. Herein a baseline design of a flat plate copper heat exchanger with copper tubing using Genetron R245fa as the working fluid was analyzed in order to assess pumping power requirements. The following thermal-hydraulic fluid flow and heat transfer relationships were programmed into the logic of the flowchart shown in Figure 9.

$$G_{HX} = h_{HX} A_{HX} \tag{6}$$

where A_{HX} denotes the contact area of the heat exchanger plate, and h_{HX} denotes the heat transfer contact conductance in units of W/m^2-K of the heat exchanger copper octagon mounting flange (see Figure 1(b)) of the Stirling device. The conductor for the contact area of the copper tubing of the heat exchanger to the heat exchanger plate is

$$G_{TUBING} = h_{TUBING} A_{TUBING} \tag{7}$$

where A_{TUBING} denotes the contact area of copper tubing on the heat exchanger plate, and h_{TUBING} denotes the heat transfer contact conductance in units of W/m^2-K . The thermal conductor for the wall thickness of the tubing is considered negligible for the model development. The thermal-hydraulic flow in the tubing is modeled using the Dittus-Boelter[8] single phase flow convection film heat transfer correlation for the Nusselt number

$$Nu = h_c D/k = 0.023 Re^{0.8} Pr^{0.3} \tag{8}$$

$$G_{CONV} = h_{CONV} A_{CONV} \tag{9}$$

$$Re = 4\rho q / A_i \mu \tag{10}$$

$$Pr = c_p \mu / k \tag{11}$$

where G_{CONV} denotes the thermal conductance in units of W/K based upon the convective boundary layer flow in the tubing, A_{CONV} denotes the convection flow surface area, q denotes the volumetric flow rate of the heat exchanger working fluid, h_{CONV} is the convective film heat transfer coefficient of the internal pipe flow, and *Re* denotes the pipe flow Reynolds number. In the above expression's various temperature dependent thermophysical properties (thermal conductivity, *k*; Prandtl number, *Pr;* density, ρ; viscosity, μ; and heat capacitance, c_p) are determined using the SINDA ARRAY based interpolation logic shown in the flowchart of Figure 9. The flow conductors of the pipe flow are modeled using the following relationships within the framework of SINDA LOGIC flowchart

$$G_{FLOW} = \rho q c_p \tag{12}$$

$$f = 0.316 * Re^{-.25} \tag{13}$$

$$\Delta p = 8 f L \rho(T) q^2 / \pi^2 D^5 \tag{14}$$

$$P = q \Delta p / \eta_p \tag{15}$$

where G_{FLOW} denotes the flow conductance in units of W/K of the fluid flow in the tubing, *f* denotes the tubing friction factor, Δp the pressure drop in tubing, η_p is the pump efficiency and *P* is the required pumping power to flow the working fluid through the heat exchanger. The pump efficiency was assumed to be 60%. This assumption was taken as a conservative estimate based upon vendor supplied pump design information.

Figure 10 shows the results of the parametric trade study of the flow rate in the heat exchangers. The target value of q = 1.5 L/min affords a pressure drop of Δp= 413.7 Pa = 0.06 psi, and a pumping power of P = 0.015 W. Knowing this pumping power is critical to allowing one to design, integrate and select a pump for this system to minimize the parasitic pump power, but requires further work to refine all of the pressure drop loses between the cold-side heat exchanger and a potential lander thermal bus interface. This is crucial to meeting our net system power requirement of 30 W_e.

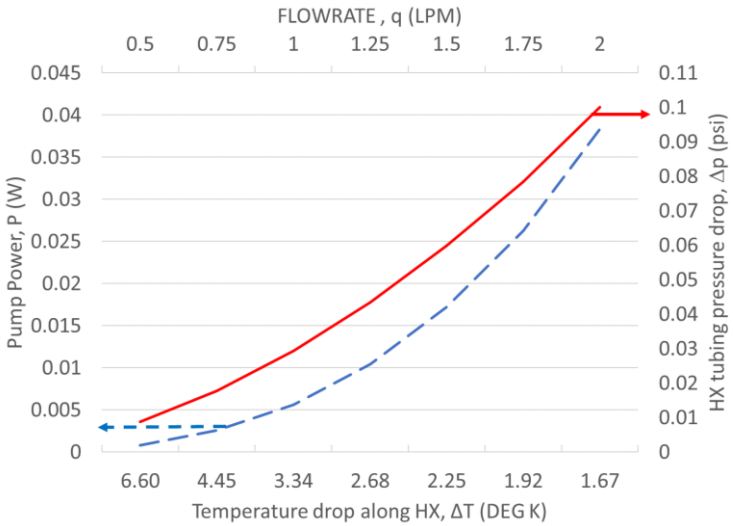
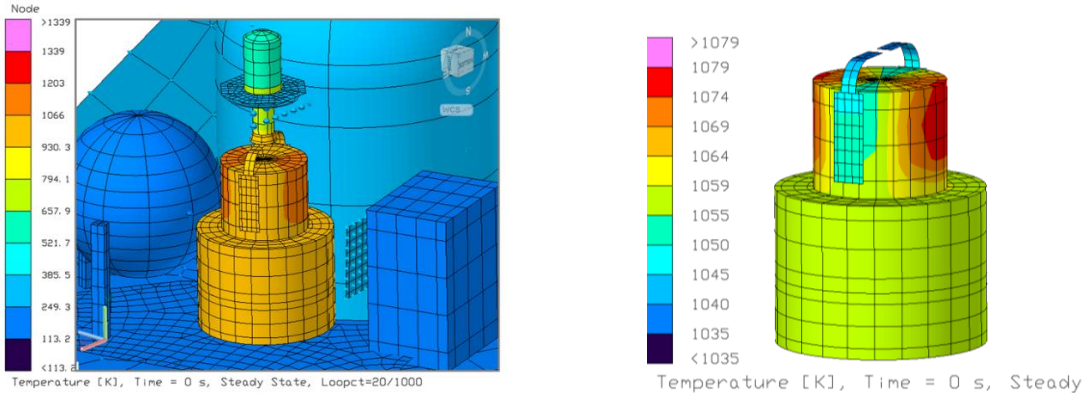


Figure 10. Effect of Heat Exchanger Flowrate on Pumping Power.

VI. Thermal Modeling Systems Level Predictions

This section of the paper presents typical results from the system level modeling effort. The power of this comprehensive thermal modeling approach is that it automatically and simultaneously computes the reaction chamber, heat pipe, Stirling power converter, and cold-side-to-lander temperatures, thermal flows and power output within the converged solutions. All system and component interdependencies are accommodated within the Thermal Desktop solution routines, so all the temperature, heat flow and power results are self-consistent with system energy balance requirements. Figure 11(a) show temperature contours of the CHIPS hardware and the landers neighboring interfaces. Figure 11(b) shows temperature contours for the CHIPS thermal subsystem. Results are shown for the following design parameters: 100% Throttling of the Stirling converter, Heat pipe interfaces: h = 5000 W/m^2-K (condenser to Stirling hot side thermal contact conductance – see Figure 2), h = 7500 W/m^2-K (reaction chamber wall to evaporator thermal contact conductance – see Figure 2), 60 mm thick Min-K ,with 25.4 mm thick Aerogel and MLI with ε* =0.03 on the reactor tank, MLI with ε* =0.03 on all other exposed surfaces (See Figure 11 showing geometry and surfaces). This thermal modeling work has investigated various interface and insulation design options and has shown that these thermal interface conductances and the thermal insulation design have a dramatic impact on system performance. Minimizing thermal losses through effective system design, MLI choices, and insulation choices, and sufficiently high thermal conductances are critical to achieving system performance requirements discussed herein.



(a) (b)

Figure 11. Thermal Temperature Contours for CHIPS Lunar Night Steady State Simulation.

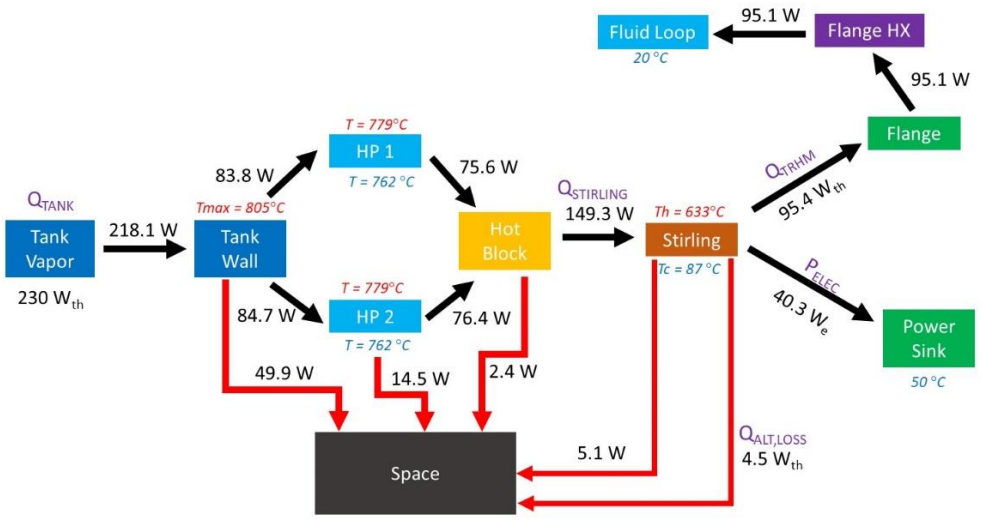


Figure 12. Systems Thermal Model Heat Map for 230 W Reactor Tank Heat Input

Figure 12 shows a typical heat map for steady state predictions. This affords 34% overall parasitic losses (9% heat pipe parasitic losses, 23% reactor tank wall parasitic). Thus, for an input of Q_{TANK}= 230 W_{th} input, Q_{THRM} = 95.4 W_{th}, $Q_{ALT,LOSS}$ = 4.5 W_e, P_{ELEC} = 40.3 W_e, corresponding to a hot-side and cold-side temperature of the Stirling converter of T_h= 633 °C, and T_c=87 °C, respectively and a $\eta = P_{ELEC}/Q_{STIRLING}$ = 27% Stirling efficiency as shown in the heat map of Figure 12. From the heat map of Figure 12, there is seen to be 6.4% parasitic losses from the Stirling converter, which is due to the 9.6 W losses through the Stirling housing. Based on the results of Figure 12, a combined 135.4 W (thermal + electric) for 336 hours is delivered, giving (135.4*336) Wh/71 kg = 641 Wh/kg. Preliminary studies currently in progress indicate that some of the reaction chamber thermal energy will need to be diverted from the reactor, to cool the SF_6 injector and keep it within desired temperature ranges in the Li/SF_6 reaction chamber. Thus, this will impact the system level thermal performance of the CHIPS hardware. Figure 13 shows the result of a trade study wherein the reactor tank heat input Q_{TANK} is varied in order to allocate cooling power to the SF_6 injector device. The impact of diverting cooling power to the injector on the outputs of Q_{THRM}, P_{ELEC} and $Q_{ALT,LOSS}$ as well as the hot side T_h, and cold side, T_c of the Stirling Conversion device is shown in Figure 13.

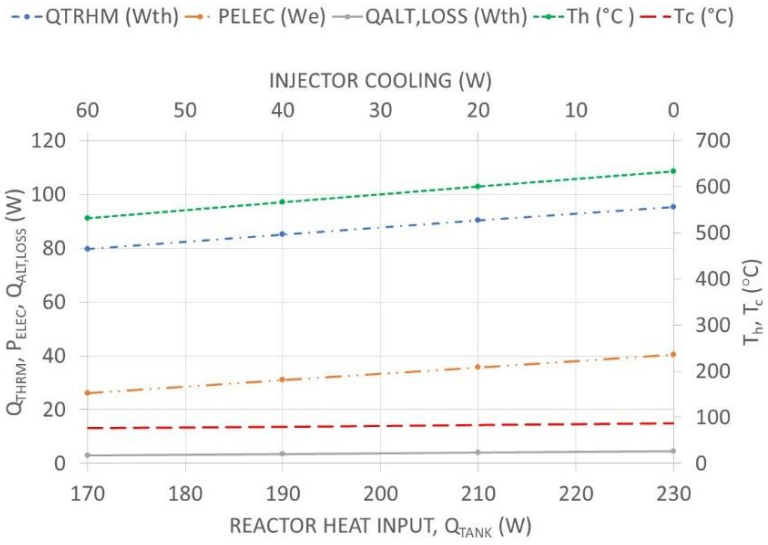


Figure 13. Systems Level Thermal Model Performance Trade Study

VII. Conclusion

This paper has presented the thermal systems modeling of the Chemical Heat Integrated Power Systems (CHIPS). The CHIPS system uses the heat generated via an exothermic Li/SF_6 reaction to drive a Stirling energy conversion device, thus producing thermal and electric power for use on long term Lunar night missions (i.e., 336 hours). The CHIPS thermal control system leverages the use of Li/SF_6 reactor tank, sodium heat pipe, Stirling converter and cold-side heat exchanger to lander interface as the key components of the thermal control system. Key to the development of the CHIPS systems-level Thermal Desktop thermal model was the use of SINDA logic to use tri-variate interpolation of vendor-based Stirling conversion device performance data in order to model its thermal behavior accurately. The critical interfaces of the sodium heat pipe to reactor tank and GRCop-84 hot block is also detailed herein. Use of high-performance thermal interfaces and minimization of parasitic losses were critical to meeting system performance goals of delivering 90 to 100 W_{th} thermal power and 30 to 40 W_e electrical power for 336 hours to a representative CLPS lander. Additionally, the systems level approach adopted herein using SINDA logic to model the heat exchanger and fluid loop from the Stirling conversion device to the lander heat sink has been presented. The power of the comprehensive thermal modeling approach (within Thermal Desktop) lies in the automatic and simultaneous computation of the reaction chamber, heat pipe, Stirling power converter, and cold-side-to-lander temperatures, thermal flows and power output within the converged solutions. Typical performance results in the form of heat maps, temperature contours, heat exchanger thermal hydraulic predictions and a trade study on the effects of reactor heat flow on Stirling conversion efficiency and overall thermal and electric power production are summarized and discussed herein. The systems level thermal heat transfer, fluid flow modeling of the CHIPS concept provided herein provides a road map for the technology development and validates the overall feasibility of the proposed concept.

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