ACKNOWLEDGEMENTS

I would like to first thank Aaron Wanstrath at AMD-Austin, for giving me an opportunity to work with his team. I also thank all my team members, especially Joe Martone and Dennis Mallory for their support throughout my thesis project. I also thank Radhesh for his support and motivation throughout my term at AMD.

I would like to thank Dr. Brian Nutter for being my Advisor, and for providing his guidance. He was always available when I had questions and also helped me with my thesis report. He gave valuable suggestions, which helped me make my project and report better.

I extend my sincere gratitude to Dr. Richard Gale for being an important member in my thesis committee and for guiding me throughout my Masters. He gave good suggestions that helped me streamline my thesis project.

I also thank my friends for their support and motivation. They were always there for me during difficult times and made my stay in Lubbock, a memorable one.

Finally, I would like to thank my Mom for her love and care. She made sure I had the best education possible and provided constant support through all my ventures.

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ABSTRACT

Testing of devices is an important factor in the semiconductor industry. There is a constant effort by major semiconductor companies to bring down test cost and time without compromising on the test quality. Implementation of built in self test techniques (BIST) are required, especially for complex components like microprocessors.

Several challenges are associated with the development of BIST techniques and the development of such techniques on automated test equipment (ATE) is time consuming. This thesis project is an attempt to address the challenges associated with the development of a certain BIST, called cache resident self testing (CReST), developed at AMD. In CReST, test vectors are loaded into the cache of the microprocessor, and the processor is used to test itself.

In this work, high speed IO links in the processor are tested. The device under test is an AMD processor with a G34 package, having four HyperTransport links.

The work includes debugging an engineering device interface board (DIB) developed to implement the loopback test, avoiding certain tester channels. This passive loopback DIB gives better performance and is expected to be used in production testing soon. A comparison of the loopback and the production DIB is presented. Also the aspects of loopback testing and principles of CReST are discussed, along with an overview of the ATE used for this process

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