A COMPENSATION TECHNIQUE FOR INTEGRATOR LEAKAGE ERROR IN SIGMA-DELTA MODULATORS

by

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The common problem faced in many high-resolution Sigma-Delta topologies is their sensitivity to the imperfections of the analog components, especially the integrator. This thesis deals in depth with the physical causes of the deviations in the integrator transfer function and their effects on the Sigma-Delta modulator performance and then proposes a solution for the elimination of the integrator pole error that has been proven as the main error in the integrators. The concept of feedback has been used to eliminate the integrator leakage (pole) error and this concept has been analyzed and also verified by comparing the power spectral densities of two modulators of which, one uses this concept and the other doesn’t.
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CHAPTER I
INTRODUCTION

In recent years, Delta-Sigma modulation has gained much interest as a technique for analog to digital conversion. As an oversampling technique, Delta-Sigma modulation has several important advantages over Nyquist-rate converters such as successive approximation and flash. In theory, Sigma-Delta modulation can provide unlimited signal-to-noise ratio, or equivalently, an unlimited number of bits of resolution by increasing the oversampling factor. The resolution of the conversion can be further improved by using a higher order loop filter. This, however, impairs or destroys the stability of the loop. The cascade structure or the MASH structure provides the higher-order noise shaping combined with the robust stability of a first order system.

The overall converter performance in general is largely determined by the characteristics of the analog components, especially the integrator, particularly in the case of cascaded modulators. The actual integrator transfer function differs from the ideal case due to nonzero switch resistance, finite op-amp bandwidth, and finite op-amp gain. It has been proven that the pole error in the integrator is the main cause for the decrease in the resolution. This error in the first integrator of the cascade results in the leakage of unshaped quantization noise to the converter output, which plays the main part in not achieving the desired resolution. It has also been proven that the pole error is mainly due to the finite dc gain of the op-amp. A very high gain op-amp could be used to increase the resolution, but this in turn would increase the area and eventually the cost.
The objective of this research is geared towards proposing a compensation technique that would eliminate the pole error in the integrator. This, when incorporated in the Sigma-Delta converter could achieve better resolution with even lower gain op-amps.

The thesis starts with an overview of different Sigma-Delta modulator topologies and their limitations, proving that the integrator pole error is the main cause for the decrease in SNR in many high-resolution Sigma-Delta topologies. The integrator errors are dealt in depth in Chapter III. Chapter III continues with the proposed method for eliminating the integrator leakage error and its verification. The implementation of the concept is also discussed in chapter IV. This chapter includes the design and simulations of the modulators in fully-differential switched-capacitor circuits. Chapter V is the conclusion of the thesis.
CHAPTER II
AN OVERVIEW OF SIGMA-DELTA MODULATORS

2.1 Oversampling Modulators

Quantization of amplitude and sampling in time are at the heart of all digital modulators. The process of quantization can be represented by the equation

\[ Y = G \cdot X + e \]  \hspace{1cm} (2.1)

Where \( Y \) is the quantized signal and \( X \) is the input to the quantizer. The gain \( G \) is the slope of the straight line that passes through the center of the quantization characteristic. The error ‘\( e \)’ is called the quantizer error. This error is completely defined by the input. However, if the input changes randomly between samples by amounts comparable with the threshold spacing without causing saturation, then the error is uncorrelated from sample to sample and has equal probability of lying anywhere in the range ± \( \Delta /2 \) (\( \Delta \) is the level spacing of the quantizer). Thus, treating the quantization error ‘\( e \)’ as white noise having equal probability of lying anywhere in the range ± \( \Delta /2 \), its mean square value is given by

\[ e^2_{\text{rms}} = \frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} e^2 \, de = \frac{\Delta^3}{12} \] \hspace{1cm} (2.2)

When a quantized signal is sampled at frequency \( f_s = 1/T \), all of its noise power folds into the frequency band \( 0 \leq f \leq f_s \) [1,2,3]. Then, if it is white, the spectral density of the sampled noise is given by
\[ E(f) = e_{\text{rms}} \sqrt{\frac{2}{f_s}} = e_{\text{rms}} \sqrt{2T}. \] (2.3)

Considering a signal in the frequency band \( 0 \leq f \leq f_o \), the oversampling ratio is defined as the ratio of the sampling frequency \( f_s \) to the Nyquist rate \( 2f_o \) and is given by the integer

\[ OSR = \frac{f_s}{2f_o}. \] (2.4)

Therefore, the noise power that falls into the signal band will be

\[ n^2_o = \int e^2(f)df = e^2_{\text{rms}}(2f_oT) = \frac{e^2_{\text{rms}}}{OSR}. \] (2.5)

Thus, the oversampling ratio reduces the inband rms quantization noise by the square root of the oversampling ratio. Therefore, each doubling of the sampling frequency decreases the in-band noise by 3 dB, increasing the resolution by half a bit.

2.2 Delta–Sigma Modulators

2.2.1 First-Order Converter

Delta-Sigma modulator [1,2,3] shown in Fig. 2.1a is a better option in the category of oversampling quantizers. The input to the circuit is fed to the quantizer via an integrator, and the quantized output is fed back and subtracted from the input. This feedback forces the average value of the quantized signal to track the average input. Any difference between them accumulates in the integrator and eventually corrects itself. The modulator is analyzed by means of the circuit shown in Fig. 2.1b. Here the quantization is represented as an added error \( e \) in accordance with equation (2.1), with the gain \( G \) set
to unity. Since it is a sampled data circuit, the integration can be represented as an accumulation.

\[
\text{Integrator} \quad W(t) \\
\text{Quantizer} \\
Y(t)
\]

Then the output of the accumulator is

\[ w_i = x_{i-1} - e_{i-1} \]  \hspace{1cm} (2.6)

and the quantized signal is

\[ y_i = x_{i-1} + (e_i - e_{i-1}) \]  \hspace{1cm} (2.7)

Thus, the circuit differentiates the quantization error, making the modulation noise the first difference of the quantization error while leaving the signal unchanged, except for a delay. The spectral density of the modulation noise

\[ n_i = e_i - e_{i-1} \]  \hspace{1cm} (2.8)
may then be expressed as \([1,2,3]\)

\[
N(f) = E(f) \left| 1 - e^{-j\omega T} \right| = 2 e_{rms} \sqrt{2T} \sin(\omega T / 2).
\] (2.9)

where \(\omega = 2\pi f\).

The feedback around the quantizer reduces the noise at low frequencies, but increases it at high frequencies. The noise power of the signal band is

\[
n^2_\omega = \int_0^{f_s} \left| N(F) \right|^2 df = e_{rms}^2 \pi^2 (2f_o T)^3.
\] (2.10)

and its rms value is

\[
n_o = e_{rms} \pi \sqrt{3 \text{OSR}}^{-3/2}.
\] (2.11)

It is seen that each doubling of the oversampling ratio reduces this noise by 9 dB and provides 1.5 bits of extra resolution. This is definitely a much greater improvement as compared to any other oversampling converter. However, this improvement in the resolution requires that the modulated signal be decimated to the Nyquist rate with a sharply selective digital filter.

### 2.2.2 Higher-Order Converter

The technique of Sigma-Delta modulation can be extended to provide higher-order predictions by adding more feedback loops to the circuit. Fig. 2.2 shows the second order structure. In general, when there are \(L\) loops and if the system is stable, the spectral density of the modulation is \([1,2,3]\)

\[
N_L(f) = e_{rms} \sqrt{2T} \left[ 2 \sin\left(\frac{\omega T}{2}\right) \right]^L.
\] (2.12)
For oversampling ratios greater than 2, the rms noise in the signal band is given approximately by

\[ n_o = e_{rms} \frac{\pi^L}{\sqrt{2L+1}} (2f_0T)^{L+1/2}. \]  

(2.13)

Fig. 2.2 Higher-Order Candy’s Structure.

Thus, the quantization noise falls \(3(2L+1)\) dB for every doubling of the sampling rate, providing \((L+0.5)\) extra bits. In general, any order Sigma-Delta modulator’s stability can be analyzed using the Fig. 2.3 where \(G/H\) is the transfer function of the system from the signal input to the output and \((H-1)/H\) is the transfer function for the error input (Noise transfer function-NTF). The linear analysis suggests that in order for any modulator to be stable the quantizer must not be allowed to become too large compared to the quantizer’s input range. The input according to Fig. 2.3 is given by
\[ Y(z) = G(z)U(z) + (H(z) - 1)E(Z). \]  
\[ (2.14) \]

This requirement leads to the conclusion that the gain of \((H(z) - 1)\), or simply the gain of \(H(z)\) must not be too large. Since the higher order modulators with a NTF of the form \(H(z) = (1 - z^{-1})^n\) have a peak gain of \(|H(-1)| = 2^n\), the higher order modulators may not be stable.

2.2.3 Multibit Converters

Instead of single bit comparators, a multibit analog-to-digital converter can be used to quantize the integrator output, reducing the mean square value of the quantization error as shown in Fig. 2.4. This method reduces the noise level as compared to the single-bit modulators. However, this approach requires a multibit converter in the feedback loop, increasing the cost of the system as linearity of the DAC should equal the overall converter resolution. A different, but less popular approach to improving resolution uses multibit quantization for the integrator output but only single-bit feedback [2] as shown in Fig. 2.5. The output of this modulator [1,2,3] is

\[ y(z) = x(z)z^{-1} + (1 - z^{-1})e_2(z) \]  
\[ (2.20) \]
where $e_2$ is the error of the multibit quantizer and is much less than the error of a single bit quantizer. Further improvement can be obtained using the topology shown in Fig. 2.6.

Fig. 2.5 Leslie-Singh Architecture

Fig. 2.6 Architecture proposed by Kinyua and Chao.
2.2.4 Cascaded Converters

Fig. 2.7 shows a cascade of two Sigma-Delta modulators. In this topology, the input to the second modulator is the error from the first modulator. The output of the second modulator is digitally recombined with the first modulation output to cancel the modulation error due to the first-stage quantizer, letting only the second modulator error to be present at the output along with the delayed input. Since a cascaded modulator structure contains only feedforward paths and no feedback between the individual modulators, it is stable as long as the individual stages are stable. The output of the cascaded stage is

\[ y(z) = x(z)z^{-2} + e_2(z)(1 - z^{-1})^2. \]  

(2.20)

The equation is the same as that of the second-order Candy’s structure. However, to derive this transfer function it was assumed that the analog components of each stage are identical. In practice, however, the integrator has many variations from its ideal transfer
function due to the nonidealties of the op-amp. The transfer function of the integrator including these nonidealties as pole and gain errors is defined as

\[ H_{int}(z) = \frac{(1-\alpha)z^{-1}}{1-(1-\beta)z^{-1}}. \]

where \( \alpha \) is the gain error and \( \beta \) is the pole error. Fig. 2.8 shows the same cascade (1-1) stage. The integrators with the gain and pole errors are used in place of the ideal integrators. The pole and gain errors of the two integrators rarely match. So the pole and the gain errors in two stages are given different values. The effect of the imperfections of the integrator on the output of the cascade stage can be found by analyzing the circuit for the output. Carrying out the analysis the output is

\[ Y_1(z) = x(1-\alpha_1)z^{-1} + e_1(1-(1-\beta_1)z^{-1}). \quad (2.22) \]

\[ Y_2(z) = e_1(1-\alpha_2)z^{-1} + e_2(1-(1-\beta_2)z^{-1}) \quad (2.23) \]

\[ Y(z) = Y_1(z) * z^{-1} + Y_2(z) * (1 - z^{-1}) \quad (2.24) \]

Fig. 2.8 (1-1) Cascade Stage including the Integrator Errors.
Thus, due to the nonideal characteristics of the analog components, a first stage unshaped noise and also a first-order noise shaped error leaks to the output. However, the dominant one among them is the uncanceled and unshaped noise from the first modulator. This is a major drawback of the cascaded Sigma-Delta technique; the cancellation of quantization noise of the first modulator is dependent on the accuracy of the analog components. Thus the nonzero pole error \( \beta \) causes a leakage of unshaped quantization noise to the output of the modulator. Fig. 2.9 shows the Matlab simulated results of a (1-1) cascade modulator using an integrator of ideal transfer function and also of the same modulator using an integrator which has a pole error \( \beta \) of 0.001 (corresponding to an op-amp gain of 60 dB). The results prove the above discussion that the pole error is the cause for the leakage of unshaped noise into the base band, thus, increasing the noise and preventing the modulator from achieving its expected resolution. An improvement of more than 5 dB could be achieved if the pole error could be completely eliminated. For example, since the noise is unshaped, \( e_i \) is attenuated by a decimation filter with an oversampling ratio of 64 and decreases 9 dB per doubling of the oversampling ratio decreases 9 dB per doubling of the oversampling ratio. Thus the gain error noise after the decimation filtering, with an oversampling ratio of 64 is given by \( N_{ge} = -60.7 + 20 \log \alpha \) dB, where -60.7 dB is the standard noise output. The discussion shows that the integrator gain and pole errors have a significant effect on the performance of a cascaded Sigma Delta modulator. The most important error is in the first integrator of the first modulator
2.2.5 Pipelined Converters

The advantages of both the so called pipelined and the noise shaping converters are combined into one topology in the pipelined Sigma-Delta modulator with interstage scaling [4]. In a simple pipelined Sigma-Delta structure, one first-order sigma delta loop and a multibit quantizer form a unit of the pipeline. The residue in the first unit is scaled and fed into the second unit, as in a standard pipelined analog-to-digital converter architecture. The output from the second unit is digitally recombined with the output of the first stage to cancel the quantization errors of the first stage and also the single bit error in the second stage. The final output has only the multibit quantizer error of the
second stage. The topology if implemented properly could give very high resolution at high frequencies. However, one of the important sources of error in the efficient implementation of this topology is again the integrator leakage error that again increases the inband noise, reducing the achievable resolution.

The above discussions illustrate the basic concept of Sigma-Delta Analog-Digital (ADC) conversion, and the limitations of different topologies. The approach for ADC system design is to create a very robust and cost effective system that produces high performance while using components of only moderate precision. The common problem in all the high-resolution Sigma-Delta structures is the integrator leakage error. In the following chapter, the physical causes of the gain and the pole errors are discussed and a compensation technique is proposed to eliminate the integrator pole error for achieving the goal of building a high resolution converter using an imperfect integrator.
Chapter III

INTEGRATOR LEAKAGE ERROR

3.1 Sources of Error in the Integrator

3.1.1 Linear Effects

It is clear from the discussion of the previous chapter that the pole error is the main hindrance in achieving high resolution in almost all Sigma-Delta topologies. This section deals with the physical causes of the gain and the pole errors in the integrator. Fig. 3.1 shows the fully differential switched capacitor implementation of an integrator.

![Fig. 3.1 Fully Differential Switched Capacitor Implementation of the Integrator](image)

The pole and the gain errors in the integrator transfer function are caused physically by the finite op-amp gain, finite op-amp bandwidth and also the non-zero switch resistance [11,12]. Thus, deriving the transfer function $H(z)$ of the integrator taking into consideration each effect separately helps to decide the relative importance of these nonidealities.
For finite op-amp gain $A$,

$$H(z) = \frac{(c_1 / c_2)z^{-1/2}(1 - 1/A - c_1/(c_2A))}{1 - (1 - c_1/(Ac_2))z^{-1}}$$

(3.1)

For finite op-amp bandwidth $B$ (in Hertz)

$$H(z) = \frac{(c_1 / c_2)z^{-1/2}[(1 - \varepsilon) + z^{-1}\varepsilon c_2/(c_1 + c_2)]}{1 - z^{-1}}$$

(3.2)

where $\varepsilon = e^{-\pi B T_s}$. For nonzero switch resistance $R_{ON}$

$$H(z) = \frac{(c_1 / c_2)z^{-1/2}(1 - 2e^{-T_s/4R_{ON}C_i})}{1 - z^{-1}}$$

(3.3)

Capacitor mismatch causes the gain error in a straightforward manner, since the gain of the integrator is determined by the ratio of the switched input capacitor to the integration capacitor. As can be seen from the above equations, gain error is caused also by finite op-amp gain and incomplete linear settling due to switch resistance or finite op-amp bandwidth. Equations (3.2) and (3.3) indicate that the op-amp bandwidth and the switch resistance do not cause the pole error. The pole error as seen from equation (3.1) is inversely proportional to the op-amp gain. Thus, increasing the gain of the op-amp decreases the pole error.

3.1.2 Nonlinear Effects

Nonlinear effects are difficult to handle analytically, inaccurate to simulate, and sometimes even difficult to consider physically [3,4]. Because of noise shaping, nonlinear effects are most important at the input (switched input capacitor). The next most important nonlinearities are the output of the first integrator (nonlinear integrating
capacitor, nonlinear op-amp) and the input to the second integrator. Distortion in succeeding integrators is less important. The effect of a nonlinear element will depend on the structure of the modulator. If the relative nonlinearity does not change, increasing the open-loop op-amp gain will help reduce distortion due to the op-amp. Decreasing the gain of the integrator will improve the distortion performance as well as the settling time but will increase the effect of nonidealties of the succeeding integrators. Minimizing distortion without sacrificing too much performance in other areas is the best way nonlinearties could be dealt due to the difficulty of modeling these very small effects [3,4].

3.2 Proposed Algorithm

As shown in the previous chapter, gain error is not of main concern in single loop or even cascaded modulator, because it causes leakage of noise to the overall modulator output that is shaped to the same order as the order of the first modulator in the cascade. A pole error has little effect on the performance of a single modulator. However, in a cascaded modulator, proved from the analysis in the previous chapter, pole error will cause the leakage of noise to the overall modulator output that is shaped to one order less than the order of the first modulator in the cascade. In fact many topologies including the cascaded structure achieve greater resolutions if the pole error in the integrator is eliminated [1,2,3]. The discussion above proves that the main cause of the pole error is the finite op-amp gain. So, the op-amp gain can be increased to reduce the pole errors. But this will in turn increase the area of the transistors and eventually the cost. Many
techniques were proposed to minimize the pole error without changing the op-amp parameters [13,14,15,16,17]. This thesis is concerned with a compensation technique that could completely eliminate the pole error without increasing the op-amp gain. Fig. 3.2 shows the block diagram of a compensated integrator.

![Compensated Integrator Diagram]

Fig. 3.2 Compensated Integrator

It uses the concept of feedback to completely eliminate the integrator leakage error. Giving a positive feedback $\beta$ completely eliminates the integrator pole error, thus making the integrator insensitive to the op-amp gain. This technique does not even need the capacitor ratio to be equal. It is practically not possible to make the capacitors values the same. Stability of the loop is of minimum concern here since the magnitude of positive feedback is very small (order of $1/A$) and this small quantity does not make the loop unstable and will rule out the chance of oscillation too. Many error problems can be handled by this kind of feedback but avoided because of the inherent characteristic of the positive feedback to destabilise the system and thus deteriorate its performance instead of actually improving it. This problem as explained before is not the case of this particular Circuit. For the system to be unstable the magnitude needs to be much higher even for a positive feedback.
3.3 Verification of the Principle

To verify the use of the feedback to eliminate the pole error, modulators with and without the feedback are compared using the Matlab simulation tool, Simulink. The compensated integrator has been simulated in the first stage of the (1-1) cascade structure. The test frequency used is 9 kHz. The results show the superior performance in resolution. There is an improvement of 7 dB in the total SNR. This same resolution could be achieved using a lower gain op-amp than this, thus decreasing the integrator’s sensitivity and thereby the Sigma-Delta modulator’s sensitivity to the dc gain of the op-amp. Fig. 3.3 shows the simulation results of the cascade (1-1) stage with an ideal integrator, the modulator with a pole error of .001(op-amp gain of 60 dB) and the one with the compensated integrator in the first stage of the cascade. The ideal integrator is also compared with the remaining two stages in the same graph. The improvement in the baseband in case of the system using the feedback is clearly seen. The power spectral density (PSD) of the compensated integrator is the same as the PSD of the modulator with an ideal integrator except for a small difference. This could be attributed to the leakage of the single noise shaped first stage quantization error due to the gain error in the integrator. The feedback gives a better noise shaping to the spectrum in the baseband. This is to be expected since the presence of the pole error causes the unshaped noise to be shown at the output, increasing the noise at low frequencies. For low frequency applications this is the noise that has to be eliminated. And this system can achieve that, thus proving it as a very important concept in the low frequency applications. The discussion below also explains the concept over a wide signal range, which is very useful for low amplitude signals.
Fig. 3.4 shows the variation of SNR obtained by varying the signal amplitude.

Again the two are compared but over a wide range of amplitude. The results very clearly show that there is a greater improvement in the total SNR due to this feedback at lower signal amplitude. However, the SNR is also less in this case. All the simulations for the verification of this concept are done above -10dB keeping in mind the signal useful range. Thus, this concept gives a greater improvement if applied to systems with a smaller signal range. These simulations are also verified by simulating the same cascade (1-1) stage in 1.2u process to transistor level in CMOS technology in the next chapter. The stage with the compensated integrator and stage without the compensated integrator is implemented and are then compared among themselves and also with the results in this chapter. The variations in the results are also analyzed. The program Spice is used to
carry out the transistor level simulations. The next chapter explains the implementation of each block of the circuit. Detailed analysis is done on the results and also on the implementation methods.

![Graph of SNR Variations with Amplitude for a Cascade (1-1) Stage](image)

**Fig. 3.4** Graph of SNR Variations with Amplitude for a Cascade (1-1) Stage

### 3.4 Implementation of the Principle

The implementation of this compensation technique in switched capacitor circuit in single ended configuration is shown in Fig. 3.5. From the transfer function of the equation (3.1), the pole error, $\beta$ is $c_1/(c_2A)$. So, the feedback to the integrator, $V_f$, is $V_o/A$ where $V_o$ is the output of the integrator. The quantity $V_o\beta$ is $V_f$ that is fed back. An op-amp in a unity gain configuration can be used as this buffer. Thus, this
compensation technique would need one extra single-ended buffer (two in case of a differential implementation) and few switches. In the integrating phase, the input to the buffer, as shown in Fig. 3.5, is taken from the input of the integrator and its output is given to the switching capacitor. If the common mode input and output reference voltages for the op-amps in the integrator and the buffer are the same, the buffer will maintain the dc voltage level necessary at the input of the integrator.

![Inv Buffer](image)

**Fig. 3.5 Single Side Implementation**

According to equation (3.1), the pole error, $\beta$ is $c_1/(c_2A)$. So, the feedback to the integrator, $V_f$, is $V_o/A$ where $V_o$ is the output of the integrator. The quantity $V_o\beta$ is $V_f$ that is fed back. An op-amp in a unity gain configuration can be used as this buffer. Thus, this compensation technique would need one extra single ended buffer (two in case of a differential implementation) and few switches. The next section deals with the analysis of the circuit. Transfer functions are derived using the analysis and they are then compared with the previous one.
3.4.1 Analysis of the Switched Capacitor Circuit

During phase $\phi_1$, the circuit is shown in Fig. 3.6 and Fig. 3.7 in phase $\phi_2$.

Equating the charges at the node $@$ before and after the closing the switches at phase $\phi_1$

$$V_0^+(n - \frac{1}{2}) = V_0^+ (n - 1)$$

Similarly applying the conservation of charge at node $@$ during phase $\phi_2$

$$C_2 \left( -\frac{V_{0^+} (n - \frac{1}{2})}{A} - V_{0^+} (n - \frac{1}{2}) \right) = C_2 \left( -\frac{V_{0^+} (n - 1)}{A} - V_{0^+} (n - 1) \right)$$

Substituting (3.4) in (3.5) and taking the Z transform on both sides results in

$$C_2 V_{0^+} (z)(1 - z^{-1})(1 + \frac{1}{A}) = C_1 V_{\circ} (z) z^{-1/2}$$

and

$$
\therefore \frac{c_1}{c_2} z^{-1/2} = \frac{H(z)}{(1 + \frac{1}{A})(1 - z^{-1})}
$$
The transfer function agrees with the linear analysis showing that the feedback eliminates the pole error. The transfer function is derived by assuming that the buffer is ideal. However, owing to the small input and output of the buffer, the offset of the op-amp in the buffer might pose a problem. This offset problem is taken care by the switching circuitry shown in Fig. 3.8.

The switches in one phase of the offset cancellation circuitry store the offset and the
stored offset voltage is fed along with the input in reversed polarity in the next phase, thus canceling the offset. This offset circuitry can be implemented very easily with switches and capacitors.
CHAPTER IV
CIRCUIT LEVEL SIMULATION AND VERIFICATION OF THE PRINCIPLE

To verify the results further, the cascade stage with and without the proposed compensated integrator in the first stage of the Sigma- Delta Modulator has been simulated in 1.2 μ process in CMOS technology in a fully differential configuration. The single-bit first-order sigma-delta modulator, discussed in the previous chapters comprises of an integrator and a comparator configured as the 1 bit analog-to-digital converter. An op-amp forms the core of the integrator. After the introduction of the first 2 stages, the design and implementation of the op-amp and the comparator are discussed.

4.1 Single Stage

The circuit diagram of the modulator is shown in Fig. 4.1. The circuit is designed using a two-phase non-overlapping clock. In phase \(\phi_1\), the sampling capacitor charges to the input voltage. The next phase is the integrating phase, in which the negative of the input along with the feedback value is integrated. The negative output of the integrator is the sum of the positive input and the negative feedback value. This value is given to the positive input of the comparator that decides between a +5 value and 0 depending on the value of the input. The negative triggered D flipflop that is given the same clock as the comparator is used to latch the value of this output, to be used later in the feedback control circuitry. The feedback values are set depending upon the input maximum range of the quantizer and also the integrator. If the output is positive, then a negative value is
the comparator is used to latch the value of this output, to be used later in the feedback control circuitry. The feedback values are set depending upon the input maximum range.
of the quantizer and also the integrator. If the output is positive, then a negative value is fed back in the next integrating phase along with the next input sample. This makes the error at the output of the modulator the difference of the present error and the past error, thereby gives the desired noise shaping in the frequency spectrum.

4.2 Second stage

Fig. 4.2 is a schematic diagram of a structure that can be used for the second modulator in the cascade stage.

Fig. 4.2 Second Stage of the Cascade (1-1) Modulator.
This is identical to the first stage except for doubling the size of the feedback capacitors and the addition of some control switches in the feedback. The feedback circuitry is now controlled by the output of this stage and also the previous stage. The input to this stage is the integrator output of the first stage. The feedback value is actually the logical addition of this stage’s output and the previous stage’s output. If the present modulator and the previous modulator outputs are different, the feedback signal is zero. If they are the same, then the feedback signal is either +2 or -2, depending on the sign of the outputs. This is the reason behind doubling the feedback capacitors. In fact, the input to the stage is the negative of the first stage quantization noise. This will not affect the output if the digital circuitry at the end of the modulator is adjusted accordingly.

4.3 Core Circuits

4.3.1 Operational Amplifier

The input to the integrator is the difference of the input signal and feedback digital to analog converter output. For the single-bit feedback system implemented, the feedback signal can change from negative reference to the positive reference, i.e., (+Δ). When integrated it could possibly change the integrator output by Δ. For sinusoidal signal inputs it can be shown that the output of the integrator is limited to values +Δ and -Δ, a total swing of 2Δ. This typically is the maximum signal voltage swing in the system and it ultimately determines Δ and consequently the maximum signal input x(t) to the system. For a 5 V supply and fully differential configuration, the maximum possible output swing is ±5 V.
For a practical circuit the maximum gain region is typically ±3 V. Every cycle, the integrator output can possibly change by Δ. The output of the op-amp must be able to make this transition within a half of the clock period. The settling behavior of the integrator is determined by the op-amp slew rate (SR) and its unity gain bandwidth (UGB). Large signal settling is determined by both factors, while small signal settling is determined by the latter factor alone. Since the integrator handles large signal changes, both the SR and UGB specifications are important.

For large signal changes, the swing is mostly limited by the slew-rate. The UGB and the phase margin determine the final settling time to the required accuracy. For sampling rate of 1 MHz and Δ of 3 V, a slew rate of 12 V is required. However, for a sampling rate of 50 MHz, this increases to 600 V/μs, which is difficult specification to meet with CMOS single stage op-amps. The use of second-stage in the op-amp, biased to produce higher output current drive and consequently higher SR, introduces a second pole in the op-amp, limiting its UGB.

Since the op-amp small signal settling should occur within one-half the clock period, the UGB should be at least an order larger than 2 MHz for a 1 MHz clock and 100 MHz for a 50 MHz clock. Further, minimum settling time is assured if the op-amp has a phase margin between 60 and 70. The next important parameter is the op-amp open loop gain. Generally, for the cascade structure to prevent the unshaped noise in the output, a gain of minimum 80 dB is desirable. However for the compensated system, a gain of 40-60 dB is sufficient, thus reducing the size of the transistors and also the area.

The use of fully differential circuitry serves to mitigate the effects of common
mode signals. In fact, common-mode voltages at the input and output need to be fixed by the circuitry external to the op-amp. The effects of clock feedthrough, signal dependent charge injection, noise coupling from substrate due to parasitic capacitance are also reduced due to the fully differential configuration.

The op-amp configuration that is best suited for such application is the folded-cascode configuration [18,19] shown in Fig. 4.3. In this single stage design, the primary pole is determined by the load capacitance and the second pole is determined by the parasitic capacitance. This parasitic pole is well separated from the main pole, allowing for a high UGB. Output common mode voltage can be set by the switched capacitor techniques, transistors operating in linear region or by separate common mode amplifier. Because of this suitability, the folded cascode configuration is used with a separate common mode amplifier to set the output common-mode voltage. In what follows, the detailed design considerations are given. The folded cascode circuit has a greater output swing than a cascode circuit. The output voltage swing of the op-amp is determined by the cascode P transistors, in the positive direction, and by the cascode N transistors, in the negative direction. For given specifications of DC gain 57 dB, unity gain bandwidth 400 MHz, SR 600 V/us, and the load capacitance $C_L=1$ pf, the equations used to design the core stage of the op-amp, are given below.

For the unity gain frequency

$$\omega_o = \frac{g_{m1} \omega_o}{C_L}$$

SR is related to $I_{ss}$
\[ I_{SS} = 2 \times SR \times c_L \]
\[ I_{DS1} = \frac{1}{2} I_{SS} \]

\[ I_{\text{casc}} = \omega_c c_{il} \tan(\Delta V_O) + \]

usually

\[ I_{\text{CASC}} = 1.5 \times I_{DS1} \]

\[ A_0 = \frac{g_{m1}}{g_{d7}g_{d8} + \left( g_{d1} + g_{d5} \right) g_{d6}} \]

\[ g_{m7} = \frac{A_0 \left( g_{d7} g_{d8} g_{m6} \right)}{g_{m1} g_{m6} - A_0 \left( g_{d1} + g_{d5} \right) g_{d6}} \]

The bias circuit and the common-mode feedback circuits are designed to meet the
requirements of this core circuitry. In this op-amp an external current reference is used to bias the circuit.

### 4.3.2 Comparator

The high signal-to-noise ratio obtained from a sigma-delta converter utilizing a coarse quantizer is primarily because of the fact that the quantization noise introduced by the quantizer is noise shaped. Any signal introduced between the integrator and quantizer is noise shaped. For this reason the nonidealties in the implementation of the quantizer are noise shaped and their effect on the signal-to-noise ratio is negligible. However, single bit quantizer is preferred in the sigma-delta loop to prevent the addition of a digital-to analog converters since its not noise shaped. A latch type comparator, that has the advantage of high speed, is suitable for this application as a single bit quantizer. Typically a resolution and offset in the vicinity of 10mv, and the hysteresis in the order of the 5% of the step size are tolerated and response time is in the order of few tens of nanoseconds. In the discussion that follows the detail explanation of the operation of this comparator is given.

The comparator designed and shown in Fig. 4.4 is based on the regenerative latch. The comparator is made up of three stages, preamp, positive feedback decision circuit and output buffers. When $\phi_2$ (phase of the comparator) is low, the p channels are isolated from the n-channels. In addition, the output of the decision circuit are pulled high, that is, the outputs of the comparator are low. When the phase is high, the regenerative action of the latch combined with preamplifier causes an imbalance in the decision circuit, forcing the outputs into a state determined by the inputs.
The preamplifier stage is used mainly to prevent the kickback to enter the driving circuitry and also the very large glitches. Kickback denotes the charge transfer either into or out of the inputs when the track and latch stage goes from track mode to latch mode. This charge transfer is caused by the charge needed to turn the transistors in the positive feedback circuitry on and by the charge that must be removed to turn the transistors in the track circuitry off. The preamplifier produces the impedance needed for this charge transfer. An added advantage of using the preamplifier stage is the extra gain, However, gains much greater than 10 for the preamplifier stage cause its time constant to become large and thus limits the speed, especially in the track mode. So care is taken to design the amplifier to fix a particular gain that will not impair the comparator performance and instead improve its gain performance.
4.3.3 Switch

The transmission gate has been used as a switch consistently throughout the design. The requirement of the switches used is that the ‘ON’ resistance should be such that the capacitors being switched settle to their final voltage with the required accuracy in one phase at the maximum clock speed to be used. This again sets the maximum clock frequency that can be utilized. Increasing the switch size involves a trade off of adding the parasitic capacitance that contributes to charge injection into the signal path from the clock signal.

4.3.4 Capacitors

The accuracy of the integrator depend upon the ratio matching of the capacitors since the gain of this circuit is directly proportional to capacitor ratio. This is also a factor in the expression for the pole error. This pole error is the dominant limitation on the signal-to noise ratio of the cascade modulators. However, in the design under consideration, the mismatch in the sampling and the integrator capacitor does not degrade the signal-to- noise ratio. Capacitor’s accuracy has always been the difficult part in the integrated analog circuit design. This design as said before does not need that the capacitors match because the feedback into the same capacitors cancel their mismatch factor. This is an added advantage in the design. This design has an overall smaller sensitivity to the analog components specially the capacitors.

4.4 System Integration

As explained in the previous sections, each part is designed to meet the
specifications of the total system and the core circuitry is aligned to form the stages shown in Figs. 4.1 and 4.2. Both these stages are then cascaded by giving the integrator output of the first stage to the second stage. The system without the compensated integrator is also implemented to note the differences in the performance of the two modulators. The circuit-level simulations are conducted using PSpice and Fig. 4.5 shows the results of these simulations.

![Fig. 4.5 Results of the P-Spice Implementation of the Cascade (1-1) Modulator](image)

These individual stages are simulated and the system is integrated together again. The circuit diagrams used for the P-Spice simulations are shown in the appendix. They are the schematic files of the simulation. They were used to verify the transistor level implementation. The results are presented in next section.
4.5 Results

These are the results from the analysis of the graphs:

1. The results obtained from the Pspice circuit-level simulations clearly verify the results of the MATLAB simulations.

2. The improvement seen due to the feedback is less in the circuit-level implementation as compared to the MATLAB simulations. This loss in improvement could be attributed to the nonideal switches that cause the charge injection errors. The charge injection error is present in every switched capacitor circuit, but it is of greater importance in the switching circuitry before the buffers due to the fact that the input to the buffer as well as the output of the buffer is a voltage of small value. The fed back value is only $V_o/A$.

3. In spite of the decreased improvement there is very clearly an improvement of 4 dB in the total SNR when feedback is used in the first stage of the integrator, thereby proving the practicality of the system.

4. This improvement of 4 dB was achieved for a system which uses a much lower gain op-amp (57 dB) as compared to the systems which use op-amps of gain in the order of 80-90 dB. This same resolution should also be achieved with much lower gain op-amps.
A new compensation technique to eliminate the integrator leakage error in Sigma-Delta modulators has been proposed for achieving high resolutions. This technique when embedded into the integrator of the first stage of a cascade circuit, reduces the sensitivity of the circuit to the dc gain of the integrator. A lower gain op-amp could be used to achieve the same resolution, thus reducing the cost and also the chip area. The use of switch circuitry that minimizes the charge injection errors is the key to effectively incorporate this technique in Sigma-Delta modulators.

The proposed system has been implemented in 1.2 micron CMOS technology using switched-capacitor circuits. A robust design procedure for fully differential implementation of this modulator has been presented. The results of the Matlab simulations have been verified with the P-spice implementation. However, nonidealties in the implementation and in the switching circuitry limit the performance obtained.

The implemented system is the simplest topology that uses the general concept of feedback to eliminate the integrator leakage error. Further work could implement the same principle in a different manner with the possibility of eliminating the use of buffer stage. The reduction of the charge-injection errors in the switched-capacitor circuitry is the subject of ongoing research. The proposed system will greatly benefit from the results of such research, extending the capabilities of the cascade topologies.
REFERENCES


APPENDIX
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