HfO_2 gate dielectric with 0.5 nm equivalent oxide thickness

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Hafnium dioxide films have been deposited using reactive electron beam evaporation in oxygen on hydrogenated Si(100) surfaces. The capacitance–voltage curves of as-deposited metal(Ti)–insulator–semiconductor structures exhibited large hysteresis and frequency dispersion. With post-deposition annealing in hydrogen at 300 °C, the frequency dispersion decreased to less than 1%/decade, while the hysteresis was reduced to 20 mV at flatband. An equivalent oxide thickness of 0.5 nm was achieved for HfO_2 thickness of 3.0 nm. We attribute this result to a combination of pristine hydrogen saturated silicon surfaces, room temperature dielectric deposition, and low temperature hydrogen annealing. © *2002 American Institute of Physics.*
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Considerable effort is being exerted to find a high dielectric constant replacement for SiO_2 in complementary metal–oxide–semiconductor (CMOS) devices. Hafnium and zirconium oxides are the leading candidates,[1] and viable devices have been fabricated using sputtering,[2,3] metal organic chemical vapor deposition,[4,5] and atomic layer chemical vapor deposition.[6] Equivalent oxide thickness as low as 1.0 nm has been reported.[2] However, the presence of SiO_x interlayer decreases the effective dielectric constant of the gate stack and limits the equivalent oxide thickness.

Preparation of hafnium dioxide by electron beam (e-beam) evaporation has been studied for optical coatings in the near-UV.[7] Lehan *et al.*,[8] showed that the refractive index and homogeneity were strongly dependent on the partial pressure of O_2 during deposition, in agreement with Baumeister and Arnon.[7] However, our survey of literature found no work done on e-beam evaporated hafnium dioxide for thin film transistor gate materials. We show here that a combination of silicon cleaning, low temperature hafnium dioxide e-beam evaporation in O_2, and post-deposition annealing in hydrogen, results in metal–insulator–semiconductor (MIS) structures that exhibit drastically reduced frequency dispersion and hysteresis.

Before deposition of the hafnium dioxide, *p*-type (100) silicon with a resistivity of 10 Ω cm was etched using a modified Shiraki[9] process. This cleaning method consists of the growth of a thick silicon dioxide, followed by several iterations of etching and thin silicon dioxide growth. The last step consists of etching with 10%–20% HF in ethyl alcohol, followed by drying the wafer with compressed nitrogen. There is no final deionized water rinse. This method produces an atomically flat, hydrogen-passivated surface. We believe the final HF/ethyl alcohol rinse results in more complete hydrogen passivation of Si surface, compared to standard HF-water rinse, by preventing the formation of Si–F species that promote oxide growth upon exposure to air.[10]

The stability of the hydrogen passivated Si(100) surface is well known.[11,12] Before deposition, the passivated surface displayed Si(100) (1×1) surface reconstruction with sharp diffraction spots at 29 V in low energy electron diffraction (LEED) measurements, indicating a well-passivated hydrogen surface characterized by predominately dihydride domains.[13] The dissociation temperature of hydrogen from a passivated silicon surface was verified, in a separate experiment, by a mass spectrometer and reflection high energy electron diffraction (RHEED) measurements. Dissociation, denoted by a sharp increase in the hydrogen peak, occurred between 640 and 670 °C, in agreement with results of RHEED measurements.[14] After reducing to room temperature, *in-situ* LEED measurements showed a sharp Si(100) $(2\times1)(1\times2)$ surface reconstruction at 27 V, confirming the presence of an atomically clean, smooth surface.

Si wafers with hydrogen-passivated surfaces were introduced into an e-gun evaporator without any additional processing and hafnium dioxide pellets with ~1%–2% zirconium were evaporated from a carbon crucible. All samples were deposited with an O_2 partial pressure of 5×10^{-5} Torr, with the oxygen injector close to the substrate surface. After deposition, thickness was measured using x-ray reflectivity, and then the sample was moved, *ex situ*, to a high-vacuum (10^{-7} Torr) annealing chamber. The samples were annealed at 300 °C for 45 min in an H_2 pressure of 1.5 Torr (H_2 pressure was maintained during temperature ramp up and cool down). Thickness of oxide was then measured again, and titanium dots ($d=64\pm0.3$ μm) were deposited on oxide surface through a shadow mask. Capacitance–voltage ($C-V$) profiles were measured at the frequencies from 10 kHz to 1 MHz.

The as-deposited films exhibited large counterclockwise hysteresis, >300 mV at flatband (not shown). Since our process is intrinsically very clean, as indicated by low voltage LEED measurements of the Si(100) surface, the presence of the usual mobile charges such as sodium and lithium is not expected to contribute to the hysteresis. Thus, trapped charges at defect sites are directly associated with the hysteresis for the unannealed films.[15] Figure 1 shows the $I-V$ data for the two samples. The decrease in leakage current is drastic, changing from 1.3 A/cm^2 in as-deposited sample to 1 mA/cm^2 in annealed sample, at flatband. Thus charge injec-

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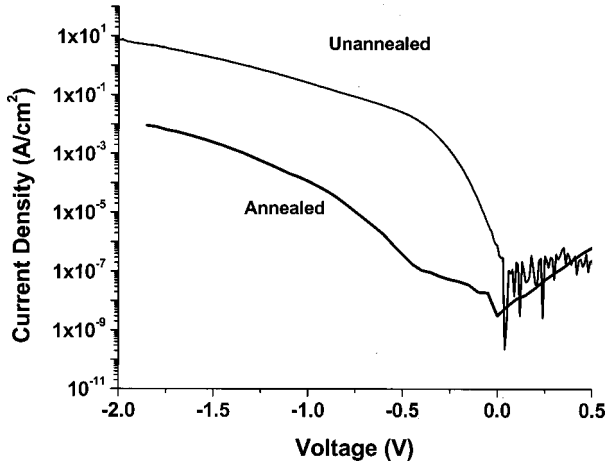

FIG. 1. Current density of annealed and unannealed 5 nm HfO_2 film.

tion, resulting in large leakage current, is the main contributor to hysteresis for the as-deposited samples. The hysteresis was greatly reduced in annealed samples to as little as 20 mV at $V_{FB}=-1.33$ V. Upon annealing, sites that harbor trapped charges are apparently passivated, reducing the leakage current.

Figure 2(a) shows the $C-V$ curves of the annealed 5.0 nm sample at 40 kHz, 100 kHz, and 1 MHz in the forward (-2 to 0 V) direction. The frequency dispersion is significant for unannealed hafnium dioxide. In fact, due to the leakage current described earlier, low frequency data was not acceptable for analysis, and thus the data is not presented. Figure 2(b) shows the hysteresis of both the annealed and unannealed 32 nm sample prepared to reduce the leakage effects. In this thick sample, the unannealed $C-V$ curves have significant frequency dispersion throughout depletion, arising from interface defects. The variations in majority carrier capture and emission at these interface states with the small signal changes ($\sim$4 mV) results in frequency dispersion, most notably in the depletion region. The presence of frequency dispersion in the as-deposited sample suggests that the initial hydrogen passivated surface has been dissociated during deposition since frequency dependant interface states are related to interfacial defects of silicon.

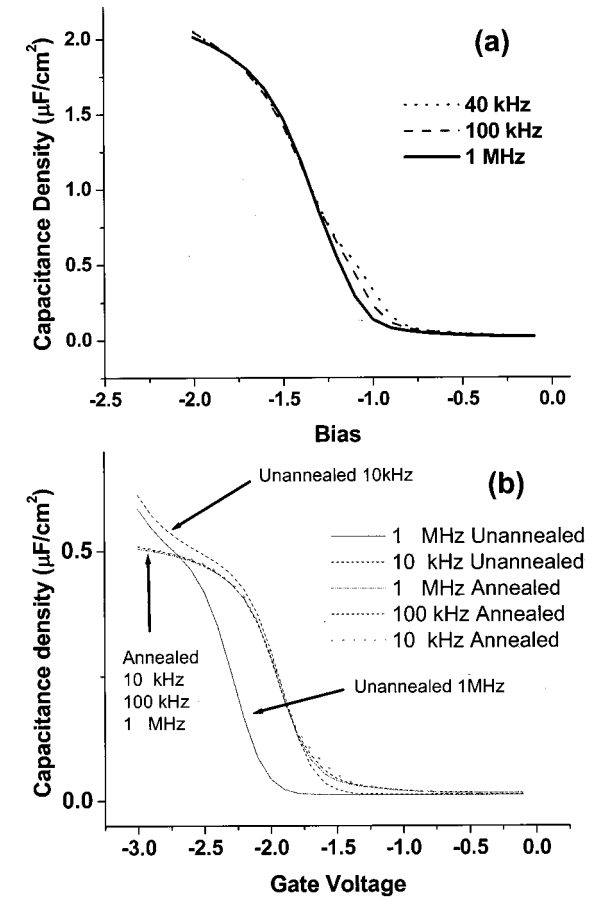

FIG. 2. Frequency dispersion of (a) the annealed 5 nm HfO_2 film and (b) the annealed and unannealed 32 nm HfO_2 film.

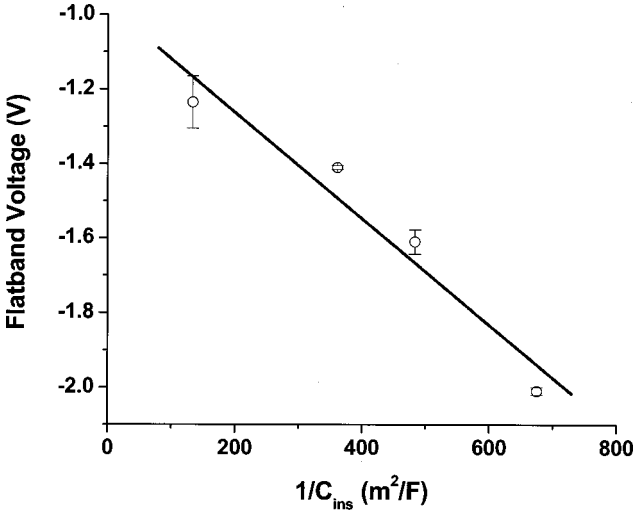

FIG. 3. Flatband voltage as a function of inverse insulator capacitance density for annealed HfO_2. Error bars are computed from the error in the least squares fit of the $C-V$ curve to the theoretical $C-V$ curve with quantum mechanical correction.

Hydrogen annealing is known to passivate interface states in SiO_2.[16] This appears to be the case in HfO_2 as well, as indicated by reduced frequency dispersion. Dispersion was 0.0125%/decade for the 32 nm sample, and 0.04%/decade for the 5.0 nm sample, much less than the recognized requirement of 1%/decade.[17] The separation of the curves with frequency at weak inversion in the 5.0 nm annealed sample is noted, and is believed to be due to silicon traps that contribute to band bending. Barring the increase in capacitance due to leakage, the unannealed and annealed films show similar total capacitance at accumulation, further indication that there is little change in the dielectric constant upon annealing.

Hydrogen anneal of silicon dioxide is reported to increase the positive fixed charge density.[18] However, as can be seen for the 10 kHz $C-V$ curves for the 32 nm sample, there is no shift in the flatband voltage after annealing, and thus no increase in the fixed charge. For several samples with lower thicknesses, the flatband voltage is slightly shifted towards zero, suggesting a small reduction in oxide fixed charges. Figure 3 shows the flatband voltage as a function of the inverse capacitance for the thinner hydrogen annealed samples. The fit to the data can be described by the equation[19]

$$V_{FB}=\phi_{ms}\pm\frac{Q_f}{C_{ins}}, \quad (1)$$

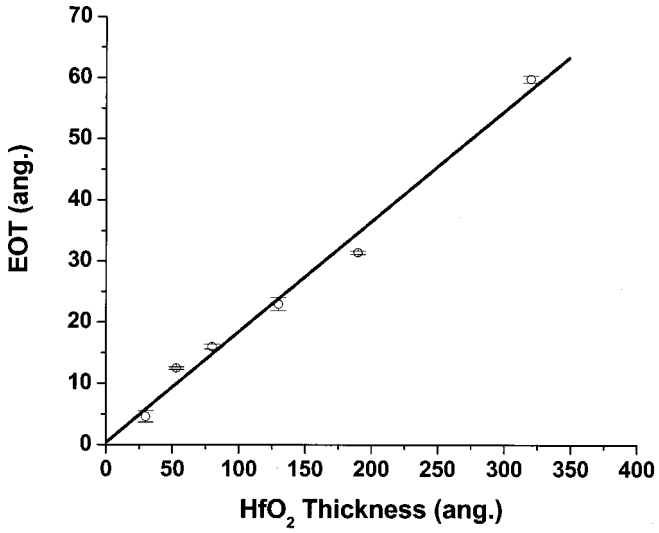

FIG. 4. Equivalent oxide thickness as a function of hafnium dioxide thickness in angstroms for annealed HfO_2. Error was computed as in Fig. 3.

where ϕ_{ms} is the metal-semiconductor work function difference, and Q_f and C_{ins} are the charge density and capacitance density, respectively. From the fit of the annealed sample data of Fig. 3, the value of ϕ_{ms} is -0.98 ± 0.1 eV, while the slope reveals a fixed charge density of $\sim10^{12}$ cm^{-2}. The extrapolated value of ϕ_{ms} is slightly higher in magnitude than the theoretical value of -0.62 eV, and has been explained by Hickmott,[20] and later Houssa,[19] as due to a dipole layer that forms at the metal–insulator interface.

Several groups have reported on the post-deposition annealing of HfO_2 sputtered in oxygen. Anneals were done either in oxygen or in inert gas. This produces low interface state density, but drastically decreases the gate stack dielectric constant. Annealing in hydrogen gas at reduced temperatures reduces formation of the interfacial oxide with the added benefit of interface and bulk passivation. Terman analysis[21,22] yields an interface density of states, D_{it}, of 6.0×10^{11} cm^{-2} eV^{-1} for the annealed 32 nm sample, reduced from a value of 6.5×10^{12} cm^{-2} eV^{-1} for the unannealed sample. Detailed analysis of conductance and capacitance measurements will be presented elsewhere.[23]

Using quantum mechanical correction[24] for leakage in the thinner samples, the equivalent oxide thickness (EOT) for the annealed samples was calculated, as seen in Fig. 4. The linearity in EOT versus T_{HfO_2} shows the independence of the process sequence on film thickness. A gate stack dielectric constant of 18 is found for the samples in this study. From the slope of the linear fit to the data, the dielectric constant of the bulk dielectric was found to be 21.5 ± 0.5. Furthermore, the *y-axis* intercept value, associated with the thickness of an interface layer, is 0.04 nm. While this number is not expected to be a direct measure of the interface oxide, it is sufficiently low that it suggests minimal interface layer formation. Given the low temperature of our process, formation of interfacial hafnium silicate is not likely. Direct calculation of an interface of silicon dioxide that results in a gate stack dielectric change from 21.5 to 18 for the 5.0 nm sample indicates an interface thickness of ~0.05 nm. We thus conclude that the interface is formed at the onset of e-beam deposition, and the low temperature hydrogen annealing does not affect the interface thickness. The annealing only passivates interface states. The interface is self-limiting and its thickness is reproducible, independent of hafnium dioxide thickness. The most notable data points are the EOT values of 1.2 and 0.5 nm obtained for the 5.0 and 3.0 nm samples, respectively. To our knowledge, 0.5 nm is the lowest EOT reported for HfO_2 in contact with silicon. Furthermore, leakage current of 0.14 A/cm^2 at -1 V compares favorably with the simulated value of $>10^4$ A/cm^2 for an actual 0.5 nm SiO_2 MOS structure.[25]

In conclusion, the combination of hydrogen surface passivation of silicon via modified Shiraki clean, hafnium dioxide deposition using reactive e-beam evaporation, and low temperature hydrogen annealing produced MIS structures with low frequency dispersion and hysteresis at flatband. EOT was reduced to as low as 0.5 nm. Linear fit to the EOT data indicated the dielectric constant of the HfO_2 film of ~21, but formation of an interfacial oxide reduces the gate stack dielectric constant to 18.

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