A HIGH-RESOLUTION CHARGE-REDISTRIBUTION ANALOG-TO-DIGITAL CONVERTER

by

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CHAPTER I

INTRODUCTION

Natural parameters such as current, voltage, pressure, displacement and time appear in analog form. However, it has been difficult to handle information purely in its natural state. A lot of times, it is necessary to convert the data from analog to digital form so that they can be handled effectively. Digital signal processing offers the advantages of both speed and accuracy. In fact, with the rapid development and the increasing complexity of integrated circuits, many digital circuits are now available to replace functions traditionally performed by analog circuits. Therefore, analog-to-digital (A/D) converters play an important role in this digital era. When necessary, the digital data can be easily converted back to their analog form by digital-to-analog (D/A) converters.

The function of an A/D converter is to convert any analog quantity into a digital word. The output of an A/D converter can be in either serial or parallel format. In the serial format, the digital data are delivered to the output 1 bit at a time, starting with the most significant bit (MSB). In the parallel format, the digital output is presented as a binary word available from N parallel

terminals, each corresponding to 1 bit of the output digital word. In most of the applications, parallel output is preferred over serial output for speed and efficiency of data handling.

The ideal transfer function of an A/D converter is shown in Figure 1.1, where for illustrative purposes, a simple 3-bit converter is assumed. From the figure, it can be seen that the transfer function is discontinuous. In fact, the output is a "quantized" version of the continuously variable analog input. As a result, each output code corresponds to a small range ΔV_o of analog input values. An N-bit A/D converter has 2^N output states and the smallest quantizing step, ΔV_o, corresponds to 1 least significant bit (LSB). In an ideal A/D converter transfer characteristic, the code center point is located at the analog level ideally corresponding to that particular code. Consequently, the code transitions should take place ±1 LSB away from this center point.

A wide range of circuit techniques are known for A/D conversion. However, most of the A/D converters fall into one of the following categories {1}:

1. Integrating A/D converters;
2. Digital-ramp, or servo, A/D converters;
3. Successive-approximation A/D converters;

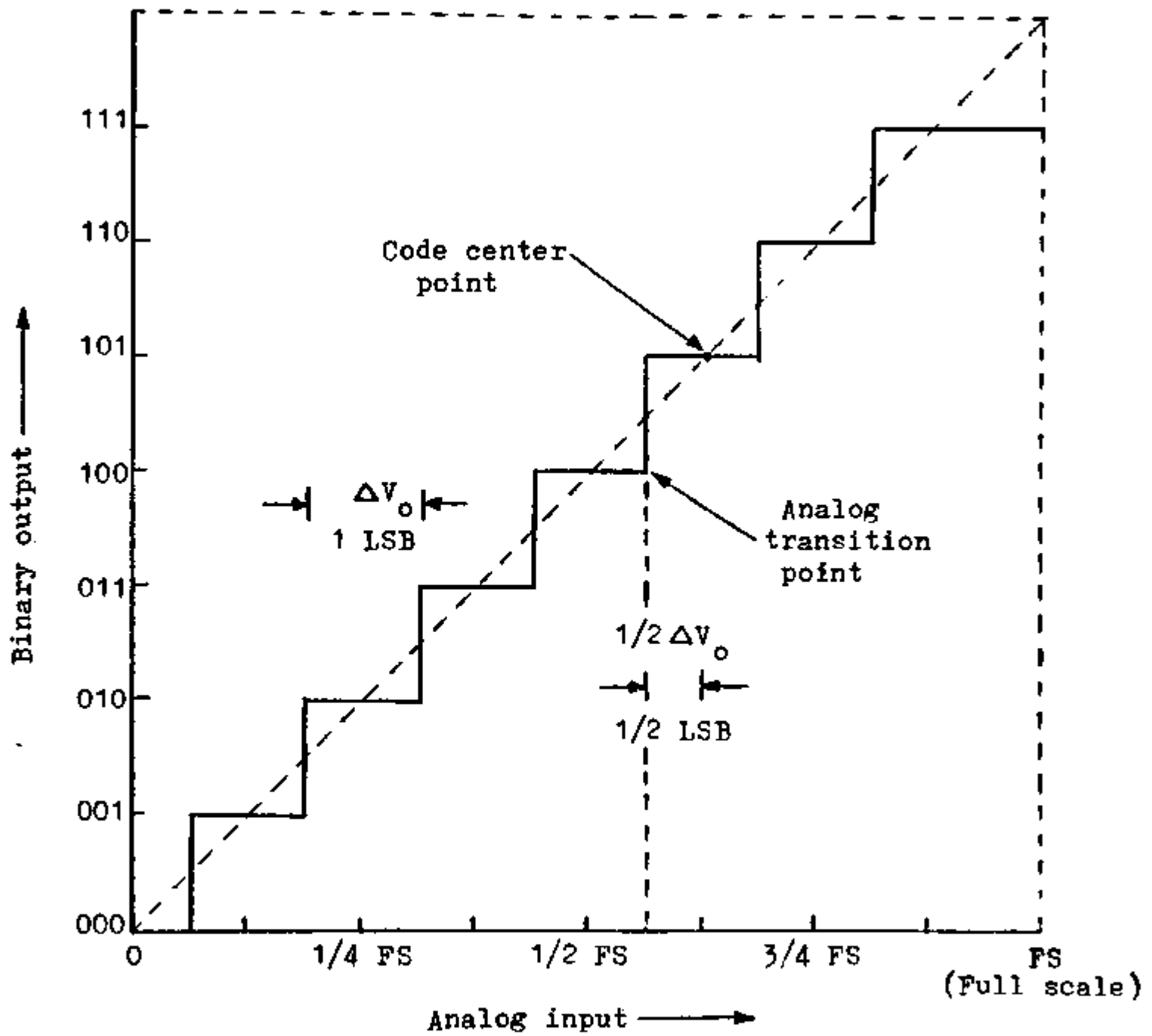


Figure 1.1: Ideal transfer characteristics of 3-bit A/D converter.

4. Parallel, or flash, A/D converters.

Each of these classes of A/D converters will be examined separately in the following sections, with emphasis on their basic principles of operation. In addition, the MOS technology will be studied.

In Chapter II, a number of MOS successive-approximation A/D converters will be reviewed. It will be seen that the conversion speed of the charge-redistribution A/D converter will be limited at high bit counts. This is due to the fact that the area and capacitance of the binary-weighted capacitor array increase rapidly as the number of bits is increased.

The objective of this thesis is to solve the above problem by proposing an R-2R charge-redistribution A/D converter (Chapter III). With technology comparable to that of the regular charge-redistribution converter, this converter should be able to achieve a higher conversion speed. It will also be shown in Chapter IV that this converter can be combined with a self-calibration technique to improve its resolution. At the same time, the performance of the self-calibration technique is enhanced.

Integrating A/D Converters

In integrating A/D converters, the conversion is performed in an indirect manner. First, the analog input is converted to a timing pulse with its duration proportional to the analog voltage V_A. The duration of this pulse is then measured digitally by counting the number of cycles of the clock signal between the beginning and the end of the pulse.

A simple integrating A/D converter is shown in Figure 1.2. Initially, the counter is set to zero and the switch S_1 is closed. Then the conversion cycle begins with the switch S_1 open. While the current source I_1 generates a linearly rising ramp voltage across the integrating capacitor C_1, the counter starts counting the input clock cycles. The comparator changes state, stops the counter, and ends the conversion cycle when the linear ramp reaches the level of the analog input V_A. The final count in the counter is then the digital equivalent of the analog signal V_A.

This simple converter illustrates only the basic principle of operation. In reality, more complex circuit techniques are used.

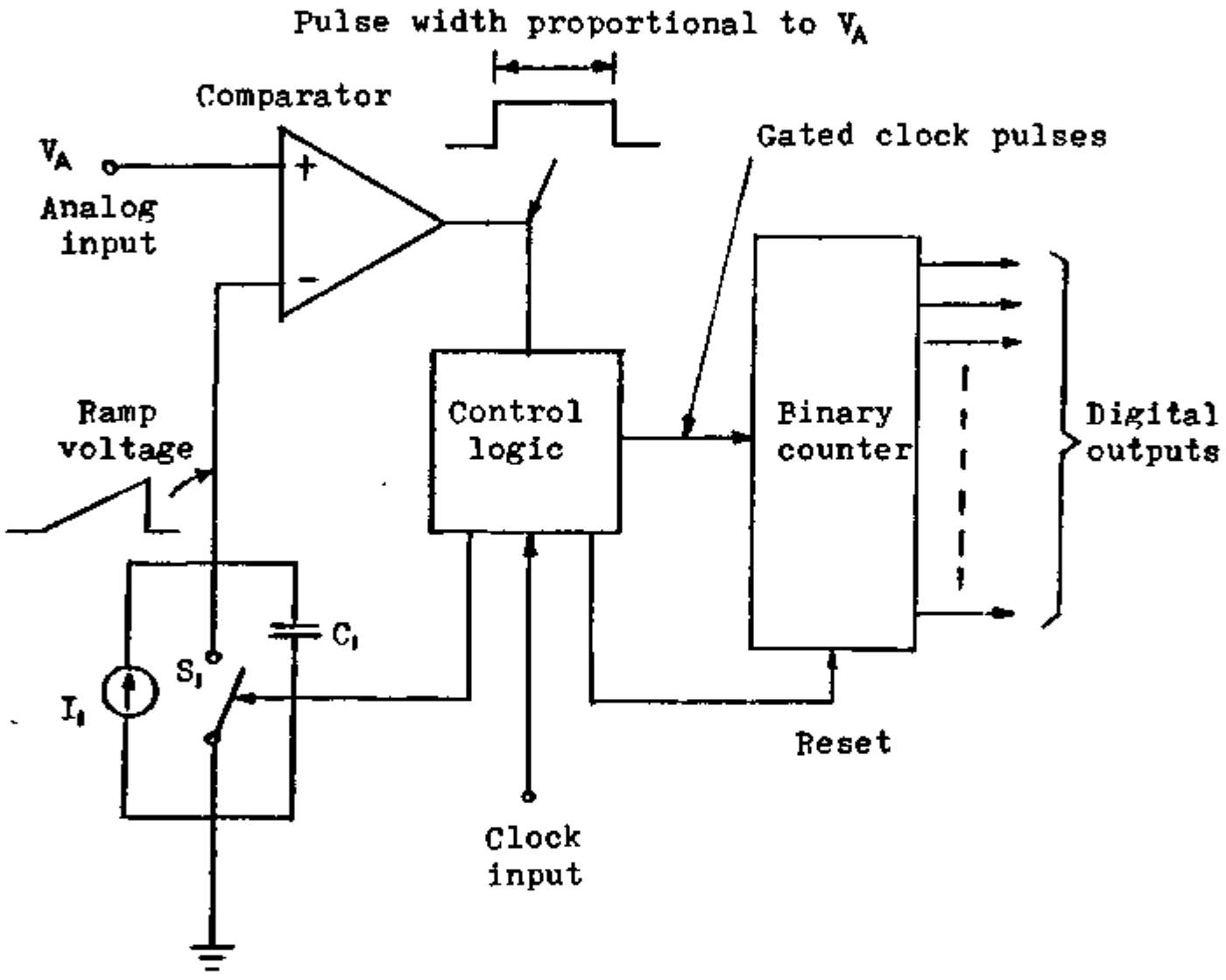


Figure 1.2: Block diagram of simple integrating A/D converter.

Digital-Ramp A/D Converters

In digital-ramp A/D converters, a combination of a binary counter and a D/A converter is used to generate a digital ramp or staircase output. This output is compared to the level of the analog input signal to give the corresponding digital code.

To illustrate the basic operations, the functional block diagram of a digital-ramp A/D converter is shown in Figure 1.3. At the beginning of the initial conversion cycle, the system counts the clock pulses. The corresponding binary count is converted to a staircase output by the D/A converter. This analog level V_o is continuously compared to the analog input level. As it reaches the analog input level V_A, the comparator changes state and stops the count. The counter output code then gives the corresponding digital word.

Successive-Approximation A/D Converters

The successive-approximation converter employs a trial-and-error technique to approximate an analog input with a corresponding digital code. As shown in the diagram of Figure 1.4, it consists of a successive-approximation register (SAR) and a D/A converter in feedback around a

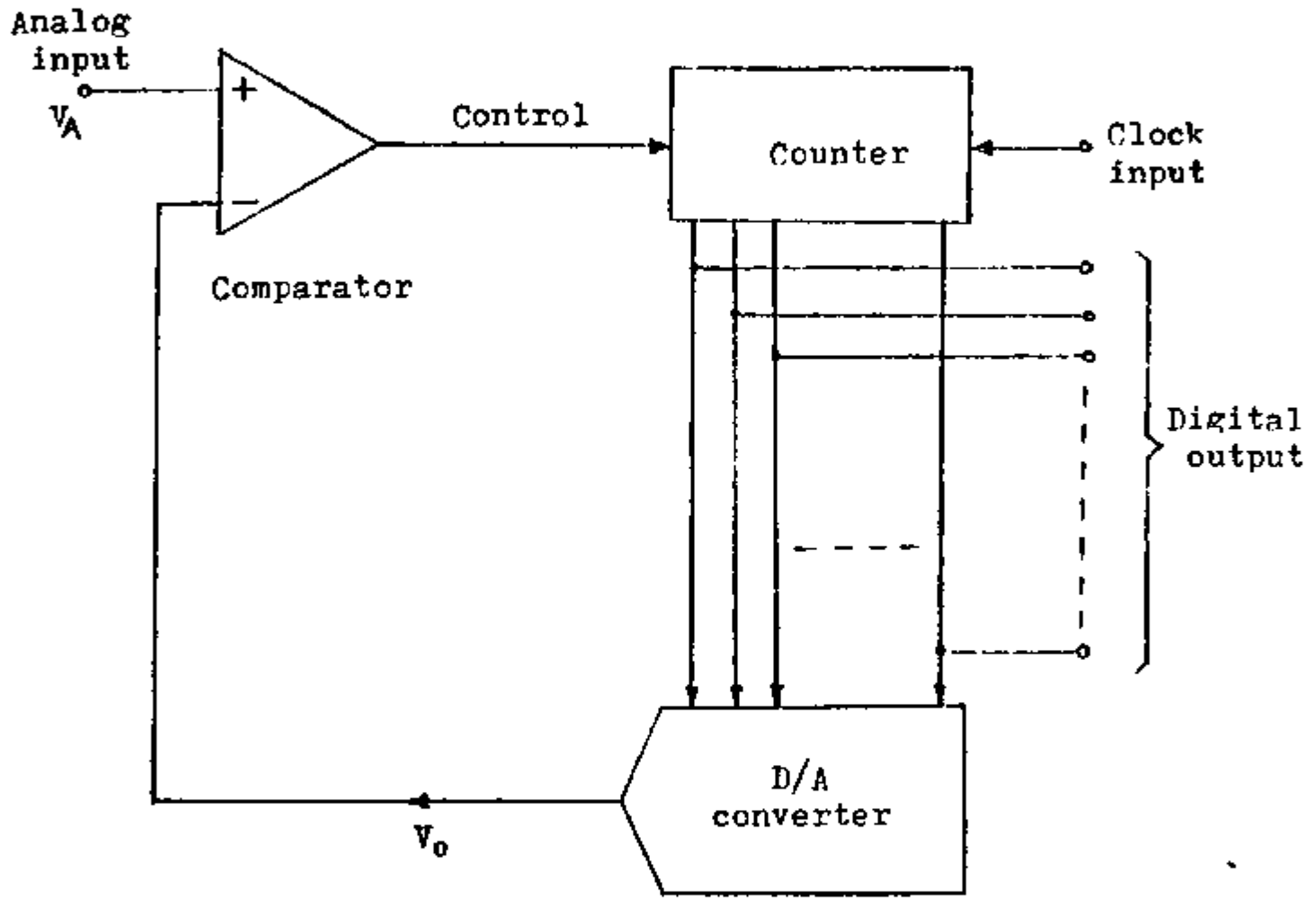


Figure 1.3: Functional block diagram of digital-ramp A/D converter.

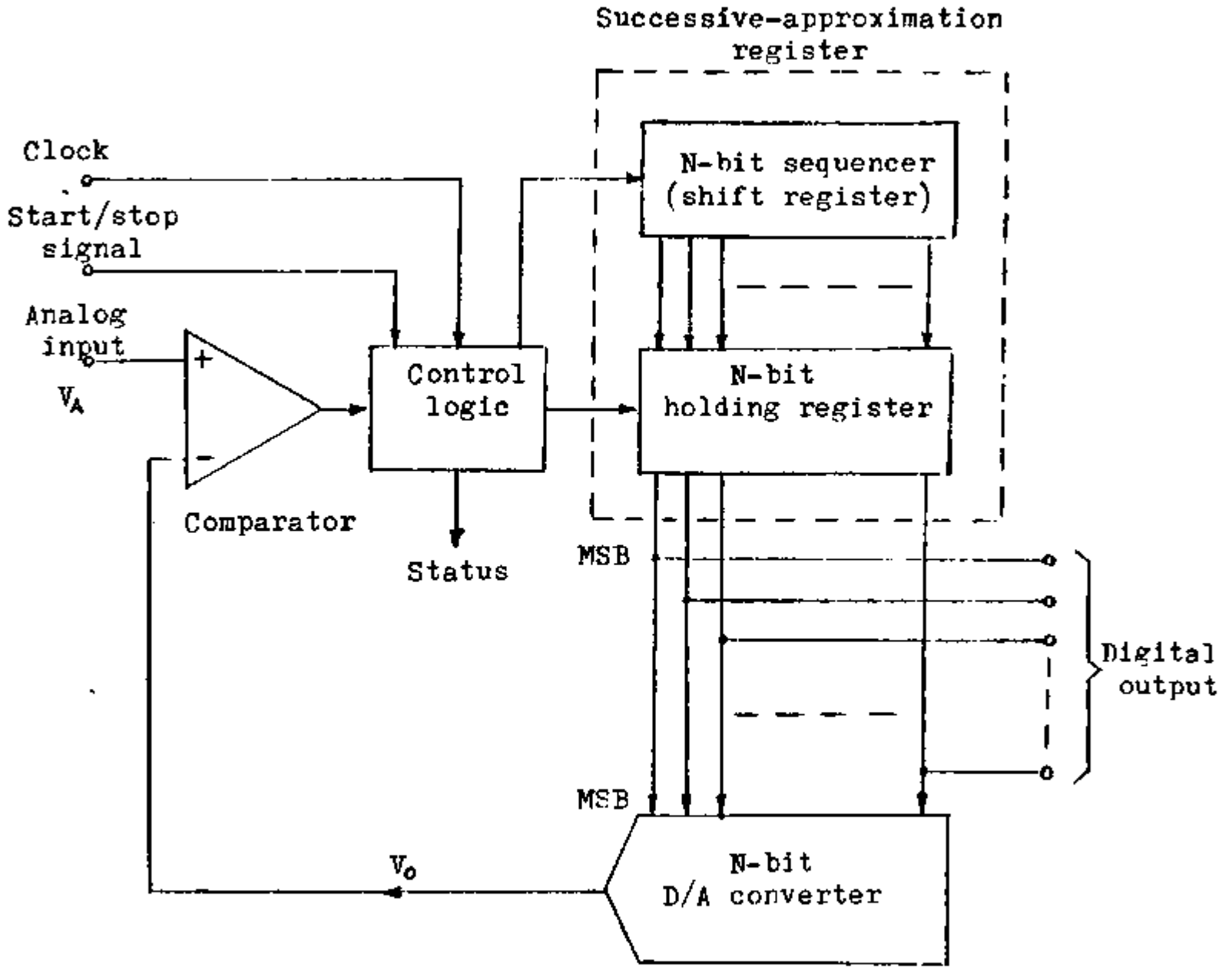


Figure 1.4: Functional block diagram of successive-approximation A/D converter.

voltage comparator. After the SAR has been cleared, the conversion process starts with a '1' inserted as a trial bit for the MSB in the holding register, while the rest of the bits remain at '0'. If the analog output V_0 of the D/A converter is smaller than V_A, the output state of the comparator remains unchanged, and the '1' is retained for the MSB. Otherwise, it is replaced by a '0'. In the next cycle, a '1' is tried for the next most significant bit. If the comparator output does not change state, it is retained. Otherwise, it is replaced by a '0'. This process continues until all bits are obtained in N successive cycles.

The operation process is depicted graphically {2} in Figure 1.5. It can be seen that an N-bit converter requires only N successive-approximation steps, or equivalently, N clock cycles. This is much faster than the integrating or the digital-ramp converters, which take up to 2^N clock cycles to complete a conversion.

Parallel A/D Converters

The parallel A/D converter uses a separate analog comparator with a fixed reference for every quantization level from zero to full scale in the digital word. The outputs of these comparators are then encoded to give a parallel digital output.

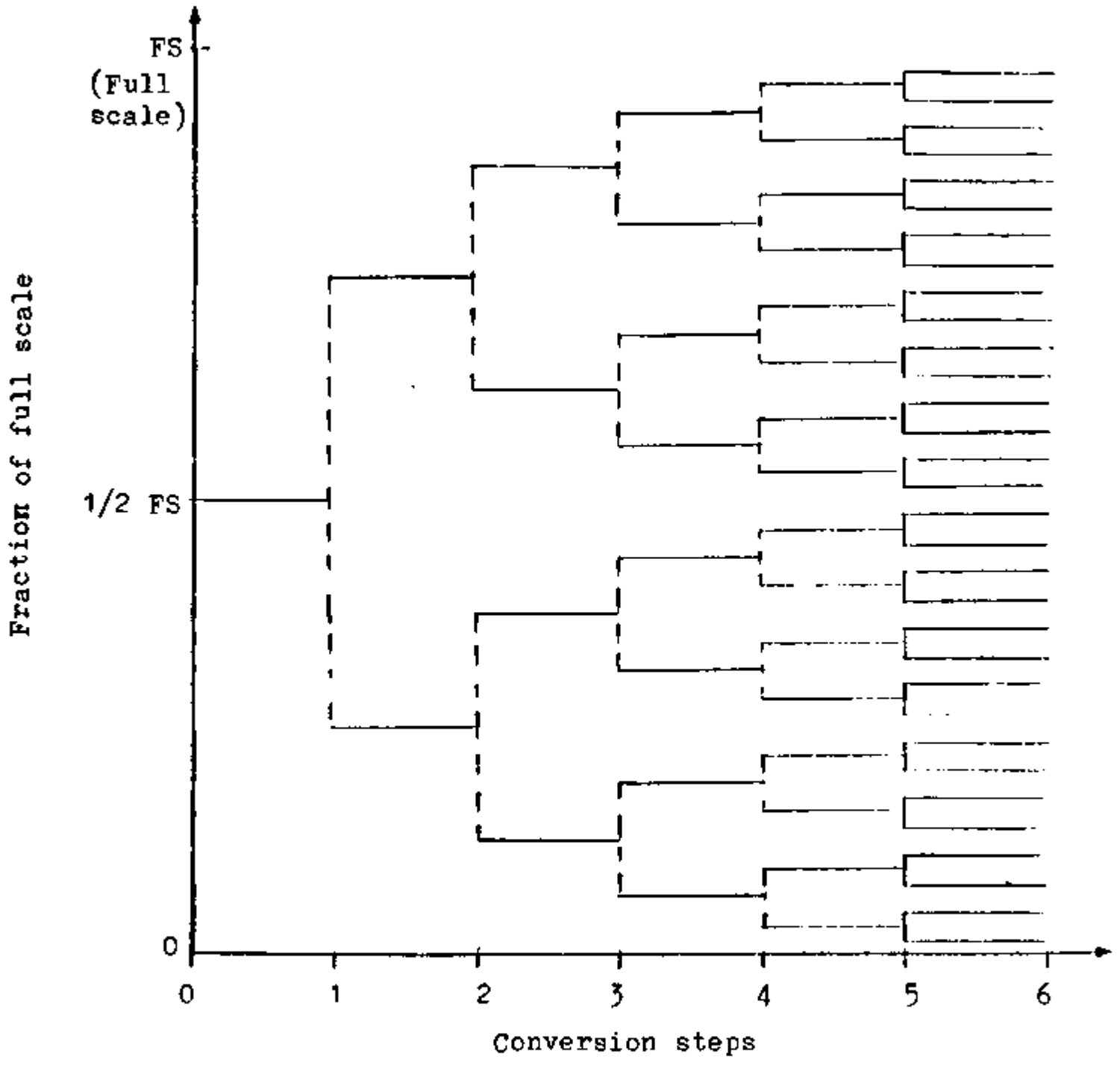


Figure 1.5: Operation of successive-approximation A/D converter.

A block diagram of a parallel A/D converter is shown in Figure 1.6. For an N-bit converter, 2^N-1 separate comparators and reference levels are needed. As a result, the system complexity increases very quickly when the number of bits is increased. However, since all input bits are processed simultaneously, the entire encoding operation can be performed very rapidly, say, within one clock cycle. This makes the parallel A/D converter the fastest type among all the converters.

MOS Technology

In the past, the integrated circuit technology for the realization of A/D converters has been bipolar due to its better analog performance. On the other hand, metal-oxide-semiconductor (MOS) technology was primarily developed for digital large-scale integration (LSI) design. The small size and the self-isolating property of the MOS transistor result in high circuit density. To take advantage of both technologies, hybrid integrated circuits have been used to build A/D converters. However, as higher levels of integration are called for, it becomes neccessary to combine substantial amount of digital circuits with the analog circuitry on the same chip. As a result, the use of MOS technology for monolithic realization becomes more and more attractive.

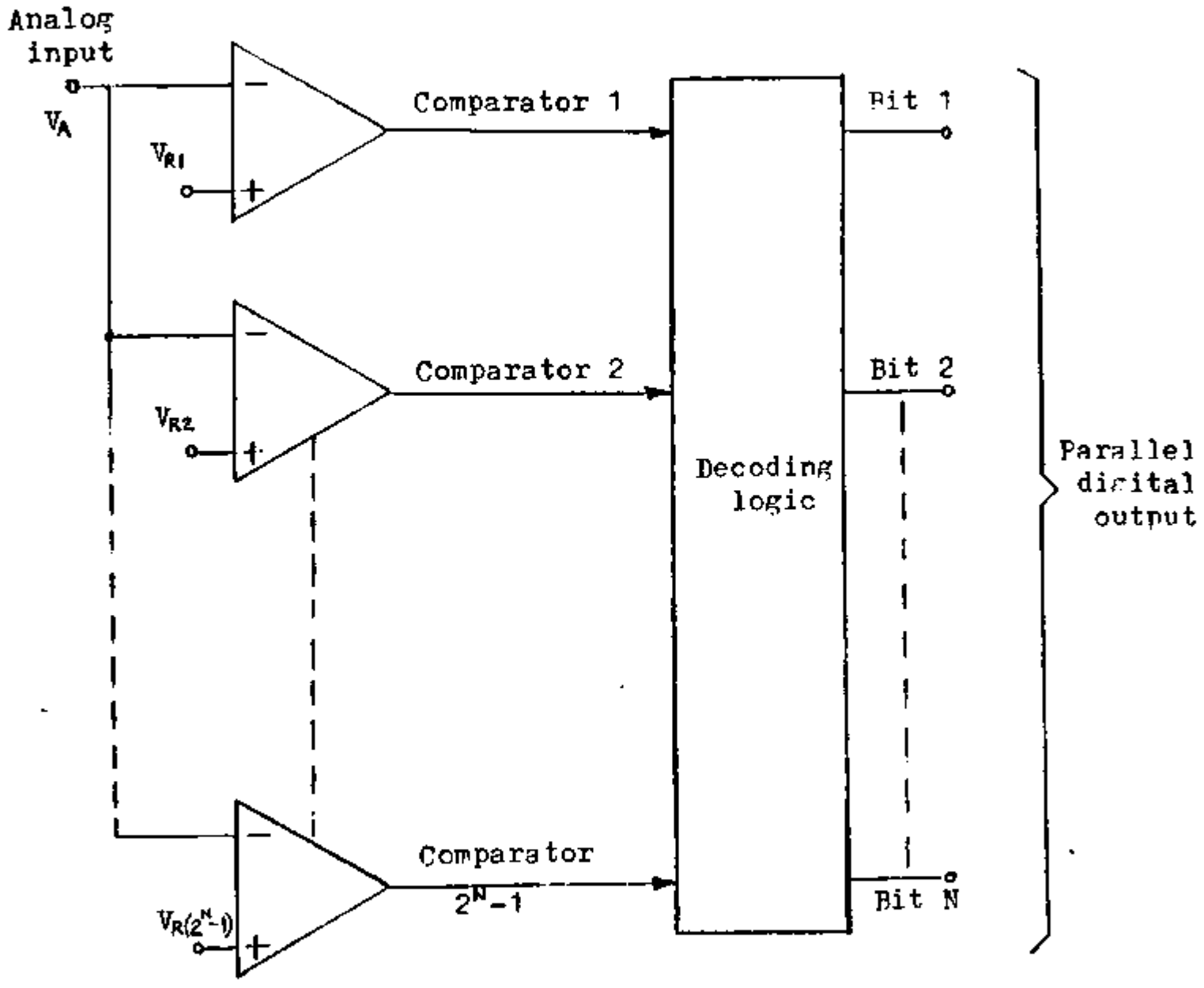


Figure 1.6: Conceptual block diagram of parallel A/D converter.

While the use of MOS transistors makes it possible to integrate analog functions on a much smaller chip area, it presents many design challenges and requires a number of compromises. The major problem is the high offset voltages associated with MOS device pairs. As a consequence, the MOS analog blocks may not be able to meet the performance specifications of their bipolar equivalents. Fortunately, they still perform satisfactorily as a subsystem within the monolithic chip.

On the other hand, the MOS technology does offer other significant advantages over bipolar technology for the realization of analog circuit functions. The most important of these is the capability of storing charge on a circuit node and sensing its voltage nondestructively over many milliseconds {3}. This property results from the essentially infinite input resistance and high off-resistance of the MOS transistor. In addition, capacitors are easily fabricated in metal gate technology. These make the MOS technology ideal for precision analog sampling and holding. In fact, this capability has led to new approaches to many analog functions.

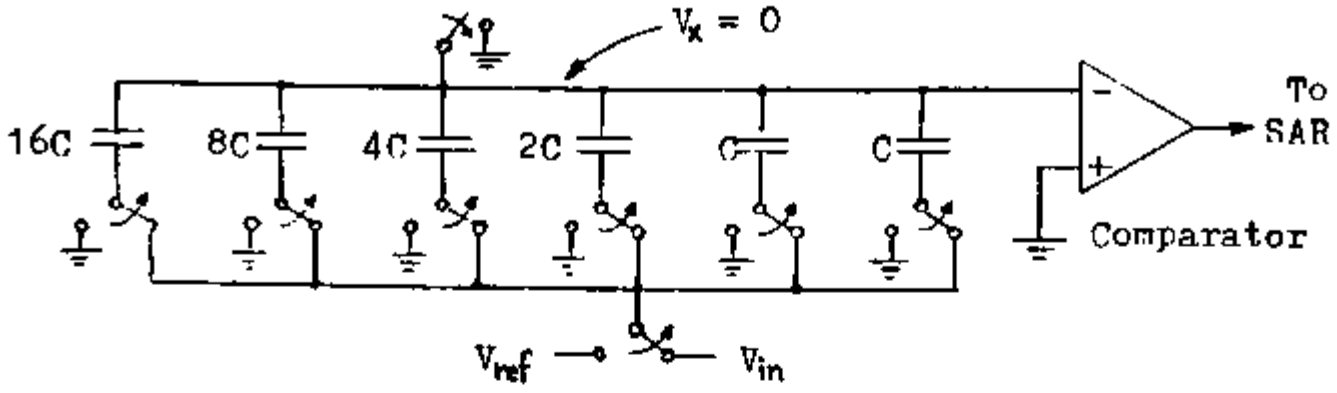
CHAPTER II

MOS SUCCESSIVE-APPROXIMATION A/D CONVERTERS

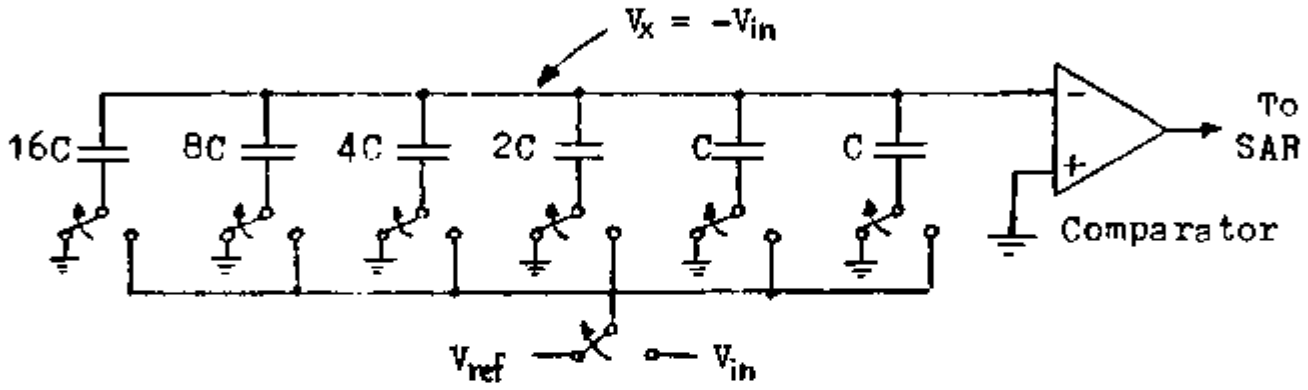
Successive approximation is one of the most commonly used A/D conversion techniques. It offers an excellent compromise between resolution and converter speed requirements. A number of approaches have been developed for designing successsive-approximation converters with MOS technology. This chapter reviews some of the major approaches.

Charge-Redistribution A/D Converters

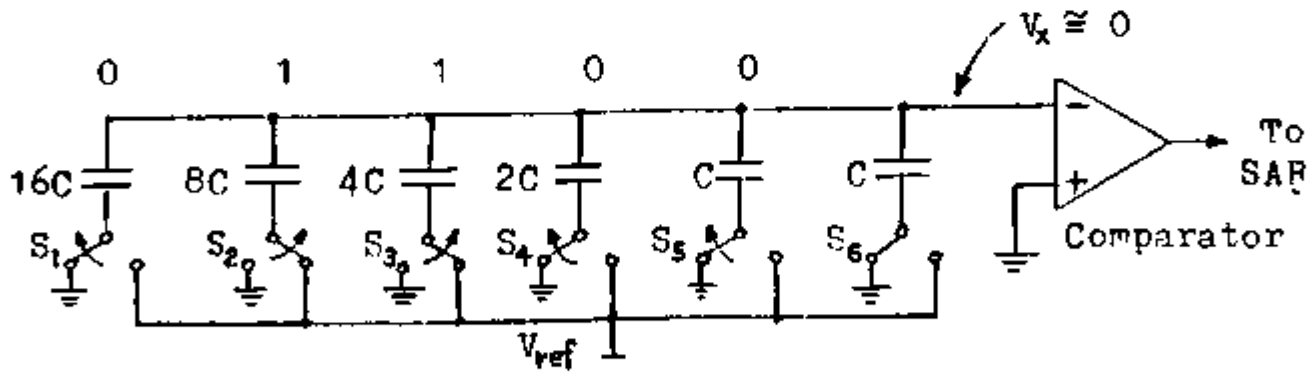
The charge-redistribution A/D converter uses a charge-scaling D/A converter and a SAR in feedback around a voltage comparator to perform the A/D conversion {4}. As shown in Figure 2.1a, the basic binary-weighted capacitive ladder being used contains an additional termination capacitor C, which is equal to the size of the LSB capacitor. The conversion is accomplished in three steps. In the first step, shown as the "sample mode" in Figure 2.1a, the top plate is connected to ground and the bottom plates to the input voltage. As a result, the top plate stores a charge proportional to the input voltage V_{in}. In the second step, called the "hold mode", the top grounding switch is opened,



(a)



(b)



(c)

Figure 2.1: Sequence of steps in operation of 5-bit charge-redistribution A/D converter: (a) Sample mode, (b) hold mode, (c) end of redistribution mode for 01100 code.

and the bottom plates are connected to ground, as shown in Figure 2.1b. Since the charge on the top plate is conserved, its potential becomes $-V_{in}$.

During the last step, called the "redistribution mode", the successive-approximation process begins. First, the switch S_1, corresponding to the MSB, is connected to V_{ref}, with the rest of the switches remain intact at ground. Consequently, the voltage V_x is increased by an amount equal to 1/2 V_{ref}, i.e.,

$$V_x = -V_{in} + 1/2\ V_{ref}.$$

If the comparator output changes state, S_1 is brought back to its original position and a '0' is stored as the MSB. Otherwise, S_1 is left connected to V_{ref} and a '1' is stored instead. Similarly, each of the remaining bits is tried one at a time to determine the digital output code, while the termination capacitor is always connected to ground. A final configuration is illustrated in Figure 2.1c for the digital output 01100. Notice that all the capacitors corresponding to '0' bits are totally discharged, and total original charge on the top plate has been redistributed between capacitors corresponding to '1' bits.

The main source of error in this type of converters is the matching and tracking of the capacitor ratios in the

array. This limits the converters to 10 bits of resolution. Due to very low temperature coefficients of MOS capacitors, the converters exhibit excellent temperature-stability characteristics. Although the conversion speed is somewhat slower than that of comparable bipolar designs, the circuit can be implemented on a much smaller area.

Potentiometric A/D Converters

The potentiometric A/D converter employs a voltage-scaling D/A converter and a SAR in feedback around a voltage comparator {5}. The technique is illustrated with a conceptual 3-bit version of the converter shown in Figure 2.2. The successive-approximation search begins by inserting a trial '1' to the MSB and then examining the state of the comparator output. In a similar manner, this is repeated for each of the lesser significant bits. When a given bit coefficient is '1', the corresponding switch or switches are closed and their complements are opened.

For an N-bit converter, 2^N resistors and approximately 2^{N+1} switches are needed. Consequently, as N is increased, the complexity of the circuit increases rapidly. However, by using MOS technology, the resistor string and the switches can be implemented in a relatively small silicon area. An important advantage of this concept is its

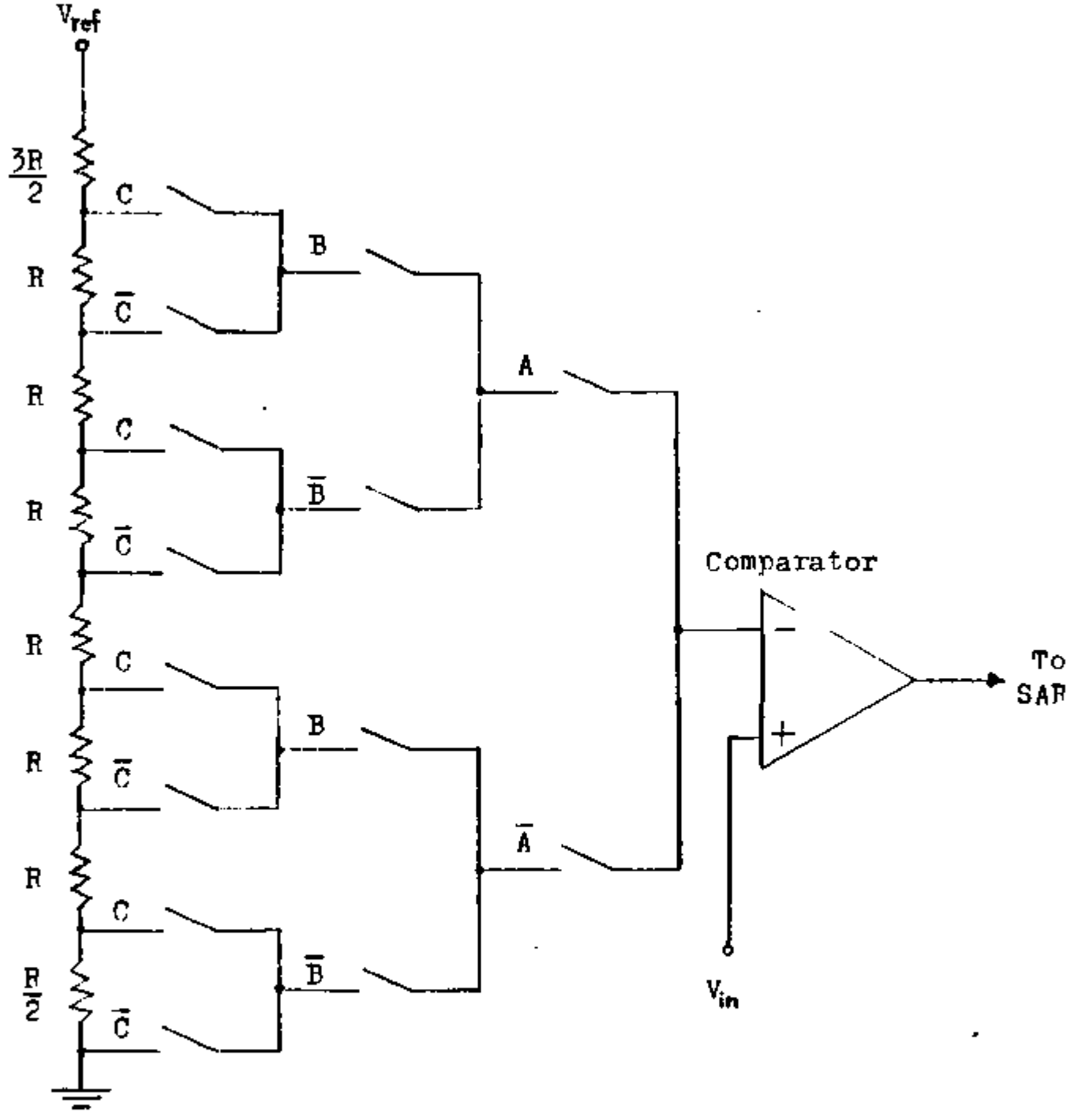


Figure 2.2: Conceptual diagram of 3-bit potentiometric A/D converter.

inherent monotonicity. Since the voltage at any one node of the resistor string is always greater than the voltage at the node below it, the converter will have no missing codes.

Charge-Redistribution Converters with Improved Resolution

In conventional charge-redistribution converters, the available resolution is limited by the component-matching tolerances to approximately 10 bits. Beyond this limit, excessive differential nonlinearity and missing codes would result. This problem can be solved to a certain extent by combining a charge-redistribution converter with a potentiometric resistor array [6]. As shown in Figure 2.3, this converter uses an M-bit resistor array along with a K-bit capacitor array to provide (M+K)-bit resolution.

The conversion starts with the sample and hold modes which are similar to that described earlier in charge-redistribution A/D converters. Then a successive-approximation search is performed among the resistor string taps to determine the segment within which the stored sample lies. After the M most significant bits are given, buses A and B are switched to the ends of the resistor defining this segment. A second successive-approximation search is performed using the capacitor array switches until the comparator input

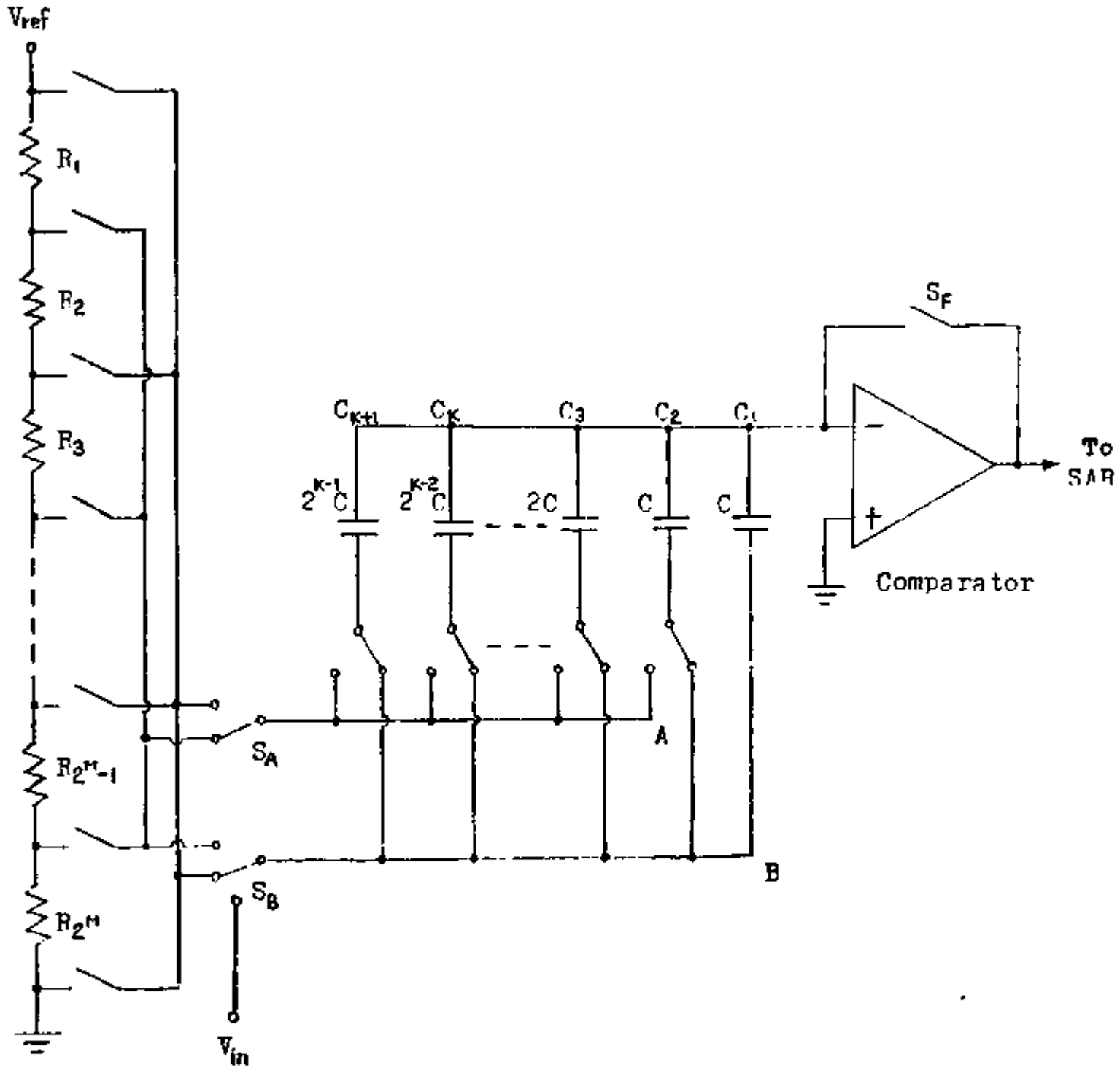


Figure 2.3: Simplified schematic diagram of A/D converter with improved resolution.

voltage converges to zero. This gives the remaining K bits of the conversion.

Since the potentiometric resistor string is inherently monotonic, the capacitor array has to be ratio-accurate to only K bits and still provides (M+N)-bit monotonic conversion. By increasing M, the area and capacitance of the capacitor array can be reduced to provide the same resolution. This in turn increases the conversion speed. However, the fact that the resistor string becomes complex at high bit counts implies that there is a compromise between the values of M and K. Typically, M and K would be chosen to be in the range of 3 to 4 bits and 8 to 10 bits, respectively. While this keeps both the resistor string and the capacitor array configurations relatively simple, 12 to 14 bits of resolution are still achieved.

Charge-Balancing A/D Converters

The problem that the potentiometric converter circuit gets complex at high bit counts can be simplified by using charge-balancing comparator circuits {7}. This is illustrated by the conceptual diagram of a 4-bit A/D converter shown in Figure 2.4. The converter consists of two 2-bit resistor strings. The first two significant bits are decoded from the top ladder while the two lesser bits are

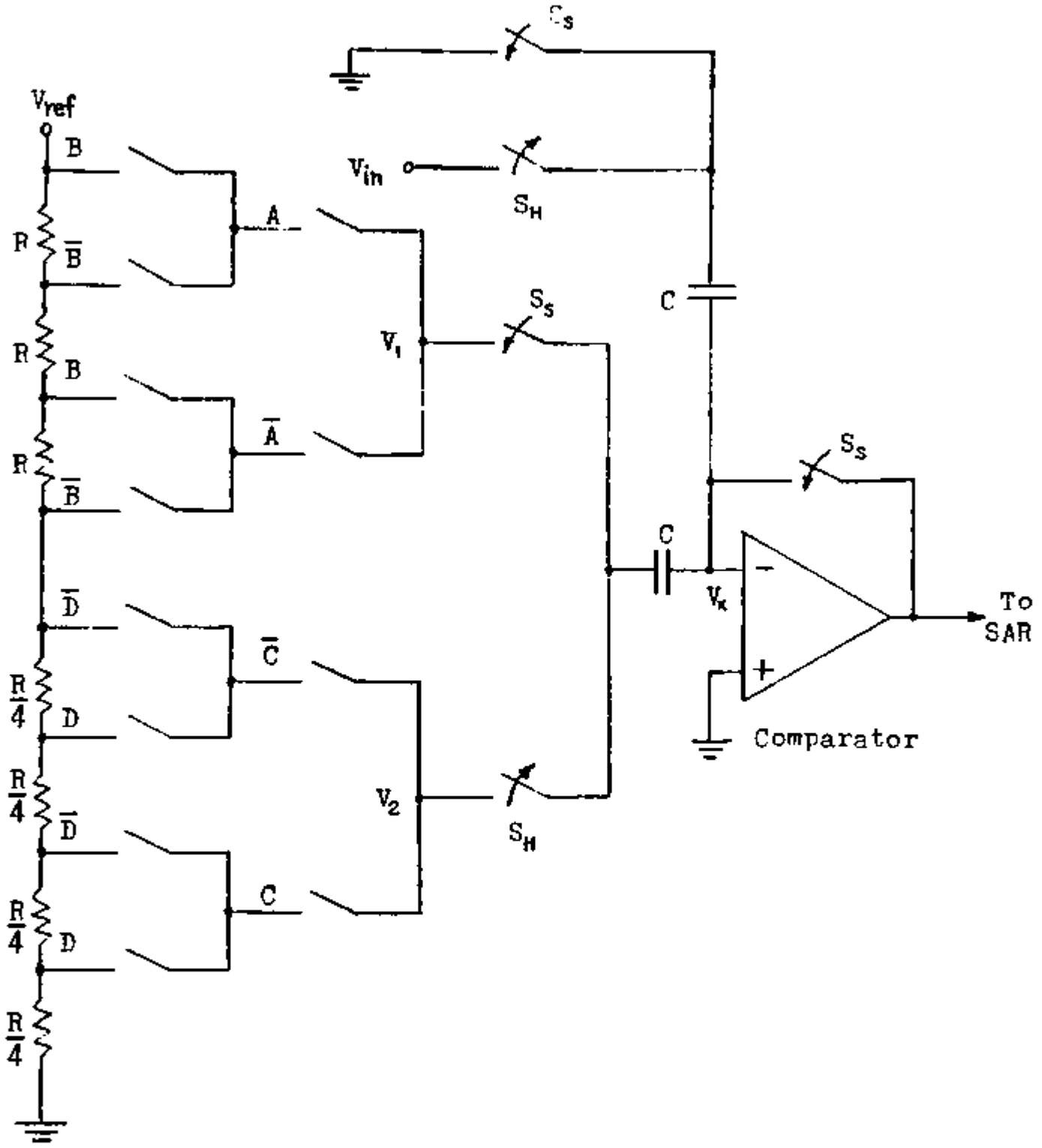


Figure 2.4: Conceptual diagram of 4-bit charge-balancing A/D converter.

decoded from the bottom ladder. Switches S_S and S_H are closed during the sample and hold modes, respectively.

The successive-approximation search is performed during the hold period, when the voltage V_X at the comparator input is given by

$$V_X = 1/2 \{V_{in} - (V_1 - V_2)\}.$$

V_1 and V_2 are the tapped analog voltages associated with the top and bottom halves of the ladder, respectively. By appropriate switching, their difference will give the analog voltages corresponding to different digital codes. For example, with switch A closed, switches B, C, D open, and their complements in the opposite state, the difference of V_1 and V_2 is 1/2 V_{ref}, which is then compared with V_{in}. Thus, the approximation process proceeds in a sample and hold manner until all 4 bits are evaluated.

With charge-balancing technique, resistor ratios and capacitor ratios can be scaled simultaneously. Using these two independent degrees of freedom, one can decode two separate sets of voltage levels from the same resistor string. This method of double-decoding is applied to the 8-bit converter shown in Figure 2.5. The voltage at the comparator input during the hold mode is

$$V_x = V_{in} - \{(V_1 - V_2) + 1/16 (V_3 - V_4) - 1/512 V_{ref}\},$$

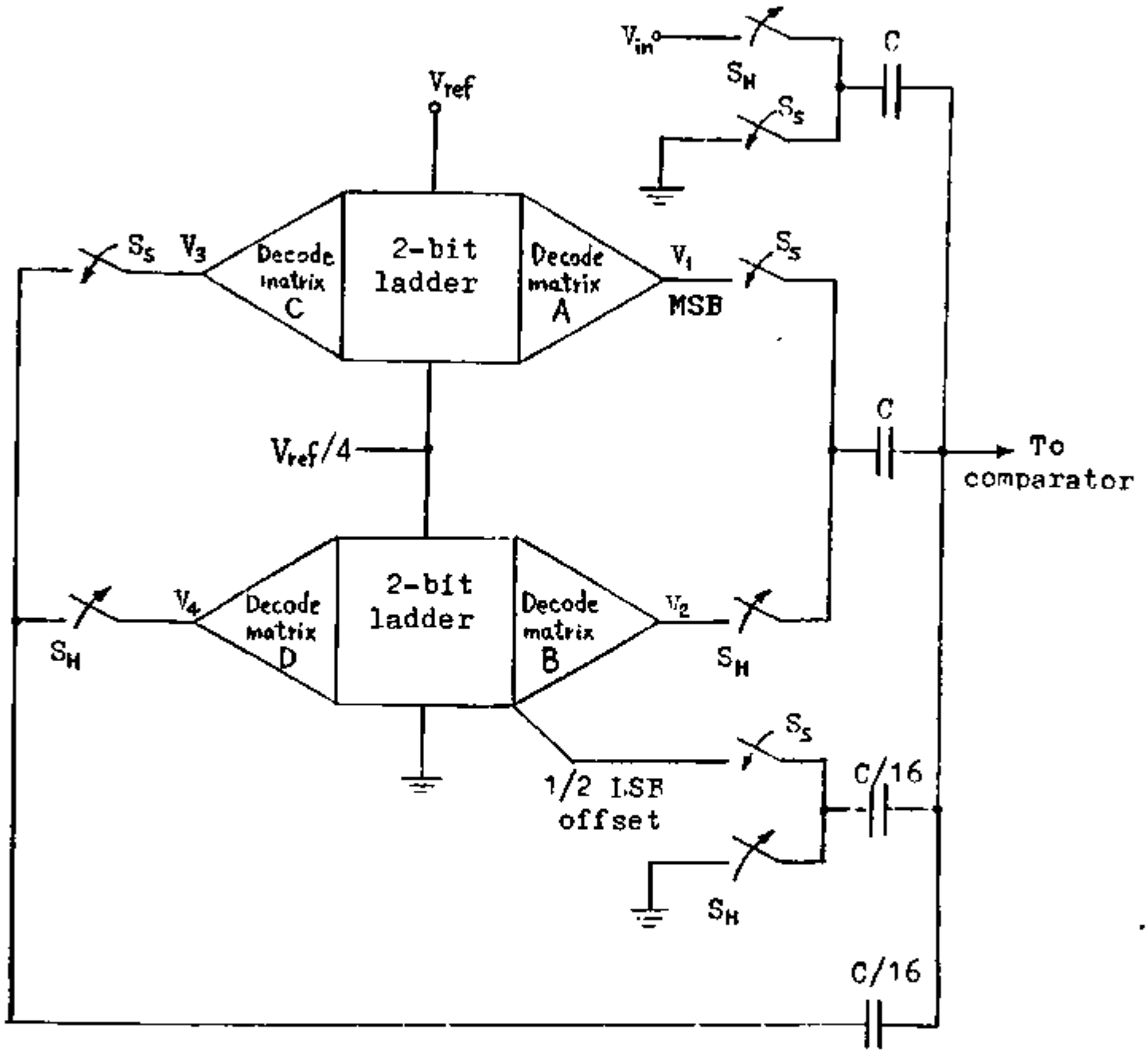


Figure 2.5: Conceptual diagram of 8-bit charge-balancing A/D converter using series connection of 2 double-decoded 2-bit ladders.

where V_1, V_2, V_3, and V_4 are the associated tapped voltages shown in the diagram. An additional tap from the bottom ladder is employed to provide 1/2 LSB offset. Since the converter requires only 16 resistors, 4 capacitors, and 32 switches, it reduces the circuit complexity and silicon chip area substantially as compared to the potentiometric converter.

CHAPTER III

R-2R CHARGE-REDISTRIBUTION A/D CONVERTERS

The advantage of the charge-redistribution A/D converter is its simplicity. Due to the nature of its technique, the converter is well suited for MOS technology. However, the area and capacitance of the binary-weighted capacitor array tend to increase rapidly at high bit counts, which in turn limits the conversion speed. By combining the converter with a potentiometric resistor array, the problem can be partially solved. The charge-balancing A/D converter can also reduce the chip area significantly but requires a series of sample and hold operations. In this chapter, a technique is proposed to solve the problem by combining the charge-redistribution converter with an R-2R resistor ladder.

Charge Redistribution using R-2R Resistor Ladder

A conceptual 4-bit version of an A/D converter is illustrated in Figure 3.1. It consists of a comparator, an R-2R resistor ladder, several unit capacitors and switches. The R-2R resistor ladder divides the reference voltage V_{ref} into 1/2, 1/4, 1/8, and 1/16 of V_{ref}, respectively. The

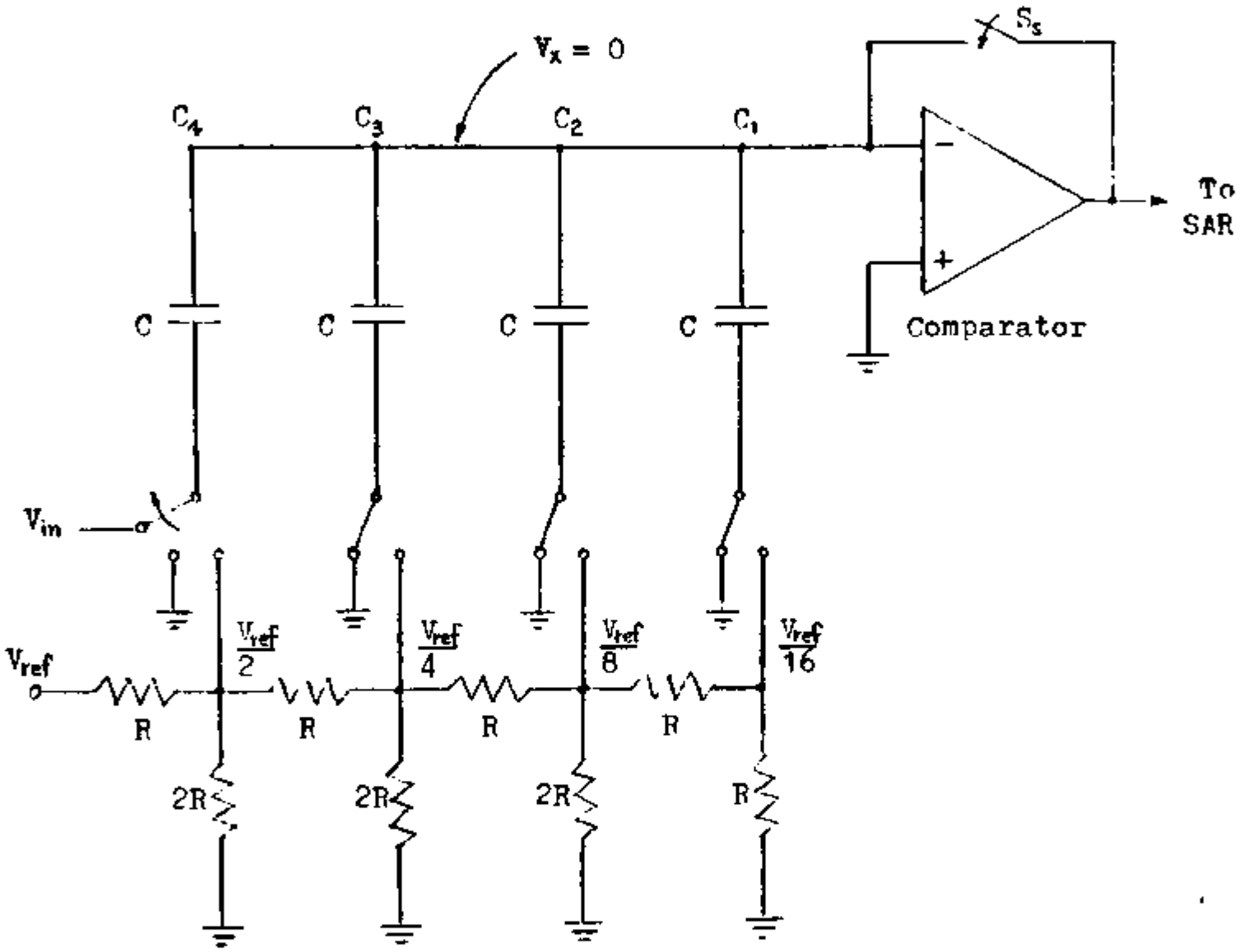


Figure 3.1: Conceptual 4-bit A/D converter illustrating the sample mode operation.

conversion starts with the sample mode (Figure 3.1) when the bottom plate of the capacitor C_4 is switched to the input voltage V_{in}, whereas the bottom plates of the remaining capacitors are connected to ground. With the switch S_S closed, a charge equal to the product of C_4 and $-V_{in}$ is stored on the top plate. In the hold mode shown in Figure 3.2, S_S is opened and all the bottom plates are connected to ground, resulting in a potential of $-1/4\ V_{in}$ at the top plate of the capacitors. The successive-approximation process begins in the redistribution mode of Figure 3.3 when the bottom plate of C_4 is connected to $1/2\ V_{ref}$. As a result, the voltage V_x at the top plate becomes $-1/4\ (V_{in} - 1/2\ V_{ref})$. If the comparator output does not change state, a '1' is stored as the MSB. Otherwise, the bottom plate of C_4 is returned to ground and a '0' is registered. In a similar manner, each of the remaining bits is tried to determine the digital output code.

For an N-bit converter, the hold mode would result in a potential of $-1/N\ V_{in}$ at the top plate of the capacitors, which implies that the comparator sensitivity has to be N times that of the regular charge-redistribution converter. This makes it more difficult to design a comparator at high bit counts. However, the problem can be solved by adding a binary-weighted capacitor array to the converter. As shown

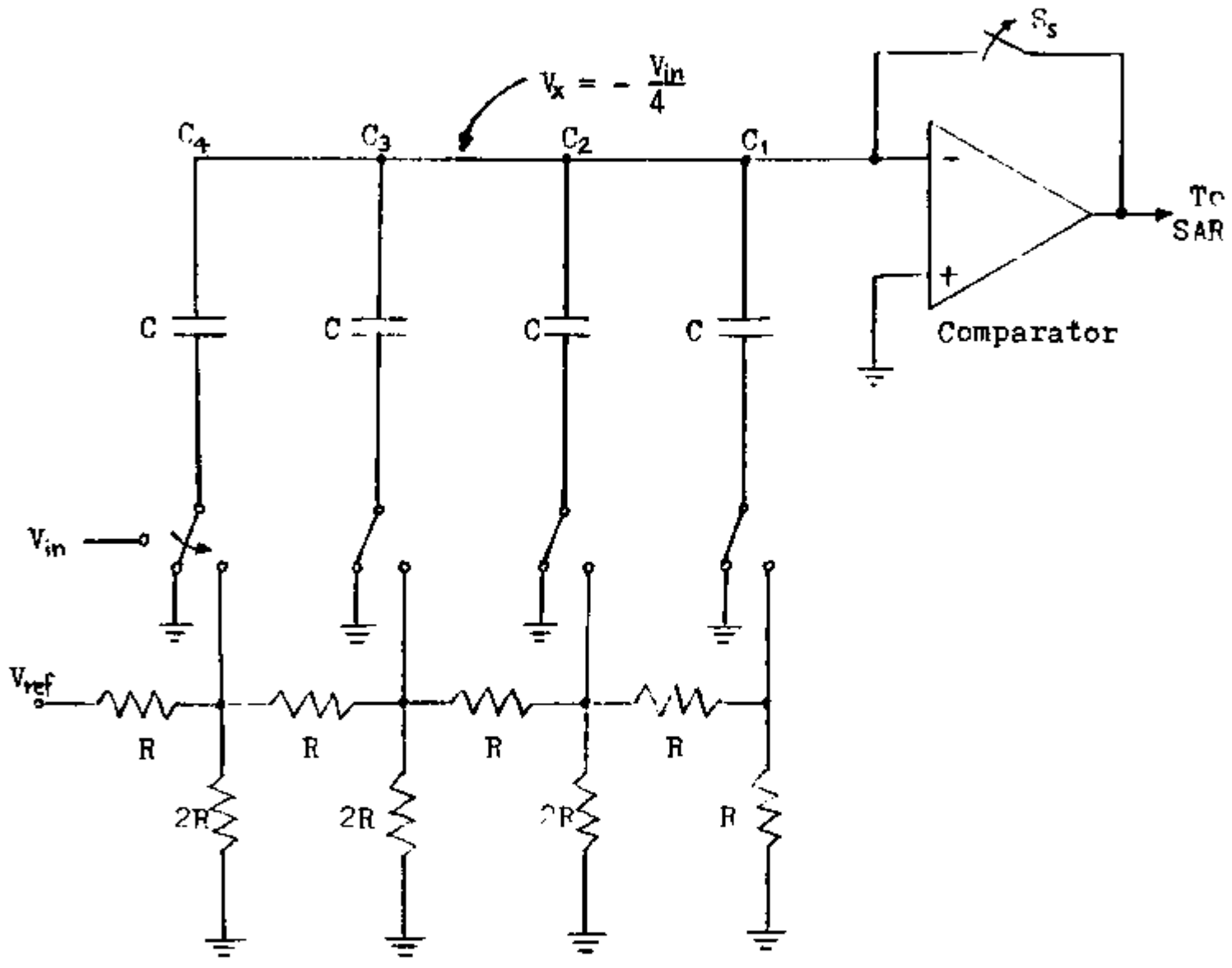


Figure 3.2: Hold mode operation of 4-bit A/D converter.

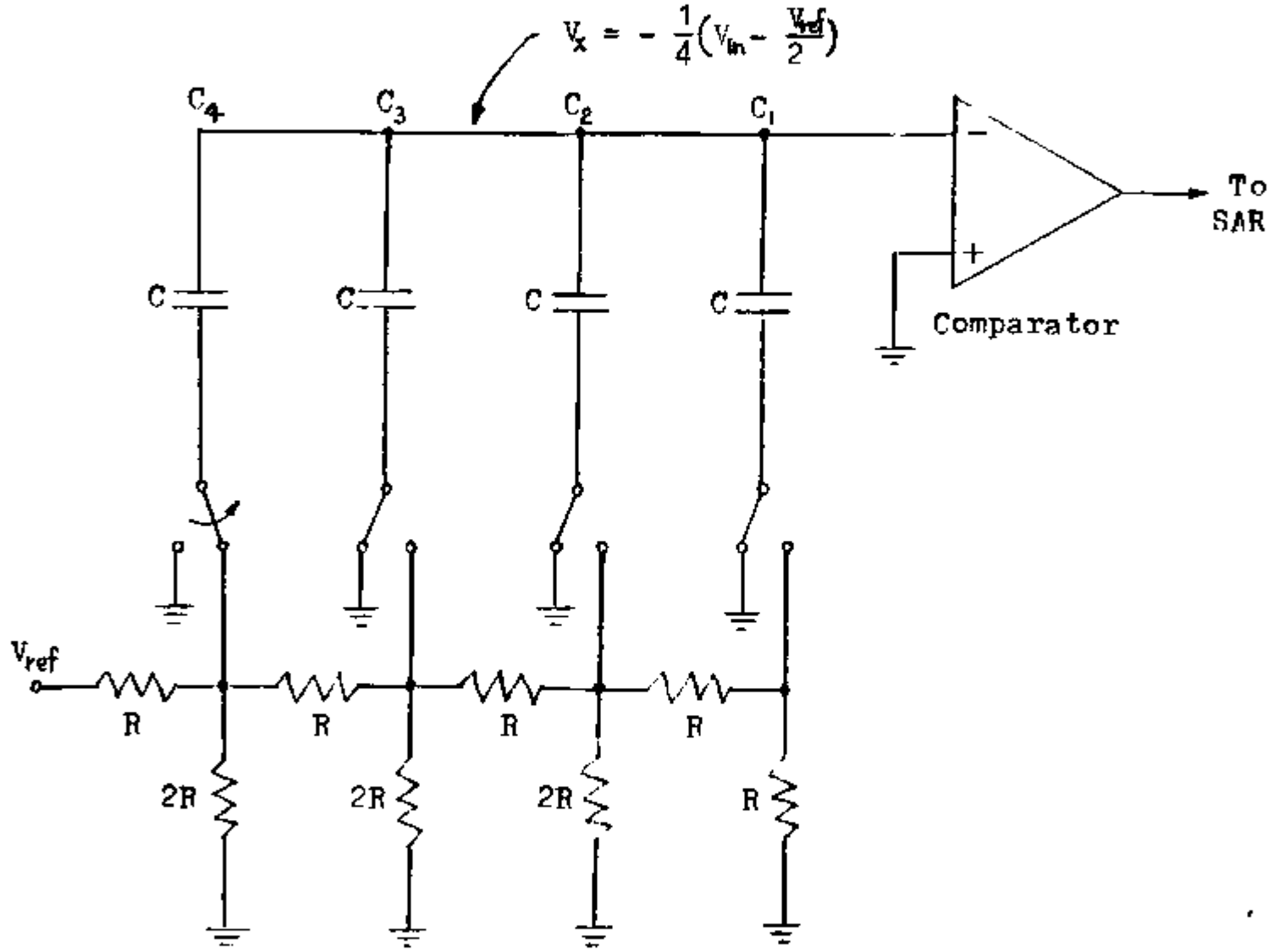


Figure 3.3: Redistribution mode operation of 4-bit A/D converter.

in Figure 3.4, the sample mode is accomplished by switching the bottom plates of this whole array to V_{in} while the capacitors $C_1, C_2, \ldots, C_M$ remain connected to ground. In the hold mode of Figure 3.5, the potential at the top plate of the capacitors becomes $-2^K V_{in}/(2^{K+M+1})$, where M and K are the numbers of bits provided by the R-2R ladder and the binary-weighted capacitor array, respectively. Thus, the comparator sensitivity requirement can be relaxed by increasing the value of K. However, too large a value of K implies a slower conversion rate and an increase in chip area. Therefore, for an N-bit converter, where N = M + K, there is always a tradeoff between M and K. For instance, consider an 8-bit converter where both M and K are equal to 4. In contrast with the regular charge-redistribution converter which has a total capacitance of 256 C, this converter requires only 21 C where C is the value of the smallest capacitor. Yet the comparator sensitivity requirement is increased by only approximately 30%. Thus, with the addition of several resistors, less chip area is required while the conversion speed is improved. The advantages become even more significant at higher bit counts, although the accuracy of the converter would be limited by the matching requirements of the resistors and capacitors.

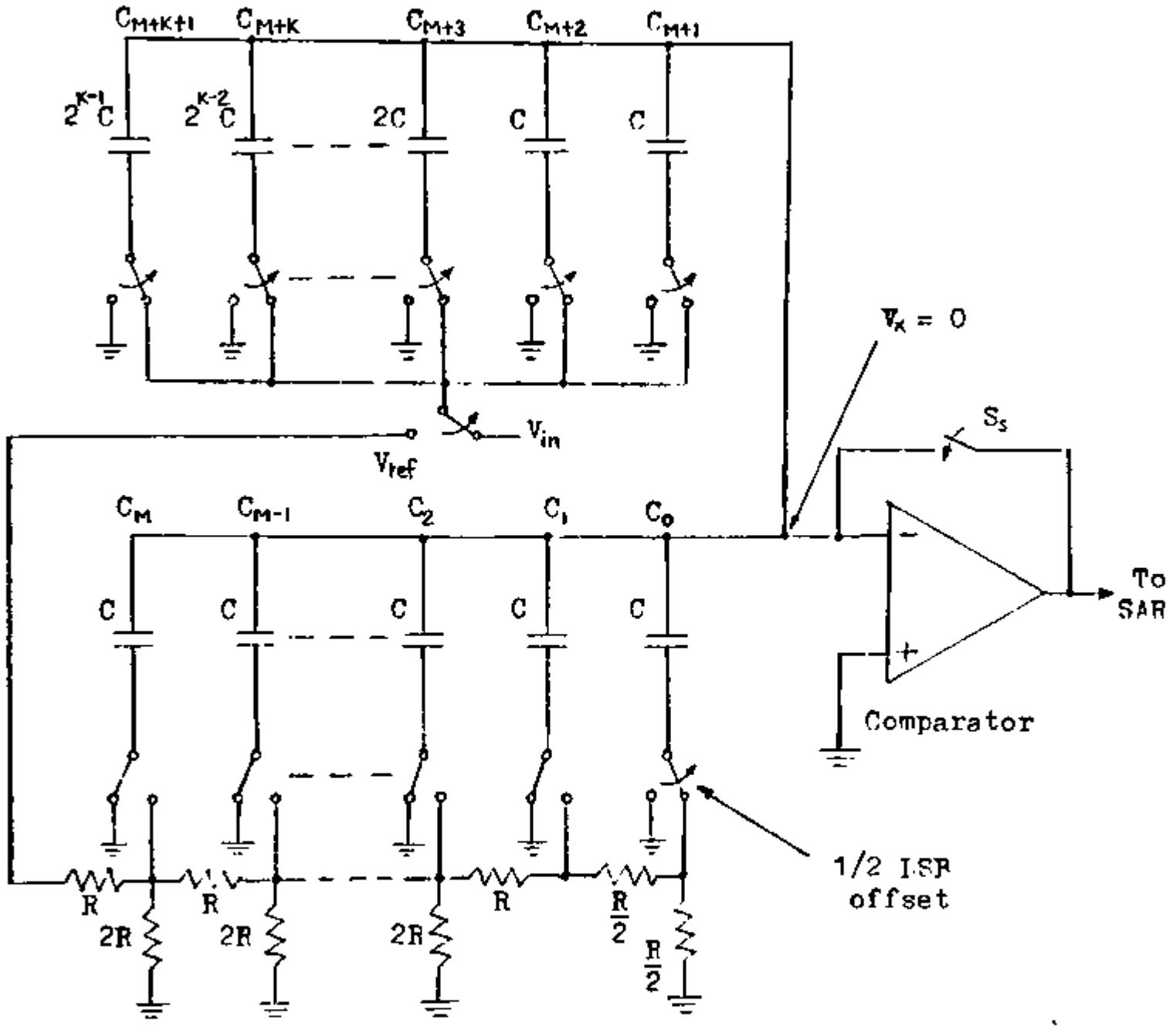


Figure 3.4: Sample mode operation of (M+K)-bit A/D converter.

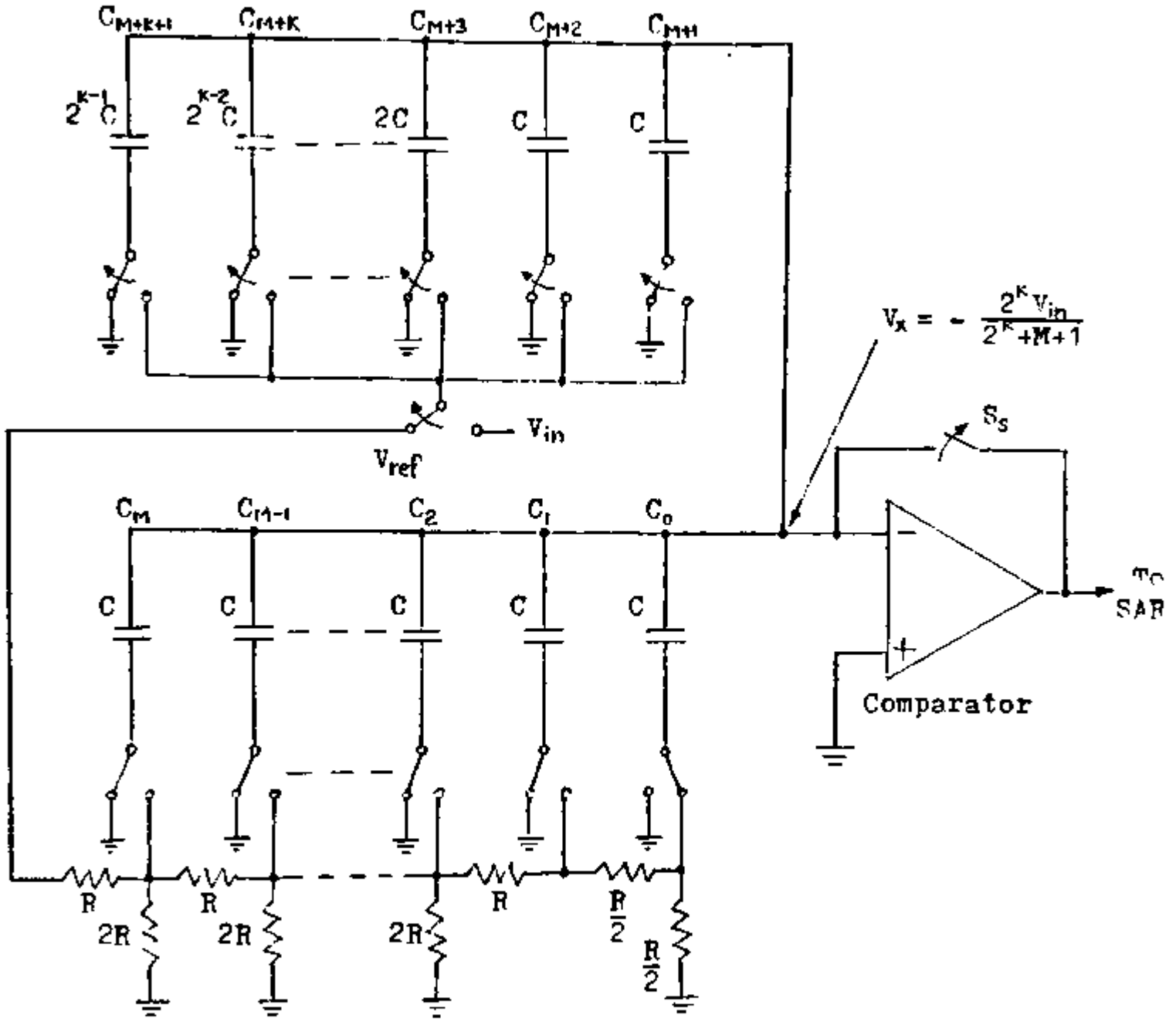


Figure 3.5: Hold mode operation of (M+K)-bit A/D converter.

During the sample mode (Figure 3.4), the offset voltage of the comparator is stored by closing S_S. Also, the bottom plate of C_o is switched to the position between the two R/2 resistors. Thus, the 1/2 LSB offset error can be eliminated by returning the bottom plate to ground during the redistribution mode. Since this converter bears a great deal of similarities to the regular charge-redistribution converter, it also shares some of the advantages. Consequently, the converter is insensitive to top-plate parasitic capacitances and its accuracy is not affected by bottom-plate parasitics. Bipolar voltage inputs can also be encoded using the single positive reference by modifying the array switching scheme {4}.

Accuracy and Speed Considerations

The major factor that limits the accuracy and speed of this A/D converter is the component mismatch. By increasing the areas of both capacitors and resistors, the matching error can be reduced. This, however, tends to decrease the conversion speed. Although the combination of capacitors and resistors gives a larger matching error than that of the capacitors themselves, it is used only at the lesser significant bits. Therefore, the practical resolution achievable should be about the same as that of the regular

charge-redistribution converter, which is about 8 to 10 bits.

While diffused resistors of proper sheet resistance are not available in the standard single-channel technology {4}, the resistors can be realized by ion-implantation techniques, giving values in the order of kilohms {1}. The R-2R resistor ladder has the property that every node has an equivalent resistance of R to ground (Figure 3.4). Although this resistance is not large as compared to the on-resistance of a switch which is typically several kilohms, it seems that the charging time would be increased. However, since the total capacitance has been reduced significantly as compared to the regular charge-redistribution converter with the same resolution, the conversion speed should turn out to be faster.

CHAPTER IV

IMPROVING PERFORMANCE OF SELF-CALIBRATION TECHNIQUE

High performance A/D converters with resolution and linearity above 11 bits are desired for many practical applications. Unfortunately, without laser trimming, a large number of converters are not able to meet these requirements. Recently, a high-resolution A/D converter has been proposed {8}. The design is based on a self-calibration technique. The R-2R charge-redistribution converter can be combined with the self-calibration technique to further enhance the conversion performance.

Self-Calibration Technique

A self-calibration A/D converter is illustrated in Figure 4.1. It consists of an N-bit binary-weighted capacitor array main D/A converter (DAC), an L-bit resistor string sub DAC, and a resistor string calibration DAC. The calibration DAC needs to have 2 more bits of resolution than the sub DAC since its ratio errors and overall quantization errors will accumulate during digital computation of error voltages of the main DAC.

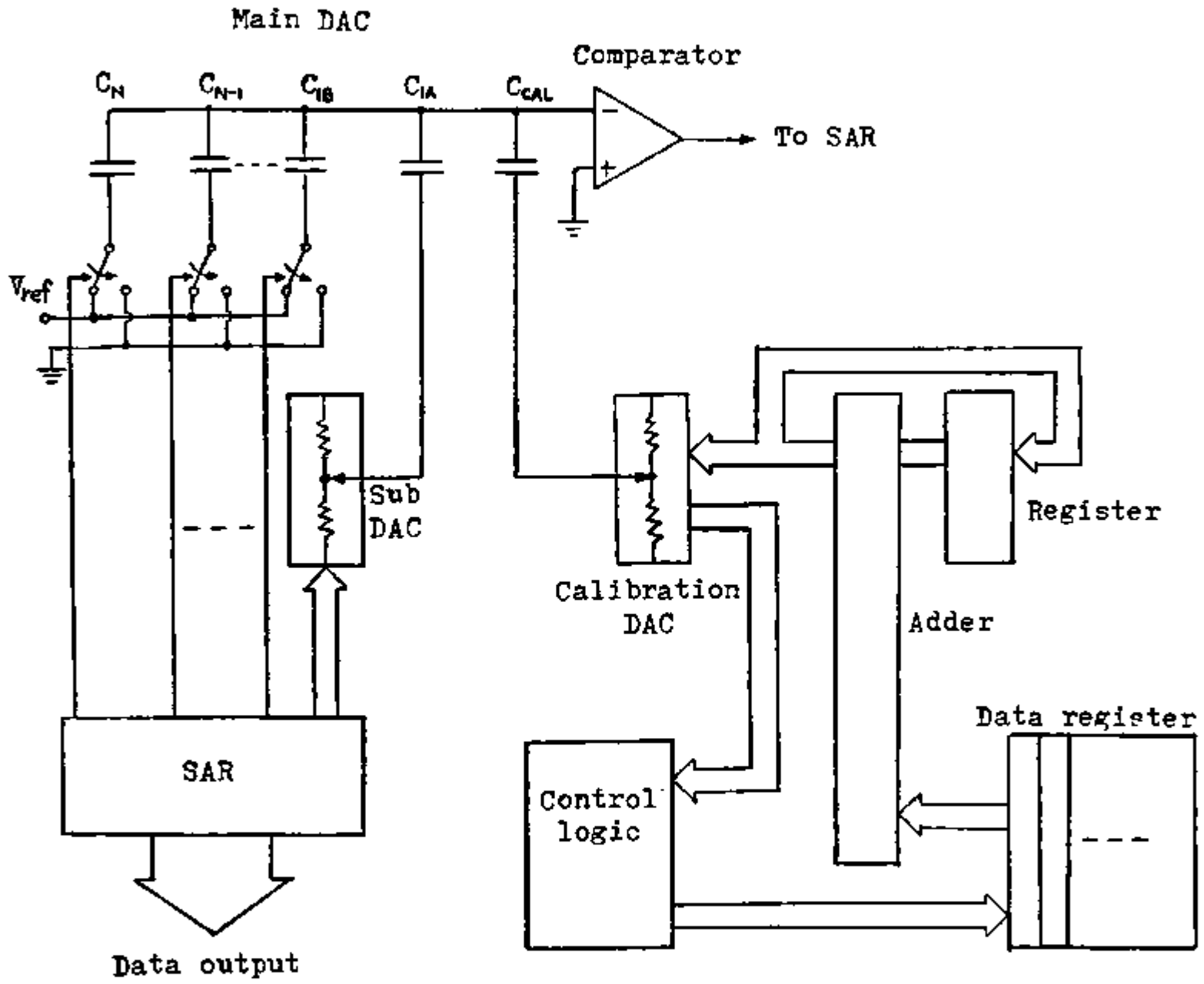


Figure 4.1: Block diagram of self-calibration A/D converter.

The calibration cycle is performed each time power is applied, or whenever necessary. It begins by measuring the nonlinearity caused by the MSB capacitor. This is achieved by sampling the reference voltage V_{ref} on all the capacitors except the MSB capacitor. The charge is then redistributed by reversing the switching configuration. A resulting residual voltage at the top plate, which is a measure of the error in the MSB capacitor, is digitized by successive approximation using the calibration DAC. This procedure is then repeated for the smaller capacitors. With the result stored in digital memory, error-correction voltages are added or subtracted by proper adjustment of the calibration DAC digital input code during the normal successive-approximation conversion cycles. Thus, the nonlinearity due to the main DAC can be cancelled.

Modifying Main DAC

The R-2R charge-redistribution converter can be applied to the self-calibration technique to improve its performance. As illustrated in Figure 4.2, the R-2R converter is used as the main DAC. The resistor string, which is used simultaneously for both sub DAC and calibration DAC by employing two sets of switches, is combined with the last resistor of the R-2R ladder to give an equivalent resistance

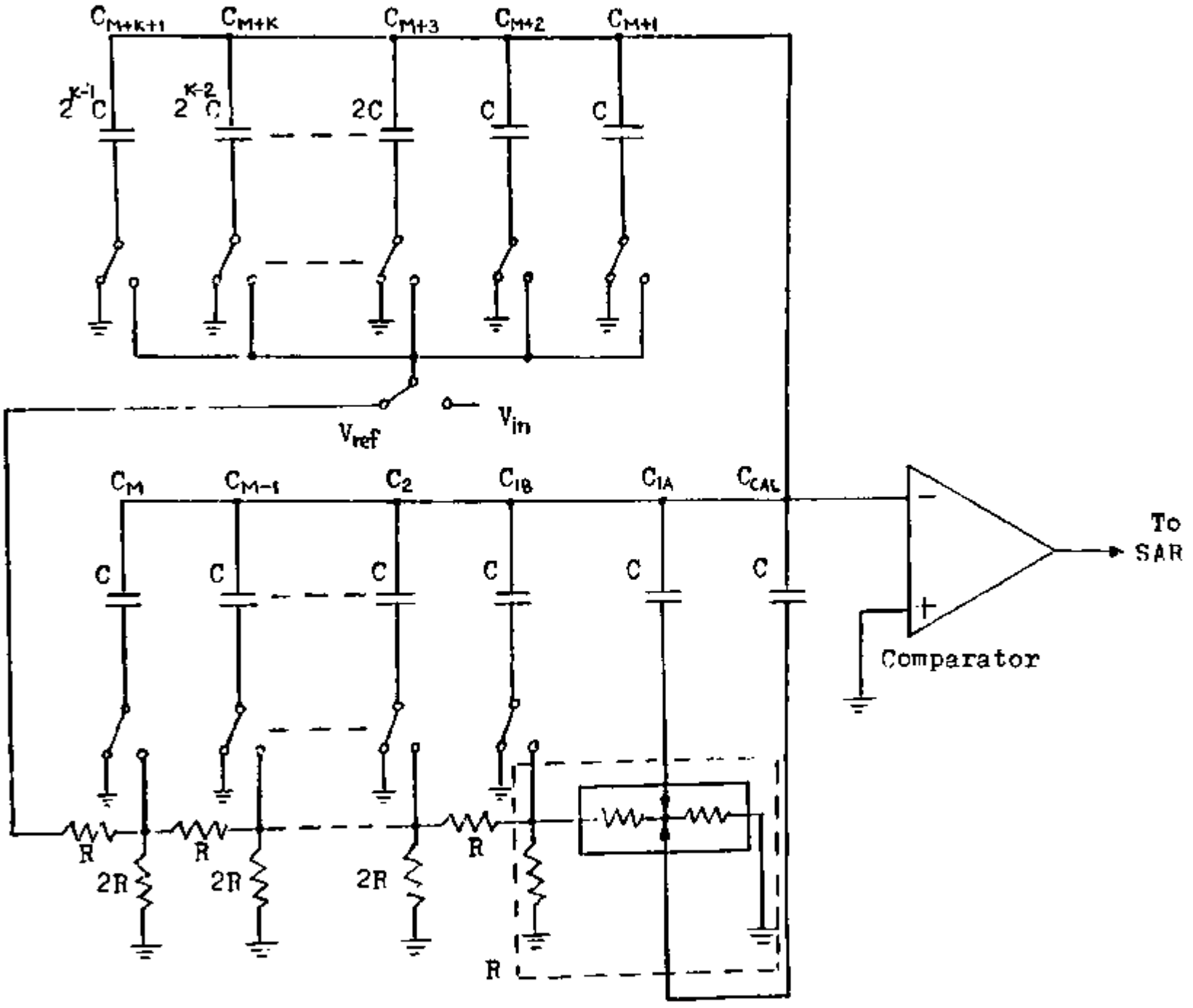


Figure 4.2: Self-calibration by modifying main DAC.

of R. Since only the binary-weighted capacitor array can be calibrated, it is necessary for the capacitor array to provide enough accuracy for the main DAC. The combination of R-2R resistor ladder and unit capacitors has to be accurate up to the largest significant bit it provides. For instance, a 13-bit converter may have a 4-bit sub DAC and a main DAC consisting of a 5-bit capacitor array and a 4-bit R-2R resistor ladder. Then the capacitor array and the R-2R resistor ladder plus unit capacitors need to provide 9-bit and 8-bit accuracy, respectively. The use of the resistor string has the advantage of monotonicity since it is inherently free of differential nonlinearity. While the capacitor array provides relatively good integral linearity {8}, the combination of R-2R resistor ladder and unit capacitors would result in reducing chip area and increasing conversion speed.

Modifying Calibration and Sub DAC's

The number of resistors and switches can be reduced by using the R-2R resistor ladder as the sub DAC and calibration DAC. A 12-bit version of the A/D converter is illustrated in Figure 4.3 where a 6-bit capacitor array is used as the main DAC. The R-2R resistor ladder, consisting of 16 resistors, is able to provide 8 bits of resolution.

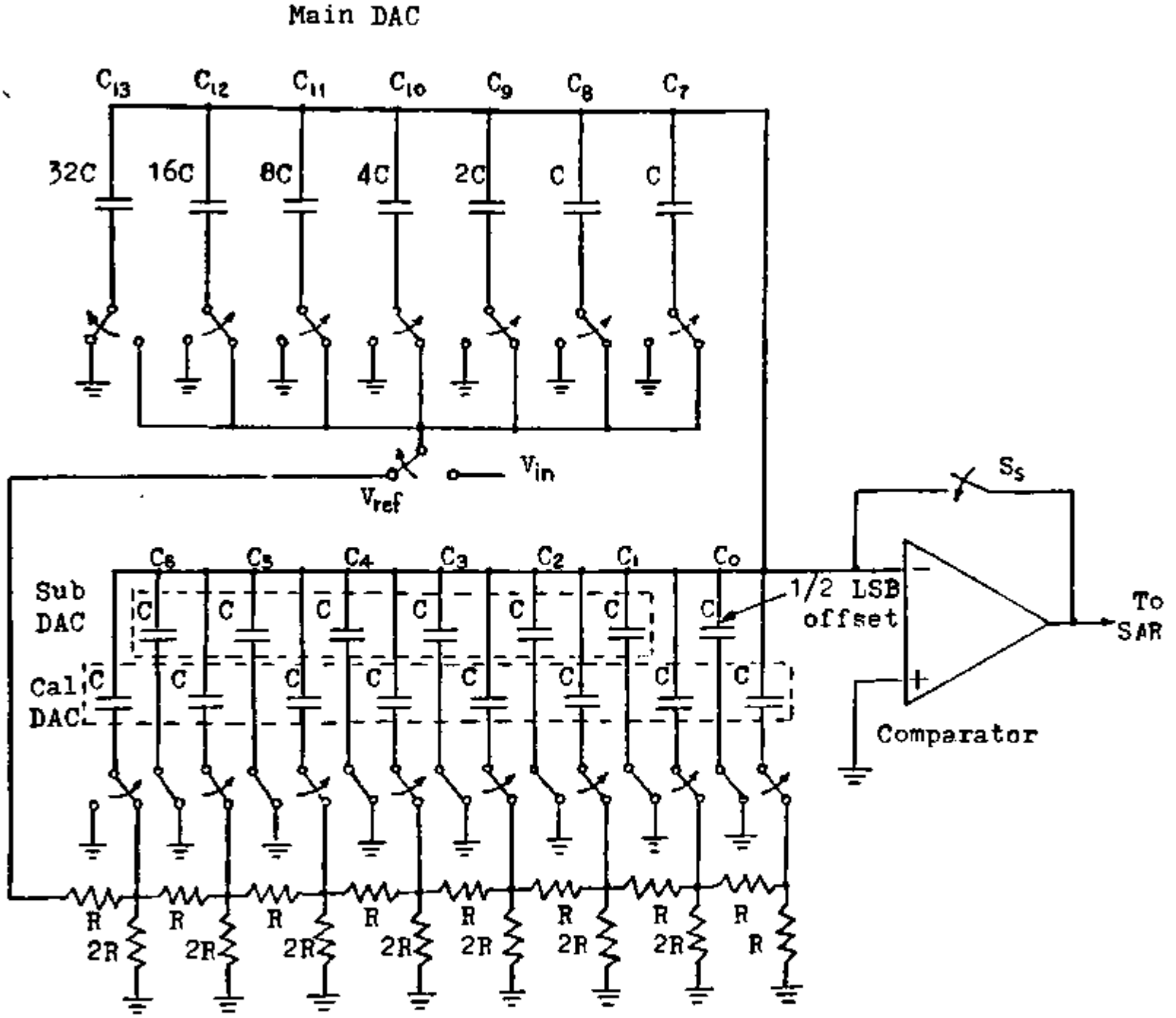


Figure 4.3: Precharge cycle of modified 12-bit A/D converter.

Out of the 15 unit capacitors used in conjunction with the ladder, 6 are used for the sub DAC, 8 are used for the calibration DAC while the remaining one is used to cancel the 1/2 LSB offset error. The bottom plate of each unit capacitor is connected by a single-pole double-throw switch, giving a total of 15 switches. Thus, the number of components required is much less than that of an 8-bit resistor string DAC, which requires 256 resistors and 510 analog switches {5}.

Since the nonlinearity errors of the capacitor array can be positive or negative, the calibration DAC needs to be able to handle both polarities. This is accomplished by switching all the bottom plates of the calibration DAC to the nodes of the R-2R ladder when sampling the reference voltage during the calibration cycle. An example for the calibration of the MSB capacitor is shown in Figure 4.3. After reversing the switching configuration of the binary-weighted capacitor array, the residual voltage at the top plate can then be measured. If it is positive, a successive approximation is performed by switching the appropriate bottom plates of the calibration DAC to ground. Otherwise, the bottom plate of the last unit capacitor C_7 in the capacitor array is switched to V_{ref} and a successive approximation is again performed (Figure 4.4). This is similar to the idea

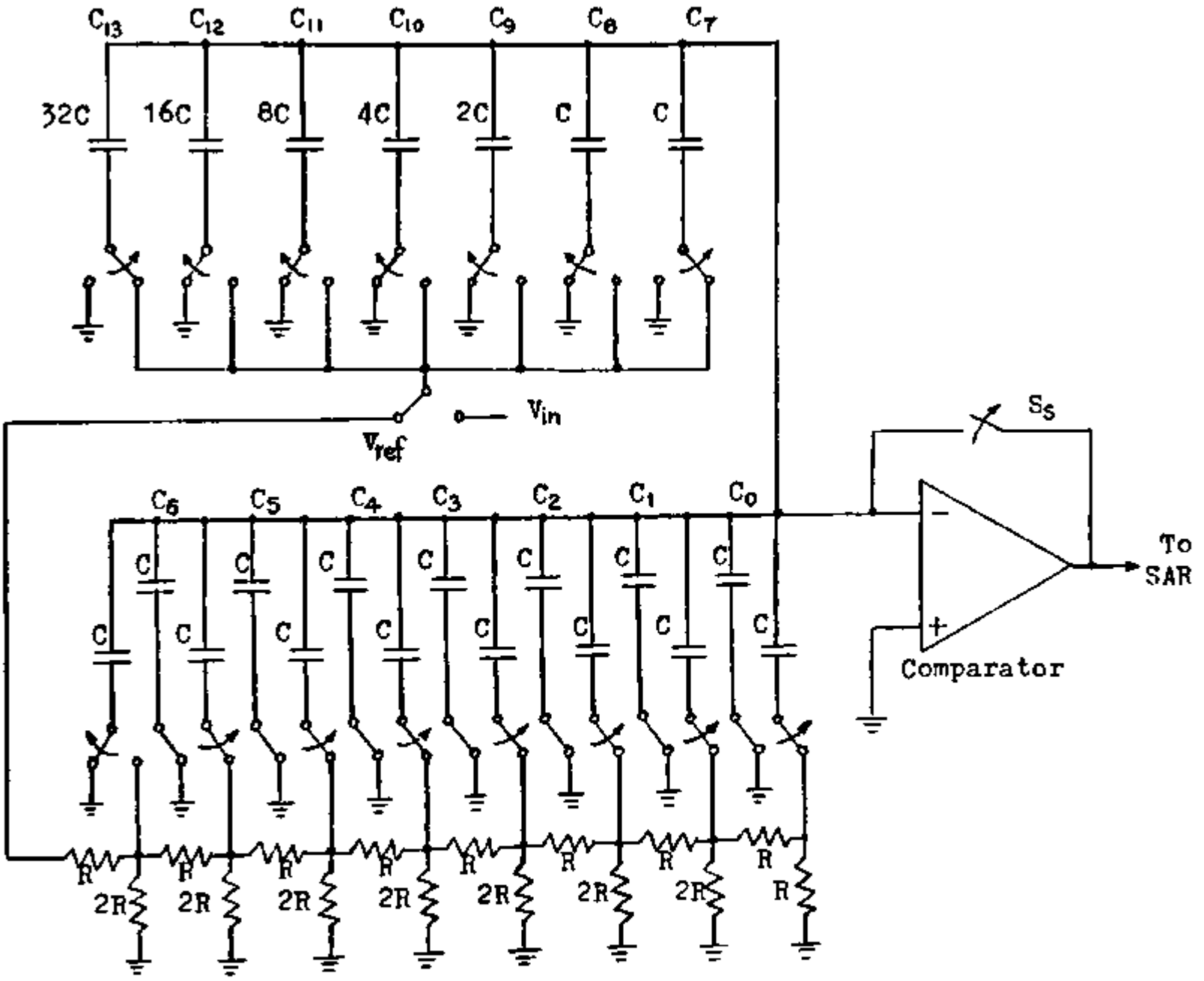


Figure 4.4: Charge redistribution and error acquisition of modified 12-bit A/D converter.

of 2's complement. The same principle is applied to add or subtract the error-correction voltages during the normal conversion cycles.

CHAPTER V

CONCLUSION

A number of MOS successive-approximation A/D converters have been reviewed. The charge-redistribution A/D converter uses capacitors as its passive components, whereas the potentiometric A/D converter uses resistors instead. The other A/D converters use combinations of both capacitors and resistors to increase resolution and reduce the number of components.

An R-2R charge-redistribution A/D converter is then proposed. As compared to the regular charge-redistribution converter which scales only capacitor ratios, it also scales voltages by using an R-2R resistor ladder. Thus, the total capacitance can be reduced. Since the R-2R configuration can effectively divide the reference voltage into successive levels, the resulting converter requires less chip area with a higher conversion speed.

It has also been shown that the R-2R configuration can be used to calibrate the binary-weighted capacitor array in a self-calibration technique. This significantly reduces the number of components normally required by a resistor string.

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